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MICROCOMPUTER MN101E

MN101E01K/01L/01M/F01M

LSI User's Manual

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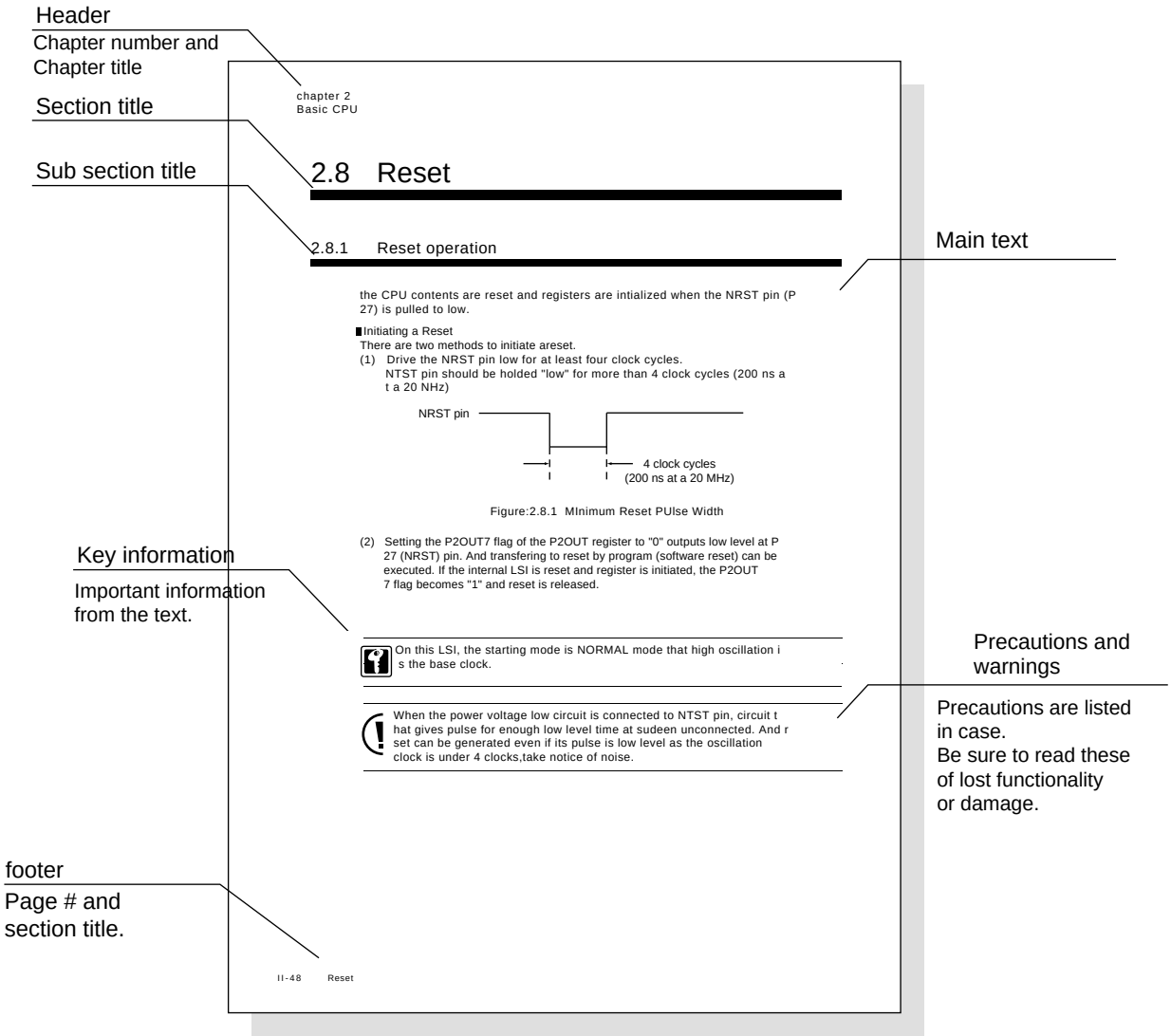
About This Manual

■Organization

In this LSI manual, this LSI functions are presented in the following order : overview, basic CPU functions, interrupt functions, port functions, timer functions, serial functions, and other peripheral hardware functions. Each section contains overview of function, block diagram, control register, operation, and setting example.

■Manual Configuration

Each section of this manual consists of a title, summary, main text, key information, precautions and warnings, and references.The layout and definition of each section are shown below.


Header
Chapter number and Chapter title
Section title
Sub section title
chapter 2
Basic CPU
2.8 Reset
2.8.1 Reset operation
Main text
the CPU contents are reset and registers are intialized when the NRST pin (P 27) is pulled to low.
Initiating a Reset
There are two methods to initiate areset.
(1) Drive the NRST pin low for at least four clock cycles.
NTST pin should be holded "low" for more than 4 clock cycles (200 ns a t a 20 NHz)
NRST pin
4 clock cycles
(200 ns at a 20 MHz)
Figure:2.8.1 MInimum Reset PUlse Width
(2) Setting the P2OUT7 flag of the P2OUT register to "0" outputs low level at P 27 (NRST) pin. And transfering to reset by program (software reset) can be executed. If the internal LSI is reset and register is initiated, the P2OUT 7 flag becomes "1" and reset is released.
Key information
Important information from the text.
On this LSI, the starting mode is NORMAL mode that high oscillation i s the base clock.
When the power voltage low circuit is connected to NTST pin, circuit t hat gives pulse for enough low level time at sudeen unconnected. And r set can be generated even if its pulse is low level as the oscillation clock is under 4 clocks,take notice of noise.
Precautions and warnings
Precautions are listed in case.
Be sure to read these of lost functionality or damage.
footer
Page # and section title.
II-48 Reset

■Finding Desired Information

This manual provides three methods for finding desired information quickly and easily.

1.Consult the index at the front of the manual to locate the beginning of each section.

2.Consult the table of contents at the front of the manual to locate desired titles.

3.A chapter number and its chapter title are located at the top corner of each page, and section titles are located at the bottom corner of each page.

■Related Manuals

Note that the following related documents are available.

- "MN101E Series Instruction Manual"
  <Describes the instruction set.>
- " Series C/E Compiler User's Manual: Usage Guide"
  <Describes the installation, the commands, and options of the C Compiler.>
- "MN101C Series C Compiler User's Manual: Language Description"
  <Describes the syntax of the C Compiler.>
- "MN101C Series C Compiler User's Manual: Library Reference"
  <Describes the standard library of the C Compiler.>
- "MN101 C/E Series Cross-assembler User's Manual"
  <Describes the assembler syntax and notation.>
- "MN101E Series C Source Code Debugger User's Manual"
  <Describes the use of C source code debugger.>
- About This Manual "MN101E Series PanaX Series Installation Manual"
  <Describes the installation of C compiler, cross-assembler and C source code debugger and the procedure for bringing up the in-circuit emulator.>

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Chapter 1 Overview

1

1.1 Overview

1.1.1 Overview

The MN101E series of 8-bit single-chip microcomputers (the memory expansion version of MN101C series) incorporate multiple types of peripheral functions. This chip series is well suited for camera, VCR, MD, TV, CD, LD, printer, telephone, home automation, pager, air conditioner, PPC, remote control, fax machine, music instrument and other applications.

This LSI brings to embedded microcomputer applications flexible, optimized hardware configurations and a simple efficient instruction set. The MN101E01L has an internal 320 KB of ROM and 14 KB of RAM. Peripheral functions include 6 external interrupts, 20 internal interrupts including NMI, 9 timer counters, 5 sets of serial interfaces, A/D converter, D/A converter, watchdog timer, automatic data transfer, synchronous output function, buzzer output, and remote control output. The configuration of this microcomputer is well suited for application as a system controller in a air conditioner, camera, timer selector for VCR, CD player, or MD.

With two oscillation system (max. 32 MHz/32 kHz) contained on the chip, the system clock can be switched to high frequency input (high speed mode), or to low frequency input (low speed mode). The system clock is generated by dividing the oscillation clock. The best operation clock for the system can be selected by switching its frequency by software.

A machine cycle (min. instructions execution) in the normal mode is 250 ns when fosc is 8 MHz, and when fosc is 20 MHz, a machine cycle is 100 ns. A machine cycle in the double speed mode is 62.5 ns when fosc is 32 MHz, and 100 ns when fosc is 10 MHz. The package is 100-pin QFP.

1.1.2 Product Summary

This manual describes the following models of the MN101E01L series. These products have identical functions. Please note that mainly dealed here is MN101E01L and MN101EF01M is described in the separate volume.

Table:1.1.1 Product Summary

Model	ROM Size	RAM Size	Classification
MN101E01K*	256 KB	10 KB	Mask ROM version
MN101E01L*	320 KB	14 KB	Mask ROM version
MN101E01M*	384 KB	24 KB	Mask ROM version
MN101EF01M*	384 KB	24 KB	Flash EEPROM version

* Under development

1.2Hardware Functions

CPU Core

MN101E Core

LOAD-STORE architecture (3-stage pipeline)

- Half-byte instruction set / Handy addressing
- Memory space 1 MB (instruction / data share)
- Machine cycle

High speed mode	Normal	62.5 µs	/	32 MHz	(3.0 V to 3.6 V)
		100.0 µs	/	10 MHz	(3.0 V to 3.6 V)
Low speed mode		61.0 µs	/	32.768 kHz	(3.0 V to 3.6 V)

- Operation modes

NORMAL mode	(High speed mode)
SLOW mode	(Low speed mode)
HALT mode	
STOP mode	

The operation clock can be switched in each mode.¶

Oscilalting circuit

Internal memory

ROM 320 KB
RAM 14 KB

Memory bank

Data memory space is expanded by the bank system.

- Bank for the source address / Bank for the destination address

ROM correction

- Maximum 3 parts of the program can be corrected.

Operating tempre-ture

- -40 °C to +85 °C (Mask ROM version)

Interrupts

20 Internal interrupts

[Incorrect code execution interrupts]

- Non maskable interrupt (NMI)

[Timer interrupts]

- Timer 0 interrupt
- Timer 1 interrupt
- Timer 2 interrupt
- Timer 3 interrupt
- Timer 4 interrupt
- Timer 5 interrupt

- Timer 6 interrupt
- Time base interrupt
- Timer 7 interrupt
- Match interrupt for Timer 7 compare register 2

[Serial interrupts]

- Serial 0 interrupt
- Serial 0 UART reception interrupt
- Serial 1 interrupt
- Serial 1 UART reception interrupt
- Serial 2 interrupt
- Serial 3 interrupt
- Serial 4 interrupt
- Serial 4 UART reception interrupt

[A/D interrupt]

- A/D conversion interrupt

[Automatic data transfer interrupts]

- ATC1 interrupt

6 External interrupts

- IRQ0 Edge selectable, noise filter connectable
- IRQ1 Edge selectable, noise filter connectable
- IRQ2 Edge selectable, both edges interrupt (STOP/HALT: recovered at both edges), level interrupt
- IRQ3 Edge selectable, both edges interrupt (STOP/HALT: recovered at both edges), level interrupt
- IRQ4 Edge selectable, key interrupt
- IRQ5 Edge selectable, both edges interrupt (STOP/HALT: recovered at both edges), level interrupt

Timer / Counters 9 Timers (8 can be operated independently)

· 8-bit timer for general use	2 sets
· 8-bit timer (also serves as UART baud rate timer)	4 sets
· 8-bit free-running timer	1 set
Time base timer	1 set
· 16-bit timer for general use	1 set

Timer 0 (8-bit timer for general use)

- Square wave output (timer pulse output), PWM output, Event count, Simple pulse with measurement, Real time output control, Remote control carrier output
- Clock source

  fosc, fosc/4, fosc/16, fosc/32, fosc/64, fs/2, fs/4, fx, external clock

Timer 1 (8-bit timer for general use)

- Square wave output (timer pulse output), Event count, Timer synchronous output, 16-bit cascade connection function (connected to timer 0)
- Clock source

  fosc, fosc/4, fosc/16, fosc/64, fosc/128, fs/2, fs/8, fx, external clock

Timer 2 (8-bit timer also serves as UART baud rate timer)

- Square wave output (timer pulse output), PWM output, Event count, Serial transfer clock output, Timer synchronous output, Simple pulse with measurement, Real time output control
- Clock source

  fosc, fosc/4, fosc/16, fosc/32, fosc/64, fs/2, fs/4, fx, external clock

Timer 3 (8-bit timer also serves as UART baud rate timer)

- Square wave output (timer pulse output), Event count, Serial transfer clock, 16-bit cascade connection function (connected to timer 2), Remote control carrier output
- Clock source

  fosc, fosc/4, fosc/16, fosc/64, fosc/128, fs/2, fs/8, fx, external clock

Timer 4 (8-bit timer also serves as UART baud rate timer)

- Square wave output (timer pulse output), PWM output, Event count, Simple pulse with measurement, Serial transfer clock
- Clock source

  fosc, fosc/4, fosc/16, fosc/32, fosc/64, fs/2, fs/4, fx, external clock

Timer 5 (8-bit timer also serves as UART baud rate timer)

- Square wave output (timer pulse output), PWM output, Event count, Serial transfer clock, 16-bit cascade connection function (connected to timer 4)
- Clock source

  fosc, fosc/4, fosc/16, fosc/64, fosc/128, fs/2, fs/8
  , fx, external clock

Timer 6 (8-bit free-running timer, Time base timer)

8-bit free-running timer

- Clock source

  fosc, fosc/2^{12} fosc/2^{13}, fs, fx, fx/2^{12}, fx/2^{13}

Time base timer

- Interrupt generation cycle

  fosc/2^{7}, fosc/2^{8}, fosc/2^{9}, fosc/2^{10}, fosc/2^{13}, fosc/2^{15},
  fx/2^{7}, fx/2^{8}, fx/2^{9}, fx/2^{10}, fx/2^{13}, fx/2^{15}

Timer 7 (16-bit timer for general use)

- Square wave output (Timer pulse output), Event count, High precision PWM output (Cycle/Duty can be changed constantly), Timer synchronous output, Input capture function (Both edges can be operated), Real time output control (at tthe falling edge of external interrupt (IRQ0), the value of PWM output (timer output) is selected from these three values; “fixed to high”, “fixed to low” and “Hi-z”.)
- Clock source

  fosc, fosc/2, fosc/4, fosc/16, fs, fs/2, fs/4, fs/16

  1/1, 1/2, 1/4, 1/16 of the external clock
- Hardware organization

Compare register with double buffer	2 sets
Input capture register	1 set
Timer interrupt	2 vectors

Watchdog timer

- Time-out period can be selected from $fs/2^{16}$, $fs/2^{18}$, $fs/2^{20}$, $fs/2^{22}$
- On detection of errors, hard reset is done inside LSI. (NMI interrupt is generated in the first execution and it is hard reset in the continuous interrupts.)

Remote control output

Based on the timer 0 and timer 3 output, a remote control carrier with duty cycle of 1/1, 1/2 or 1/3 can be output.

Synchronous output function

Timer synchronous output, interrupt synchronous output

- Port 7 outputs the latched data, on the event timing of the synchronous output signal of timer 1, 2, of 7, or of the external interrupt 2 (IRQ2).

Buzzer output

Output frequency can be selected from $fosc/2^9$, $fosc/2^{10}$, $fosc/2^{11}$, $fosc/2^{12}$, $fosc/2^{13}$, $fosc/2^{14}$, $fx/2^3$, $fx/2^4$.

Data automatic transfer

Data is transferred automatically in all memory space (1 MB)

- Startup the external interrupt / internal event / software.
- 255 byte max. can be transferred continuously.
- Support continuous serial transmission / reception.
- Burst transfer function (Urgent stop of interrupts is contained.)

A/D converter

10 bits ×8 channel

D/A converter

8 bits ×1 channel

Serial interface

5 types

Serial 0 (Full duplex UART / Synchronous serial interface)

Synchronous serial interface

- Transfer clock source

  fosc/2, fosc/4, fosc/16, fosc/64, fs/2, fs/4,
  Timer 2 (Timer 4) output
- MSB/LSB can be selected as the first bit to be transferred. An arbitrate transfer size from 1 to 8 bits can be selected.
- Sequence transmission, reception or both are available.

Full duplex UART (Baud rate timer, timer 2 or timer 4)

- Parity check, Overrun error / Framing error detection
- Transfer size 7 to 8 bits can be selected.
- In UART communication, transmission complete interrupt and reception complete interrupt are available.

Serial 1 (Full duplex UART / Synchronous serial interface)

Synchronous serial interface

- Transfer clock source

  fosc/2, fosc/4, fosc/16, fosc/64, fs/2, fs/4,
  Timer 4 (Timer 5) output

- MSB/LSB can be selected as the first bit to be transferred. An arbitrate transfer size from 1 to 8 bits can be selected.
- Sequence transmission, reception or both are available.

Full duplex UART (Baud rate timer, timer 4 or timer 5)

- Parity check, Overrun error / Framing error detection
- Transfer size 7 to 8 bits can be selected.
- In UART communication, transmission complete interrupt and reception complete interrupt are available.

Serial 2 (Single master IIC / Synchronous serial interface)

Synchronous serial interface

- Transfer clock source

  fosc/2, fosc/4, fosc/8, fosc/16, fosc/32, fosc/64, fosc/128, fs/2, fs/4,
  Timer 2 (Timer 3) output, External clock
- MSB/LSB can be selected as the first bit to be transferred. An arbitrate transfer size from 1 to 8 bits can be selected.
- Sequence transmission, reception or both are available.

Single master IIC

- Single master IIC communication is available (9 bits transfer)

Serial 3 (Single master IIC / Synchronous serial interface)

Synchronous serial interface

- Transfer clock source

  fosc/2, fosc/4, fosc/8, fosc/16, fosc/32, fosc/64, fosc/128, fs/2, fs/4,
  Timer 3 (Timer 5) output
- MSB/LSB can be selected as the first bit to be transferred. An arbitrate transfer size from 1 to 8 bits can be selected.
- Sequence transmission, reception or both are available.

Single master IIC

- Single master IIC communication is available (9 bits transfer)

Serial 4 (Full duplex UART / Synchronous serial interface)

Synchronous serial interface

- Transfer clock source

  fosc/2, fosc/4, fosc/16, fosc/64, fs/2, fs/4,
  Timer 2 (Timer 5) output, External clock
- MSB/LSB can be selected as the first bit to be transferred. An arbitrate transfer size from 1 to 8 bits can be selected.
- Sequence transmission, reception or both are available.

Full duplex UART (Baud rate timer, timer 2 or timer 5)

- Parity check, Overrun error / Framing error detection
- Transfer size 7 to 8 bits can be selected.

  In UART communication, transmission complete interrupt and reception complete interrupt are available.

*) Maximum transfer clock of each serial interface: 5 MHz

LED driver

- LED (large current) driver ports 8 ports

Port		
	· I/O ports (I/F port for 5 V I/O)	34 ports
	Usable as A/D input	8 ports
	· I/O ports (I/F port for 3 V I/O)	50 ports
	LED (large current) driver ports	8 ports (push-pull configuration)
	Usable as D/A output	1 port
	· Special function pins	16 pins
	· Analog reference voltage input pin	3 pins
	· Operation mode input pin	2 pins
	· Reset input pin	1 pin
	· Power pin	8 pins
	· Internal power pin	3 pins *1
	· External power pin	3 pins *2
	Oscillator pins	4 pins
	*1 Voltage for internal power pin : 3.0 V to 3.6 V	
	*2 Voltage for external power pin : 3.0 V to 5.5 V	
Package	100 pinQFP (18 mm square/0.65 mm pitch)	

1.3 Pin Description

1.3.1 Pin configuration

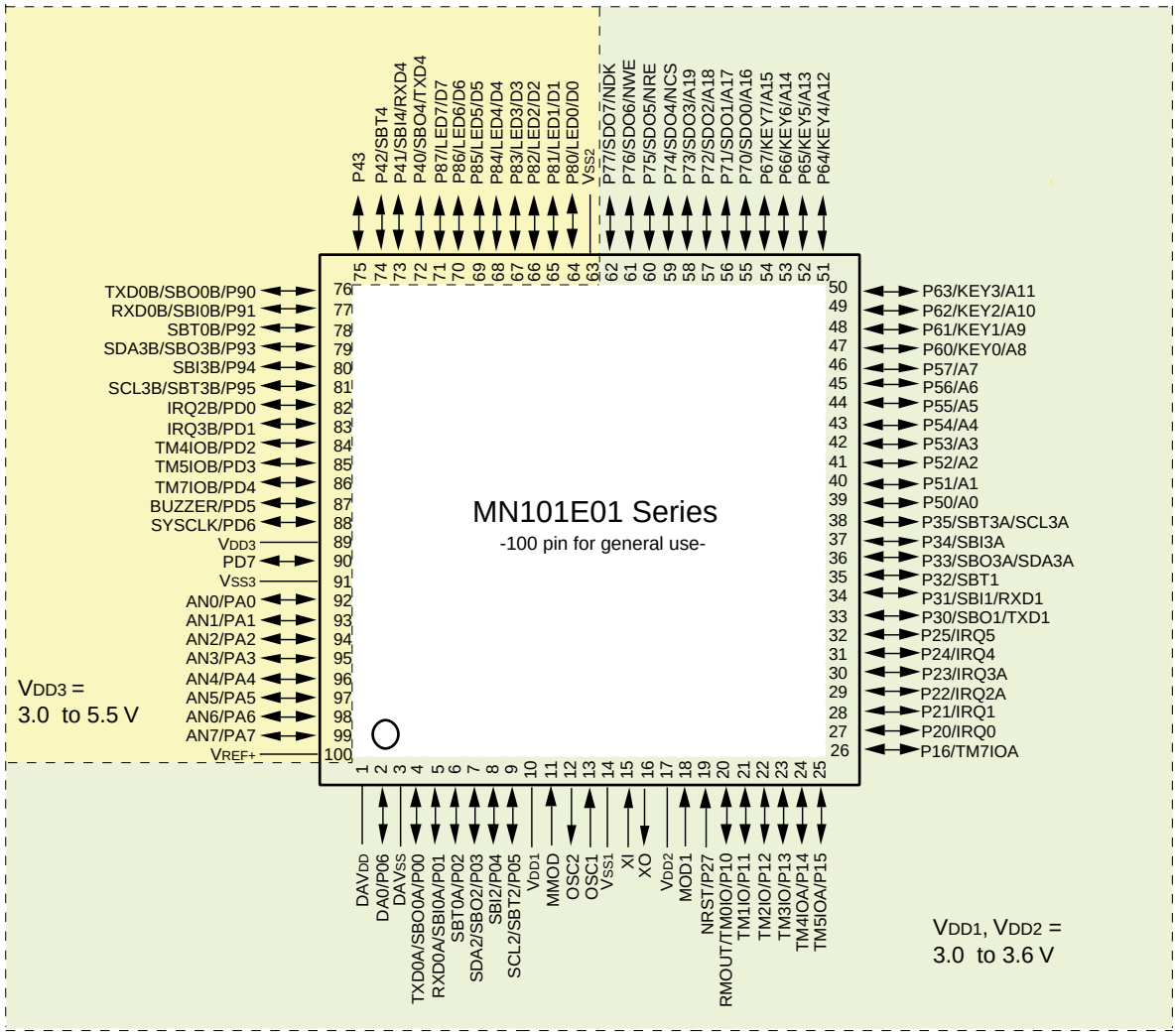


Figure:1.3.1 Pin Configuration (100QFP: TOP VIEW)

1.3.2 Pin Specification

Table:1.3.1 Pin Specification

Pins	Special Functions		I/O	Direction Control	Pin Control	Functions Description	
P00	SBO0A	TXD0A	in/out	P0DIR0	P0PLU0	SBO0A: Serial 0 transmission data output	TXD0A: UART 0 transmission data output
P01	SBI0A	RXD0A	in/out	P0DIR1	P0PLU1	SBI0A: Serial 0 reception data input	RXD0A: UART 0 reception data input
P02	SBT0A		in/out	P0DIR2	P0PLU2	SBT0A: Serial 0 clock input / output	
P03	SBO2	SDA2	in/out	P0DIR3	P0PLU3	SBO2: Serial 2 transmission data output	SDA2: IIC2 data input / output
P04	SBI2		in/out	P0DIR4	P0PLU4	SBI2: Serial 2 reception data input	
P05	SBT2	SCL2	in/out	P0DIR5	P0PLU5	SBT2: Serial 2 clock input / output	SCL2: IIC2 clock input / output
P06	DA0		in/out	P0DIR6	P0PLU6	DA0: DA0 output	
P10	TM0IO	RMOUT	in/out	P1DIR0	P1PLU0	TM0IO: Timer 0 input / output	RMOUT: Remote control carrier output
P11	TM1IO		in/out	P1DIR1	P1PLU1	TM1IO: Timer 1 input / output	
P12	TM2IO		in/out	P1DIR2	P1PLU2	TM2IO: Timer 2 input / output	
P13	TM3IO		in/out	P1DIR3	P1PLU3	TM3IO: Timer 3 input / output	
P14	TM4IOA		in/out	P1DIR4	P1PLU4	TM4IOA: Timer 4 input / output	
P15	TM5IOA		in/out	P1DIR5	P1PLU5	TM5OA: Timer 5 input / output	
P16	TM7IOA		in/out	P1DIR6	P1PLU6	TM7IOA: Timer 7 input / output	
P20	IRQ0		in/out	P2DIR0	P2PLU0	IRQ0: External interrupt input 0	
P21	IRQ1		in/out	P2DIR1	P2PLU1	IRQ1: External interrupt input 1	
P22	IRQ2A		in/out	P2DIR2	P2PLU2	IRQ2A: External interrupt input 2	
P23	IRQ3A		in/out	P2DIR3	P2PLU3	IRQ3A: External interrupt input 3	
P24	IRQ4		in/out	P2DIR4	P2PLU4	IRQ4: External interrupt input 4	
P25	IRQ5		in/out	P2DIR5	P2PLU5	IRQ5: External interrupt input 5	
P27	NRST		in	-	-	NRST: Reset	
P30	SBO1	TXD1	in/out	P3DIR0	P3PLU0	SBO1: Serial 1 transmission data output	TXD1: UART 1 transmission data output
P31	SBI1	RXD1	in/out	P3DIR1	P3PLU1	SBI1: Serial 1 reception data input	RXD1:UART 1 reception data input
P32	SBT1		in/out	P3DIR2	P3PLU2	SBT1: Serial 1 clock input / output	
P33	SBO3A	SDA3A	in/out	P3DIR3	P3PLU3	SBO3A: Serial 3 transmission data output	SDA3A: IIC3 data input / output
P34	SBI3A		in/out	P3DIR4	P3PLU4	SBI3A: Serial 3 reception data input	
P35	SBT3A	SCL3A	in/out	P3DIR5	P3PLU4	SBT3A: Serial 3 clock input / output	SCL3A: IIC3 clock input / output
P40	SBO4	TXD4	in/out	P4DIR0	P4PLU0	SBO4: Serial 4 transmission data output	TXD4: UART 4 transmission data output
P41	SBI4	RXD4	in/out	P4DIR1	P4PLU1	SBI4: Serial 4 reception data input	RXD4: UART 4 reception data input
P42	SBT4		in/out	P4DIR2	P4PLU2	SBT4: Serial 4 clock input / output	
P43			in/out	P4DIR3	P4PLU3		
P50	A0		in/out	P5DIR0	P5PLU0	A0: Address output (bp0)	
P51	A1		in/out	P5DIR1	P5PLU1	A1: Address output (bp1)	
P52	A2		in/out	P5DIR2	P5PLU2	A2: Address output (bp2)	
P53	A3		in/out	P5DIR3	P5PLU3	A3: Address output (bp3)	
P54	A4		in/out	P5DIR4	P5PLU4	A4: Address output (bp4)	
P55	A5		in/out	P5DIR5	P5PLU5	A5: Address output (bp5)	
P56	A6		in/out	P5DIR6	P5PLU6	A6: Address output (bp6)	
P57	A7		in/out	P5DIR7	P5PLU7	A7: Address output (bp7)	

Pins	Special Functions		I/O	Direction Control	Pin Control	Functions Description	
P60	KEY0	A8	in/out	P6DIR0	P6PLU0	KEY0: KEY interrupt input 0	A8: Address output (bp8)
P61	KEY1	A9	in/out	P6DIR1	P6PLU1	KEY1: KEY interrupt input 1	A9: Address output (bp9)
P62	KEY2	A10	in/out	P6DIR2	P6PLU2	KEY2: KEY interrupt input 2	A10: Address output (bp10)
P63	KEY3	A11	in/out	P6DIR3	P6PLU3	KEY3: KEY interrupt input 3	A11: Address output (bp11)
P64	KEY4	A12	in/out	P6DIR4	P6PLU4	KEY4: KEY interrupt input 4	A12: Address output (bp12)
P65	KEY5	A13	in/out	P6DIR5	P6PLU5	KEY5: KEY interrupt input 5	A13: Address output (bp13)
P66	KEY6	A14	in/out	P6DIR6	P6PLU6	KEY6: KEY interrupt input 6	A14: Address output (bp14)
P67	KEY7	A15	in/out	P6DIR7	P6PLU7	KEY7: KEY interrupt input 7	A15: Address output (bp15)
P70	SDO0	A16	in/out	P7DIR0	P7PLU0	SDO0: Timer synchrpnous output 0	A16: Address output (bp16)
P71	SDO1	A16	in/out	P7DIR1	P7PLU1	SDO1: Timer synchrpnous output 1	A17: Address output (bp17)
P72	SDO2	A17	in/out	P7DIR2	P7PLU2	SDO2: Timer synchrpnous output 2	A18: Address output (bp18)
P73	SDO3	A18	in/out	P7DIR3	P7PLU3	SDO3: Timer synchrpnous output 3	A19: Address output (bp19)
P74	SDO4	NCS	in/out	P7DIR4	P7PLU4	SDO4: Timer synchrpnous output 4	NCS: Chip selection signal
P75	SDO5	NRE	in/out	P7DIR5	P7PLU5	SDO5: Timer synchrpnous output 5	NRE: Read enable signal
P76	SDO6	NWE	in/out	P7DIR6	P7PLU6	SDO6: Timer synchrpnous output 6	NWE: Write enable signal
P77	SDO7	NDK	in/out	P7DIR7	P7PLU7	SDO7: Timer synchrpnous output 7	NDK: Data acknowledge signal
P80	LED0	D0	in/out	P8DIR0	P8PLU0	LED0: LED driver pin 0	D0: Data I/O (bp0)
P81	LED1	D1	in/out	P8DIR1	P8PLU1	LED1: LED driver pin 1	D1: Data I/O (bp1)
P82	LED2	D2	in/out	P8DIR2	P8PLU2	LED2: LED driver pin 2	D2: Data I/O (bp2)
P83	LED3	D3	in/out	P8DIR3	P8PLU3	LED3: LED driver pin 3	D3: Data I/O (bp3)
P84	LED4	D4	in/out	P8DIR4	P8PLU4	LED4: LED driver pin 4	D4: Data I/O (bp4)
P85	LED5	D5	in/out	P8DIR5	P8PLU5	LED5: LED driver pin 5	D5: Data I/O (bp5)
P86	LED6	D6	in/out	P8DIR6	P8PLU6	LED6: LED driver pin 6	D6: Data I/O (bp6)
P87	LED7	D7	in/out	P8DIR7	P8PLU7	LED7: LED driver pin 7	D7: Data I/O (bp7)
P90	SBO0B	TXD0B	in/out	P9DIR0	P9PLU0	SBO0B: Serial 0 transmission data output	TXD0B: UART 0 transmission data output
P91	SBI0B	RXD0B	in/out	P9DIR1	P9PLU1	SBI0B: Serial 0 reception data input	RXD0B: UART 0 reception data input
P92	SBT0B		in/out	P9DIR2	P9PLU2	SBT0B: Serial 0 clock input / output	
P93	SBO3B	SDA3B	in/out	P9DIR3	P9PLU3	SBO3B: Serial 3 transmission data output	SDA3B: IIC3 data input / output
P94	SBI3B		in/out	P9DIR4	P9PLU4	SBI3B: Serial 3 reception data input	
P95	SBT3B	SCL3B	in/out	P9DIR5	P9PLU5	SBT3B: Serial 3 clock input / output	SCL3B: IIC3 clock input / output
PA0	AN0		in/out	PADIR0	PAPLU0	AN0: Analog 0 input	
PA1	AN1		in/out	PADIR1	PAPLU1	AN1: Analog 1 input	
PA2	AN2		in/out	PADIR2	PAPLU2	AN2: Analog 2 input	
PA3	AN3		in/out	PADIR3	PAPLU3	AN3: Analog 3 input	
PA4	AN4		in/out	PADIR4	PAPLU4	AN4: Analog 4 input	
PA5	AN5		in/out	PADIR5	PAPLU5	AN5: Analog 5 input	
PA6	AN6		in/out	PADIR6	PAPLU6	AN6: Analog 6 input	
PA7	AN7		in/out	PADIR7	PAPLU7	AN7: Analog 7 input	
PD0	IRQ2B		in/out	PDDIR0	PDPLU0	IRQ2B: External interrupt input 2	
PD1	IRQ3B		in/out	PDDIR1	PDPLU1	IRQ3B: External interrupt input 3	
PD2	TM4IOB		in/out	PDDIR2	PDPLU2	TM4IOB: Timer 4 input / output	
PD3	TM5IOB		in/out	PDDIR3	PDPLU3	TM5IOB: Timer 5 input / output	
PD4	TM7IOB		in/out	PDDIR4	PDPLU4	TM7IOB: Timer 7 input / output	
PD5	BUZZER		in/out	PDDIR5	PDPLU5	BUZZER: Buzzer output	
PD6	SYSCLK		in/out	PDDIR6	PDPLU6	SYSCLK: System clock output	

1.3.3 Pin Functions

Table:1.3.2 Pin Functions

Name	NO.	I/O	Other Function	Function	Description
$V_{SS}1$ $V_{SS}2$ $V_{SS}3$ $V_{DD}1$ $V_{DD}2$ $V_{DD}3$	14 63 91 10 17 89	-		Power supply pins	Apply 3.0 V to 3.6 V to $V_{DD}1$,2, 3.0 V to 5.5 V to $V_{DD}3$ and 0 V to $V_{SS}1$, $V_{SS}2$ and $V_{SS}3$.
OSC1 OSC2	13 12	Input Output		Clock input pins Clock output pins	Connect these oscillation pins to ceramic or crystal ocsillators for high-frequency clock operation. If the clock is an external input, connect it to OSC1 and leave OSC2 open. The chip will not operate with an external clock when using either the STOP or SLOW modes.
XI XO	15 16	Input Output		Clock input pins Clock output pins	Connect these oscillation pins to crystal oscillators for low-frequency clock operation. If the clock is an external input, connect it to XI and leave XO open. the chip will not operate with an external clock when using the STOP mode. If these pins are not used, connect XI to V_{SS} and leave XO open.
NRST	19	Input	P27	Reset pins [Active low]	This pin resets the chip when power is turned on, is allocated as P27 and contains an internal pull-up resistor (Type. 100 kΩ). Setting this pin low initialize the internal state of the device. Thereafter, setting the input to high releases the reset. The hardware waits for the system clock to stabilize, then processes the reset interrupt. Also, if “0” is written to P27 and the reset is initiated by software, a low level will be output. The output has an n-channel open-drain configuration. If a capacitor is to be inserted between NRST and V_{SS}, it is recommended that a discharge diode be placed between NRST and V_{DD}.
P00 P01 P02 P03 P04 P05 P06	4 5 6 7 8 9 2	I/O	SBO0A, TXD0A SBI0A, RXD0A SBT0A SBO2, SDA2 SBI2 SBT2, SCL2 DA0	I/O port 0	7-bit COMS tri-state I/O port. Each bit can be set individually as either an input or output by the P0DIR register. A pull-up / pull-down resistor for each bit can be selected individually by the P0PLU register. At reset, the input mode is selected and pull-up resistors are disabled (high impedance output).
P10 P11 P12 P13 P14 P15 P16	20 21 22 23 24 25 26	I/O	TM0IO, RMOUT TM1IO TM2IO TM3IO TM4IOA TM5IOA TM7IOA	I/O port 1	7-bit COMS tri-state I/O port. Each bit can be set individually as either an input or output by the P1DIR register. A pull-up / pull-down resistor for each bit can be selected individually by the P1PLU register. At reset, the input mode is selected and pull-up resistors are disabled (high impedance output).
P20 P21 P22 P23 P24 P25	27 28 29 30 31 32	I/O	IRQ0 IRQ1 IRQ2A IRQ3A IRQ4 IRQ5	I/O port 2	6-bit COMS tri-state I/O port. Each bit can be set individually as either an input or output by the P2DIR register. A pull-up / pull-down resistor for each bit can be selected individually by the P2PLU register. At reset, the input mode is selected and pull-up resistors are disabled (high impedance output).
P27	19	Input	NRST	I/O port 2	Port P27 has an n-channel open-drain configuration. When “0” is written and the reset is initiated by software, a low level will be output. Pull-up resistors are built-in.
P30 P31 P32 P33 P34 P35	33 34 35 36 37 38	I/O	SBO1, TXD1 SBI1, RXD1 SBT1 SBO3A, SDA3A SBI3A SBT3A, SCL3A	I/O port 3	6-bit COMS tri-state I/O port. Each bit can be set individually as either an input or output by the P3DIR register. A pull-up / pull-down resistor for each bit can be selected individually by the P3PLU register. At reset, the input mode is selected and pull-up resistors are disabled (high impedance output).

Name	NO.	I/O	Other Function	Function	Description
P40 P41 P42 P43	72 73 74 75	I/O	SBO4, TXD4 SBI4, RXD4 SBT4	I/O port 4	4-bit COMS tri-state I/O port. Each bit can be set individually as either an input or output by the P4DIR register. A pull-up / pull-down resistor for each bit can be selected individually by the P4PLU register. A pull-up / pull-down resistor for each port can be selected individually by the SELUD register. (However, pull-up and pull-down resistors cannot be mixed.) At reset, the input mode is selected and pull-up resistors are disabled (high impedance output).
P50 P51 P52 P53 P54 P55 P56 P57	39 40 41 42 43 44 45 46	I/O	AN0 AN1 AN2 AN3 AN4 AN5 AN6 AN7	I/O port 5	8-bit COMS tri-state I/O port. Each bit can be set individually as either an input or output by the P5DIR register. A pull-up / pull-down resistor for each bit can be selected individually by the P5PLU register. At reset, the input mode is selected and pull-up resistors are disabled (high impedance output).
P60 P61 P62 P63 P64 P65 P66 P67	47 48 49 50 51 52 53 54	I/O	KEY0, A8 KEY1, A9 KEY2, A10 KEY3, A11 KEY4, A12 KEY5, A13 KEY6, A14 KEY7, A15	I/O port 6	8-bit COMS tri-state I/O port. Each bit can be set individually as either an input or output by the P6DIR register. A pull-up / pull-down resistor for each bit can be selected individually by the P6PLU register. At reset, the input mode is selected and pull-up resistors are disabled (high impedance output).
P70 P71 P72 P73 P74 P75 P76 P77	55 56 57 58 59 60 61 62	I/O	SDO0, A16 SDO0, A17 SDO0, A18 SDO0, A19 SDO0, NCS SDO0, NRE SDO0, NWE SDO0, NDK	I/O port 7	8-bit COMS tri-state I/O port. Each bit can be set individually as either an input or output by the P7DIR register. A pull-up / pull-down resistor for each port can be selected individually by the SELUD register. (However, pull-up and pull-down resistors cannot be mixed.) At reset, the input mode is selected and pull-up resistors are disabled (high impedance output).
P80 P81 P82 P83 P84 P85 P86 P87	64 65 66 67 68 69 70 71	I/O	LED0, D0 LED0, D1 LED0, D2 LED0, D3 LED0, D4 LED0, D5 LED0, D6 LED0, D7	I/O port 8	8-bit COMS tri-state I/O port. Each bit can be set individually as either an input or output by the P8DIR register. A pull-up / pull-down resistor for each bit can be selected individually by the P8PLU register. Direct LED drive is available at output. At reset, the input mode is selected and pull-up resistors are disabled (high impedance output).
P90 P91 P92 P93 P94 P95	76 77 78 79 80 81	I/O	SBO0B, TXD0B SBI0B, RXD0B SBT0B SBO3B, SDA3B SBI3B SBT3B, SCL3B	I/O port 9	6-bit COMS tri-state I/O port. Each bit can be set individually as either an input or output by the P9DIR register. A pull-up / pull-down resistor for each bit can be selected individually by the P9PLU register. At reset, the input mode is selected and pull-up resistors are disabled (high impedance output).
PA0 PA1 PA2 PA3 PA4 PA5 PA6 PA7	92 93 94 95 96 97 98 99	I/O	AN0 AN1 AN2 AN3 AN4 AN5 AN6 AN7	Input port A	8-bit COMS tri-state I/O port. Each bit can be set individually as either an input or output by the PADIR register. A pull-up / pull-down resistor for each bit can be selected individually by the PAPLU register. A pull-up / pull-down resistor for each port can be selected individually by the SELUD register. (However, pull-up and pull-down resistors cannot be mixed.) At reset, the input mode is selected and pull-up resistors are disabled (high impedance output).
PD0 PD1 PD2 PD3 PD4 PD5 PD6 PD7	82 83 84 85 86 87 88 90	I/O	IRQ2B IRQ3B TM4IOB TM5IOB TM7IOB BUZZER SYSLK	Input port D	8-bit COMS tri-state I/O port. Each bit can be set individually as either an input or output by the PDDIR register. A pull-up / pull-down resistor for each bit can be selected individually by the PDPLU register. At reset, the input mode is selected and pull-up resistors are disabled (high impedance output).

Name	NO.	I/O	Other Function	Function	Description
SBO0A SBO0B SBO1 SBO2 SBO3A SBO3B SBO4	4 76 33 7 36 79 72	I/O	P00, TXD0A, P90, TXD0B P30, TXD1 P03, SDA2 P33, SDA3A P93, SDA3B P40, TXD4	Serial interface transmission/ reception data I/O pins	Transmission data output pins for serial interface 0 to 4. The output configuration, either COMS push-pull or n-channel open-drain can be selected with the P0ODC, P3ODC, P4ODC and P9ODC registers. Pull-up and pull-down registers can be selected by the P0PLU, P3PLU, P4PLU and P9PLU registers. Select the output mode at the P0DIR, P3DIR, P4DIR and P9DIR registers and serial data output mode by serial mode register 1 (SC0MD1, SC1MD1, SC2MD1, SC3MD1, SC4MD1). These can be used as normal I/O pins when the serial interface is not used.
SBI0A SBI0B SBI1 SBI2 SBI3A SBI3B SBI4	5 77 34 8 37 80 73	Input	P01, RXD0A P91, RXD0B P31, RXD1 P04 P34 P94 P41, RXD4	Serial interface received data input pins	Received data output pins for serial interface 0 to 4. Pull-up and pull-down resistors can be selected by the P0PLU, P3PLU, P4PLU and P9PLUregisters. Select input mode by the P0DIR, P3DIR, P4DIR and P9DIR registers and serial output mode by the serial mode register 1 (SC0MD1, SC1MD1, SC2MD1, SC3MD1, SC4MD1). These can be used as normal I/O pins when the serial interface is not used.
SBT0A SBT0B SBT1 SBT2 SBT3A SBT3B SBT4	6 78 35 9 38 81 74	I/O	P02 P92 P32 P05, SCL2 P35, SCL3A P95, SCL3B P42	Serial interface clock I/O pins	Clock I/O pins for serial interface 0 to 4. The output configuration, either COMS push-pull or n-channel open-drain can be selected with the P0ODC, P3ODC, P4ODC and P9ODC registers. Pull-up and pull-down registers can be selected by the P0PLU, P3PLU, P4PLU and P9PLU registers. Select the output mode at the P0DIR, P3DIR, P4DIR and P9DIR registers and serial data output mode by serial mode register 1 (SC0MD1, SC1MD1, SC2MD1, SC3MD1, SC4MD1). These can be used as normal I/O pins when the serial interface is not used.
TXD0A TXD0B TXD1 TXD4	4 76 33 72	Output	P00, SBO0A P90, SBO0B P30, SBI1 P40, SBI4	UART transmis-sion data output pins	In the serial interface in UART mode, this pin is configured as the transmission data output pin. The output configuration, either COMS push-pull or n-channel open-drain can be selected with the P0ODC, P3ODC, P4ODC and P9ODC registers. Clock I/O can be selected by the P0PLU registers. Select the output mode with the P0DIR, P3DIR, P4DIR and P9DIR registers and serial data output mode by serial mode register 1 (SC0MD1, SC1MD1, SC4MD1). These can be used as normal I/O pins when the serial interface is not used.
RXD0A RXD0B RXD1 RXD4	5 77 34 73	Input	P91, SBI0A P34, SBI0B P04, SBI1 P41, SBI4	UART received data input pins	In the serial interface in UART mode, this pin is configured as the reception data output pin. Pull-up and pull-down resistors can be selected by the P0PLU, P3PLU, P4PLU and P9PLUregisters. Select the input mode with the P0DIR, P3DIR, P4DIR and P9DIR registers and serial input mode by serial mode register 1 (SC0MD1, SC1MD1, SC4MD1). These can be used as normal I/O pins when the serial interface is not used.
SDA2 SDA3A SDA3B	7 36 79	I/O	P03, SBO2 P33, SBO3A P93, SBO3B	IIC data I/O pins	In the serial interface in IIC mode, this pin is configured as the data output pin. The output configuration, n-channel open-drain can be selected and select pull-up resistor with the P0DC, P3DC, and P9DC register. Pull-up and pull-down resistors can be selected by the P0PLU and P3PLU registers. Select output mode with the P0DIR, P3DIR, and P9DIR register, and serial data I/O at the serial mode register 1 (SC2MD1, SC3MD1). These can be used as normal I/O pins when the serial interface is not used.

Name	NO.	I/O	Other Function	Function	Description
SCL2 SCL3A SCL3B	9 38 81	Output	P05, SBT2 P35, SBT3A P95, SBT3B	IIC clock output pins	In the serial interface in IIC mode, this pin is configured as the clock output pin. The output configuration, n-channel open-drain can be selected and select pull-up resistor with the P0DC, P3DC, and P9DC register. Pull-up and pull-down resistors can be selected by the P0PLU, P3PLU, and P9PLU registers. Select output mode with the P0DIR, P3DIR, and P9DIR register, and serial data I/O at the serial mode register 1 (SC2MD1, SC3MD1). These can be used as normal I/O pins when the serial interface is not used.
TM0IO TM1IO TM2IO TM3IO TM4IOA TM4IOB TM5IOA TM5IOB	20 21 22 23 24 84 25 85	I/O	P10, RMOUT P11 P12 P13 P14 PD2 P15 PD3	Timer I/O pins	Event counter clock input pin, timer output and PWM signal output pin for 8-bit timer 0 to 5. To use this pin as event clock input, configure this as input by the P1DIR and PDDIR register. In the input mode, pull-up / pull-down resistors can be selected by the P1PLU and PDPLU register. For timer output, PWM signal output, select the special function pin by the port 1 output mode register (P1OMD) and the port D output mode register (PDOMD), and set to the output mode at the P1DIE register. These can be used as normal I/O pins when the serial interface is not used.
RMOUT	20	I/O	P10, TM0IO	Remote control transmission signal output pins	Output pin for remote control transmission signal with a carrier signal. For remote control carrier output, select the special function pin by the port 1 output mode register (P1OMD) and set to the output mode by the P1DIR register. Select the remote control carrier output with the remote control carrier output control register (RMCTR) at the same time. These can be used as normal I/O pins when the serial interface is not used.
BUZZER	87	I/O	PD5	Buzzer output	Piezoelectric buzzer driver pin. The driving frequency can be selected by the DLYCTR register. Select output mode with the PDDIR regieter and buzzer output with the DLYCTR register. These can be used as normal I/O pins when not used as buzzer output pin.
TM7IOA TM7IOB	26 86	I/O	P16 PD4	Timer I/O pins	Event counter clock input pin, timer output and PWM signal output pin for 16-bit timer 7. To use this pin as event clock input, configure this as input by the P1DIR and PDDIRregister. In the input mode, pull-up / pull-down resistors can be selected by the P1PLU and PDPLU register. For timer output, PWM signal output, select the special function pin by the port 1 output mode register (P1OMD) and the port D output mode register (PDOMD), and set to the output mode at the P1DIR and PDDIRregister. These can be used as normal I/O pins when not used as timer I/O pins.
SDO0 SDO1 SDO2 SDO3 SDO4 SDO5 SDO6 SDO7	55 56 57 58 59 60 61 62	Output	P70, A16 P71, A17 P72, A18 P73, A19 P74, NCS P75, NRE P76, NWE P77, NDK	Synchronous output pins	8-bit synchronous output pins. Synchronous output for each bit can be selected individually by the port 7 synchronous output control register (P7SYO). Set to the output mode by the P7DIR register. When not used for synchronous output, these pins can be used as a normal I/O pins.
V_{REF+}	100	-		+ power supply for A/D converter	Reference power supply pins for the A/D converter. Normally, the values of $V_{REF+} = V_{DD3}$ is used.

Name	NO.	I/O	Other Function	Function	Description
AN0 AN1 AN2 AN3 AN4 AN5 AN6 AN7	92 93 94 95 96 97 98 99	Input	PA0 PA1 PA2 PA3 PA4 PA5 PA6 PA7	Analog input pins	Analog input pins for an 8-channel, 10-bit A/D converter. When not used for analog input, these pins can be used as normal input pins.
DA_{VDD} DA_{VSS}	1 3		D/A converter+power D/A converter-power		Reference power supply voltage pin for D/A converter. Normally used as; $DA_{VDD}=V_{DD1, 2,}$ $DA_{VSS}=V_{SS.}$
DA0	2	Output	P06	Analog output pin	Analog input pins for an 1-channel, 8-bit A/D converter. When not used for analog input, these pins can be used as normal input pins.
IRQ0 IRQ1 IRQ2A IRQ2B IRQ3A IRQ3B IRQ4 IRQ5	27 28 29 82 30 83 31 32	Input	P20 P21 P22 PD0 P23 PD1 P24 P25	External interrupt input pins	External interrupt input pins. The valid edge for IRQ0 to 5 can be selected with the IRQnICR register. IRQ2, 3 and 5 can be set at both edges at pin voltage level. When not used for interrupts, these can be used as normal input pins.
KEY0 KEY1 KEY2 KEY3 KEY4 KEY5 KEY6 KEY7	47 48 49 50 51 52 53 54	Input	P60, A8 P61, A9 P62, A10 P63, A11 P64, A12 P65, A13 P66, A14 P67, A15	Key interrupt input pins	Key interrupt pins activated on input ORed condition. These can be set to key input pins by 2-bit with the key interrupt control register (KEYT3_1IMD). When not used for KEY input, these pins can be used as a normal I/O pins.
LED0 LED1 LED2 LED3 LED4 LED5 LED6 LED7	64 65 66 67 68 69 70 71	I/O	P80, D0 P81, D1 P82, D2 P83, D3 P84, D4 P85, D5 P86, D6 P87, D7	LED drive pins	Large current output pins. When not used for LED output, these pins can be used as a normal I/O pins.
MMOD	11	Input		Memory mode switch pin	These pins sets memory expansion mode. When used in processor mode, input “H”, and input “L” in other use. Do not change the setup after reset release.
MOD1	18	Input			Set always to “H”.

Name	NO.	I/O	Other Function	Function	Description
NWE	61	Output	P61, SDO6	Write enable pins [Active low]	Memory control signal used when the memory area is expanded to the external. NWE is the strove signal output for the write operation of the external memory and NRE is the strove signal output for the read operation of the external memory NCS is the tip selection signal outputs the external memory at the access. NDK is the aknowledge signal that indicates end of access to the external memory. SYSCLK is the internal system clock of this microcontroller and used as reference signal to external control systems, as well. A0-A19 is the address signal to the external memory, D0-D7 is the data I/O signal to the external memory.
NRE	60	Output	P75, SDO5	Read enable pins [Active low]	
NCS	59	Ouput	P74, SDO4	Tip select pins [Active low]	
NDK	62	Input	P77, SDO7	Data aknowledge pins [Active low]	
SYSCLK	88	Output	PD6	System clock pin	
A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10 A11 A12 A13 A14 A15 A16 A17 A18 A19	39 40 41 42 43 44 45 46 47 48 49 50 51 52 53 54 55 56 57 58	Output Output Output Output Output Output Output Output Output Output Output Output Output Output Output Output Output Output Output Output	P50 P51 P52 P53 P54 P55 P56 P57 P60, KEY0 P61, KEY1 P62, KEY2 P63, KEY3 P64, KEY4 P65, KEY5 P66, KEY6 P67, KEY7 P70, SDO0 P71, SDO1 P72, SDO2 P73, SDO3	Address pins	
D0 D1 D2 D3 D4 D5 D6 D7	64 65 66 67 68 69 70 71	I/O I/O I/O I/O I/O I/O I/O I/O	P80, LED0 P81, LED1 P82, LED2 P83, LED3 P84, LED4 P85, LED5 P86, LED6 P87, LED7	Data pins	

1.4 Block Diagram

1.4.1 Block Diagram

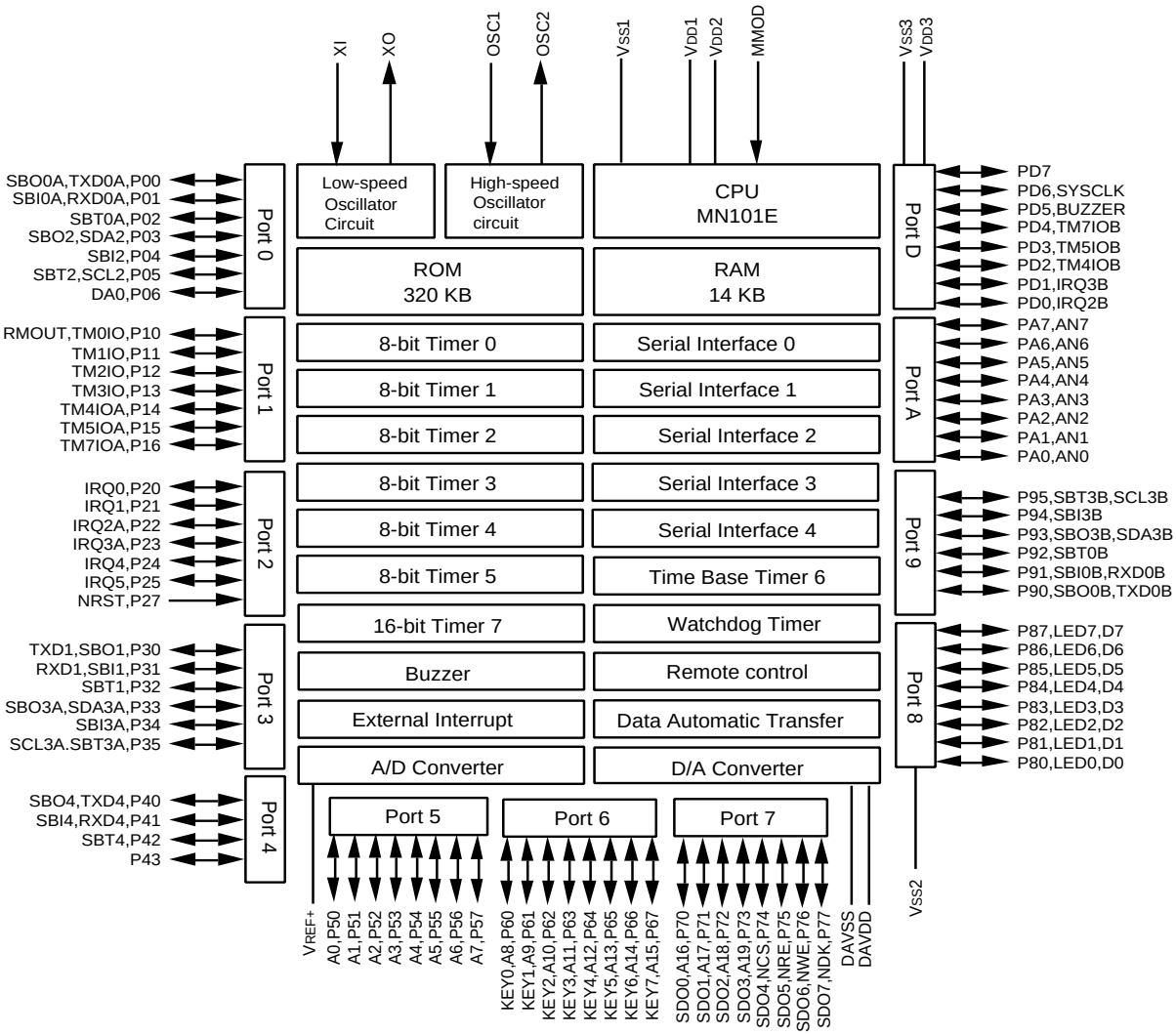


Figure:1.4.1 Block Diagram

* Depending on the models. [See 1-1-1 Product Summary]

1.5 Electrical Characteristics

This LSI manual describes the standard specification.

Machine cycle (system clock fs) is described based on the standard mode:1/2 of high oscillation at NORMAL mode, or on the clock frequency:1/2 of low oscillation at SLOW mode. Please ask our sales offices for the product specifications.

Contents	Structure	CMOS integrated circuit
	Application	General purpose
	Function	CMOS, 8-bit, single chip micro controller

1.5.1 Absolute Maximum Ratings

Parameter			Symbol	Rating	Unit
1	Power supply voltage		$V_{DD1,2}$	-0.3 to +4.6	V
2			V_{DD3}	-0.3 to +7.0	
3	Input pin voltage		V_{I1}	-0.3 to $V_{DD1,2}$ + 0.3	V
4	I/O pin voltage		V_{O1}	-0.3 to $V_{DD1,2}$ + 0.3	
5			V_{IO2}	-0.3 to V_{DD3} + 0.3	
6	Peak output current	P8	I_{OL1} (peak)	40	mA
7		Other than P8	I_{OL2} (peak)	20	
8			I_{OLH} (peak)	-10	
9	Average output current *1	P8	I_{OL1} (avg)	30	
10		Other than P8	I_{OL2} (avg)	15	
11			I_{OH} (avg)	-5	
12	Power dissipation		P_D	400	mW
13	Operation ambient temperature		T_{opr}	-40 to +85	°C
14	Storage temperature		Tstg	-55 to +125	

*1 Applied to any 100-ms period.

*2 Connect at least one bypass capacitor of 0.1 μF or larger between the power supply pin and the ground for latch-up prevention.

*3 The absolute maximum ratings are the tolerance for the LSI to be operated properly.

1.5.2 Operating Conditions

Ta=-40 °C to 85 °C $V_{DD1}=V_{DD2}$=3.0 V to 3.6 V, $V_{DD3}=V_{DD1}$ to 5.5 V, $V_{SS1}=V_{SS2}=V_{SS3}$=0 V

Parameter		Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
Power supply voltage *4							
1	Power supply voltage $V_{DD1}=V_{DD2}$	V_{DD1-1}	4.00 MHz < fosc ≤ 32.0 MHz [Normal mode:fs=fosc/2]	3.0	-	3.6	V
2		V_{DD1-2}	4.00 MHz < fosc ≤ 10.0 MHz [Normal mode:fs=fosc]	3.0	-	3.6	
3		V_{DD1-3}	fx=32.768 kHz	3.0	-	3.6	
4	Power supply voltage V_{DD3}	V_{DD3-1}	4.00 MHz < fosc ≤ 32.0 MHz [Normal mode:fs=fosc/2]	V_{DD1}	-	5.5	
5		V_{DD3-2}	4.00 MHz < fosc ≤ 32.0 MHz [Normal mode:fs=fosc/2]	V_{DD1}	-	5.5	
6		V_{DD3-3}	fx=32.768 kHz	V_{DD1}	-	5.5	
7	Voltage to maintain RAM data $V_{DD1}=V_{DD2}$	V_{DD1-4}	At STOP mode	1.8	-	3.6	
8	Voltage to maintain RAM data V_{DD3}	V_{DD3-4}	At STOP mode	V_{DD1}	-	3.6	
Operation speed *5							
9	Instruction execution time	t_{c1}	V_{DD1}=3.0 to 3.6 V [Normal mode:fs=fosc/2]	0.0625	-	-	µs
10		t_{c2}	V_{DD}=3.0 to 3.6 V [Double-speed mode:fs=fosc]	0.100	-	-	
11		t_{c3}	V_{DD}=3.0 to 3.6 V [fs=fx/2]	61.0	-	-	
High speed oscillator 1 Fig. 1-5-1							
12	Crystal frequency	f_{xtal1}	V_{DD}=3.0 to 3.6 V	4.0	-	32.0	MHz
13	External capacitors *6	C_{11}		-	15	-	pF
14		C_{12}		-	15	-	
15	Internal feedback resistor	R_{f10}		-	1.0	-	MΩ

*4 fosc: Input clock frequency to OSC1
fx Input clock frequency to XI

*5 t_{c1}, t_{c2} OSC1 is the CPU clock.
t_{c3} XI is the CPU clock.

*6 Connect external capacitors that suits the used pin. When crystal oscillator or ceramic oscillator is used, the frequency is changed depending on the condenser rate. Therefore, consult the manufacturer of the pin for the appropriate external capacitor.

Ta=-40 °C to 85 °C $V_{DD1}=V_{DD2}=3.0$ V to 3.6 V, $V_{DD3}=V_{DD1}$ to 5.5 V, $V_{SS1}=V_{SS2}=V_{SS3}=0$ V

Parameter		Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
Low speed oscillator 1 Fig. 1-5-2							
16	Crystal frequency	f_{xtal2}	V_{DD}=3.0 to 3.6 V	32	-	100	MHz
17	External capacitors *7	C_{21}		-	22	-	pF
18		C_{22}		-	22	-	
19	Internal feedback resistor	R_{f20}		-	7.0	-	MΩ
External clock input 1 OSC1 (OSC2 is unconnected)							
20	Clock frequency	f_{OSC}		4.0	-	32.0	MHz
21	High level pulse width *8	t_{wh1}	Fig. 1-5-3	11.625	-	-	ns
22	Low level pulse width *8	t_{wl1}		11.625	-	-	
23	Rising time	t_{wr1}	Fig. 1-5-3	-	-	5.0	
24	Falling time	t_{wf1}		-	-	5.0	
External clock input 2 XI (XO is unconnected)							
25	Clock frequency	fx		32	-	100	kHz
26	High level pulse width *8	t_{wh2}	Fig. 1-5-4	3.5	-	-	µs
27	Low level pulse width *8	t_{wl2}		3.5	-	-	
28	Rising time	t_{wr2}	Fig. 1-5-4	-	-	20	ns
29	Falling time	t_{wf2}		-	-	20	

*7 Connect external capacitors that suits the used pin. When crystal oscillator or ceramic oscillator is used, the frequency is changed depending on the condenser rate. Therefore, consult the manufacturer of the pin for the appropriate external capacitor.

*8 *8 Clock duty rate should be 45% to 55%.

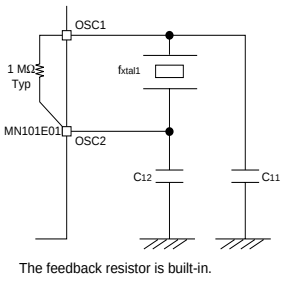


Figure:1.5.1 HIgh speed oscillator

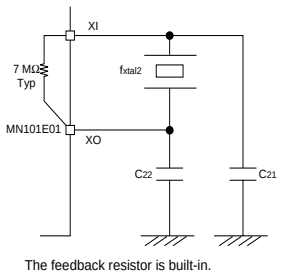


Figure:1.5.2 Low speed oscillator

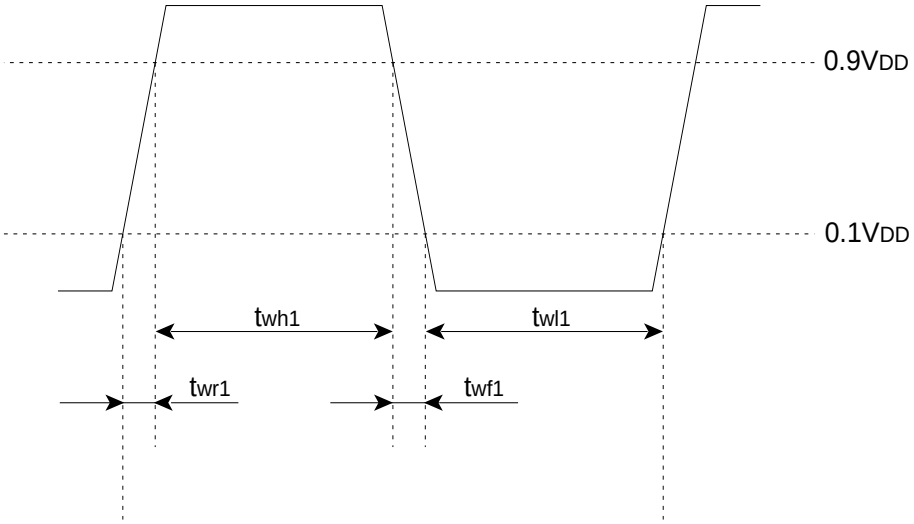


Figure:1.5.3 OSC1 Timing Chart

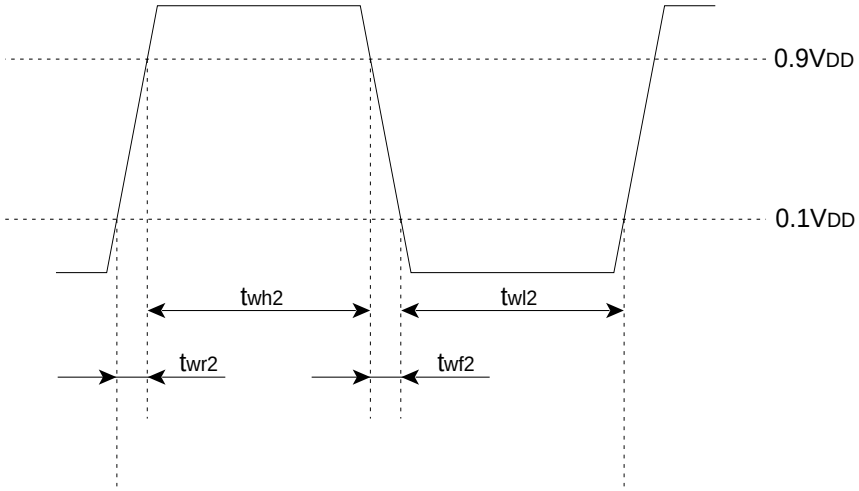


Figure:1.5.4 XI Timing Chart

1.5.3 DC Characteristics

Ta=-40 °C to 85 °C V_{DD1}=V_{DD2}=3.0 V to 3.6 V, V_{DD3}=V_{DD1} to 5.5 V, V_{SS1}=V_{SS2}=V_{SS3}=0 V

Parameter		Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
Power supply current *9							
1	Power supply current	I_{DD1}	fosc=32.0 MHz V_{DD1}=3.3 V [fs=fosc/2]	-	11 (48)*10	30 (80)	mA
2		I_{DD2}	fosc=20.0 MHz V_{DD1}=3.3 V [fs=fosc/2]	-	8 (43)	22 (75)	
3		I_{DD3}	fx=32.768 kHz V_{DD1}=3.3 V [fs=fx/2]	-	30 (60)	120 (180)	µA
4	Supply current during HALT1 mode	I_{DD4}	fx=32.768 kHz V_{DD1}=3.3 V	-	12	30	
5	Supply current during STOP mode	I_{DD5}	V_{DD1}=3.3 V Ta=25 °C	-	0.3	3.0	
6		I_{DD6}	V_{DD1}=3.3 V Ta=+85 °C	-	-	80	

*9 Measured under conditions without load.

- The supply current during operation, I_{DD1}, I_{DD2} are measured under the following conditions:
  After all I/O pins are set to input mode and the oscillation is set to <NORMAL mode>, the MMOD pin is at V_{SS} level, the input pins are at V_{DD} level, and a 32 MHz (20 MHz) square wave of V_{DD} and V_{SS} amplitudes is input to the OSC1 pin.
- The supply current during operation, I_{DD3}, is measured under the following conditions:
  After all I/O pins are set to input mode and the oscillation is set to <SLOW mode>, the MMOD pin is at V_{SS} level, the input pins are at V_{DD} level, and a 32.768 kHz square wave of V_{DD} and V_{SS} amplitudes is input to the XI pin.
- The supply current during HALT1 mode, I_{DD4} are measured under the following conditions:
  After all I/O pins are set to input mode and the oscillation is set to <HALT mode>, the MMOD pin is at V_{SS} level, the input pins are at V_{DD} level, and an 32.768 kHz square wave of V_{DD} and V_{SS} amplitudes is input to the XI pin.
- The supply current during STOP mode, I_{DD5}, I_{DD6} is measured under the following conditions:
  After the oscillation is set to <STOP mode>, the MMOD pin is at V_{SS} level, the input pins are at V_{DD} level, and the OSC1 and XI pins are unconnected.

*10
- ( ) is for Flash version

Ta=-40 °C to 85 °C V_{DD1}=V_{DD2}=3.0 V to 3.6 V, V_{DD3}=V_{DD1} to 5.5 V, V_{SS1}=V_{SS2}=V_{SS3}=0 V

Parameter		Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
Input pin MMOD, MOD1							
6	Input high voltage 1	V_{IH1}		0.8 V_{DD1}	-	V_{DD1}	V
7	Input low voltage 1	V_{IL1}		0	-	0.2 V_{DD1}	
8	Input leakage current	I_{LK1}	V_{IN}=0 V to V_{DD1}	-	-	± 2.0	μA
I/O pin P00 to P06, P10 to P16, P20 to P25, P30 to P35, P50 to P57, P60 to P67 (Schmitt trigger input)							
9	Input high voltage	V_{IH2}		0.8 V_{DD1}	-	V_{DD1}	V
10	Input low voltage	V_{IL2}		0	-	0.2 V_{DD1}	
11	Input leakage current	I_{LK2}	V_{IN}=0 V to V_{DD1}	-	-	± 2.0	μA
12	Pull-up resistor	R_{PU2}	V_{DD1}=3.3 V V_{IN}=V_{SS1}	30	100	350	kΩ
13	Output high voltage	V_{OH2}	V_{DD1}=3.3 V I_{OH}=-2.0 mA	2.4	-	-	V
14	Output low voltage	V_{OL2}	V_{DD1}=3.3 V I_{OL}=2.0 mA	-	-	0.4	
I/O pin P70 to P77 (Schmitt trigger input)							
15	Input high voltage	V_{IH3}		0.8 V_{DD1}	-	V_{DD1}	V
16	Input low voltage	V_{IL3}		0	-	0.2 V_{DD1}	
17	Input leakage current	I_{LK3}	V_{IN}=0 V to V_{DD1}	-	-	± 2.0	μA
18	Pull-up resistor	R_{PU3}	V_{DD1}=3.3 V V_{IN}=V_{SS1}	30	100	350	kΩ
19	Pull-down resistor	R_{DW3}	V_{DD1}=3.3 V V_{IN}=V_{SS1}	30	100	350	
20	Output high voltage	V_{OH3}	V_{DD1}=3.0 V I_{OH}=-2.0 mA	2.4	-	-	V
21	Output low voltage	V_{OL3}	V_{DD1}=3.0 V I_{OL}=2.0 mA	-	-	0.4	
I/O pin 3 P90 to P95, PD0 to PD7 (Schmitt trigger input)							
22	Input high voltage	V_{IH4}		0.8 V_{DD3}	-	V_{DD3}	V
23	Input low voltage	V_{IL4}		0	-	0.2 V_{DD3}	
24	Input leakage current	I_{LK4}	V_{IN}=0 V to V_{DD3}	-	-	± 2.0	μA
25	Pull-up resistor	R_{PU4}	V_{DD3}=5.0 V I_{IN}=1.5 V	10	30	120	kΩ
26	Output high voltage	V_{OH4}	V_{DD3}=5.0 V I_{OH}=-0.5 mA	4.5	-	-	V
27	Output low voltage	V_{OL4}	V_{DD3}=5.0 V I_{OL}=1.0 mA	-	-	0.5	
I/O pin 4 (V_{DD3}=3.0 V to 5.5 V) P40 to P43, PA0 to PA7 (Schmitt trigger input)							
28	Input high voltage	V_{IH5}		0.8 V_{DD3}	-	V_{DD3}	V
29	Input low voltage	V_{IL5}		0	-	0.2 V_{DD3}	
30	Input leakage current	I_{LK5}	V_I=0 V to V_{DD3}	-	-	± 2.0	μA
31	Pull-up resistor	R_{PU5}	V_{DD3}=5.0 V $_{IN}$=1.5	10	30	120	kΩ
32	Pull-down resistor	R_{DW5}	V_{DD3}=5.0 V $_{IN}$=3.5	10	30	120	
33	Output high voltage	V_{OH5}	V_{DD3}=5.0 V I_{OH}=-0.5 mA	4.5	-	-	V
34	Output low voltage	V_{OL5}	V_{DD3}=5.0 V I_{OL}=1.0 mA	-	-	0.5	
I/O pin 5 P80 to P87 (Schmitt trigger input)							
35	Input high voltage	V_{IH6}		0.8 V_{DD3}	-	V_{DD3}	V
36	Input low voltage	V_{IL6}		0	-	0.2 V_{DD3}	

Parameter		Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
37	Input leakage current	I_{LK6}	V_{IN}=0 V to V_{DD3}	-	-	± 2.0	μA
38	Pull-up resistor	R_{PU6}	V_{DD3}=5.0 V $_{IN}$=1.5	10	30	120	kΩ
39	Output high voltage	V_{OH6}	V_{DD3}=5.0 V I_{OH}=-0.5 mA	4.5	-	-	V
40	Output low voltage	V_{OL6}	V_{DD3}=5.0 V I_{OL}=15.0 mA	-	-	1.0	
I/O pin 7 P27 (NRST) (Schmitt trigger input)							
41	Input high voltage	V_{IH7}		0.8 V_{DD1}	-	V_{DD1}	V
42	Input low voltage	V_{IL7}		0	-	0.15 V_{DD1}	
43	Pull-up resistor	R_{PU7}	V_{DD1}=3.3 V V_{IN}=V_{SS1}	30	100	350	kΩ

1.5.4 A/D Converter Characteristics

Ta=-40 °C to 85 °C $V_{DD1}=V_{DD2}=3.0$ V to 3.6 V, $V_{DD3}=V_{DD1}$ to 5.5 V, $V_{SS1}=V_{SS2}=V_{SS3}=0$ V

Parameter		Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
1	Resolution			-	-	10	Bits
2	Non-linearity error	NLE	V_{DD3}=5.0 V V_{SS1}=0 V V_{REF+}=5.0 V T_{AD}=500 ns	-	-	± 3	LSB
3	Differential non-linearity error	DNLE		-	-	± 3	
4	Zero transition voltage		V_{DD3}=5.0 V V_{SS1}=0 V V_{REF+}=5.0 V T_{AD}=500 ns	-	30	100	mV
5	Full-scale transition voltage			4900	4970		
6	A/D conversion time		T_{AD}=500 ns	8.10	-	-	µs
7			T_{AD}=15.26 µs	-	-	488.41	
8	Sampling time		T_{AD}=500 ns	1.0	-	9.0	
9			T_{AD}=15.26 µs	30.52	-	274.68	
10	Reference voltage	V_{REF+}		V_{DD1}	-	V_{DD3}	V
11	Analog input voltage			V_{SS1}	-	V_{REF+}	
12	Analog input leakage current		When channel is OFF V_{ADIN}=0 V to 5 V	-	-	± 2	µA
13	Reference voltage pin input leakage current		When V_{REF+} is OFF $V_{SS3} \leq V_{REF+} \leq V_{DD3}$	-	-	± 2.0	
14	Ladder resistance	R_{LADD}	$V_{SS3}=V_{REF+}$=5.0 V V_{SS}=0 V	15	35	50	kΩ

The values of 2 to 5 are guaranteed in the condition that $V_{DD3}=V_{ref+}$=5.0 V.

1.5.5 D/A Converter Characteristics

Ta=-40 °C to 85 °C V_{DD1}=V_{DD2}=3.0 V to 3.6 V, V_{DD3}=V_{DD1} to 5.5 V, V_{SS1}=V_{SS2}=V_{SS3}=0 V

Parameter		Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
1	Resolution			-	-	8	Bits
2	Reference voltage low level	D_{AVSS}	DA_{VDD}=3.3 V, DA_{VSS}=0 V D7 to D0=ALL "L"	0	-	1.0	V
3	Reference voltage high level	D_{AVDD}		2.0	-	V_{DD1}	
4	Zero scale output voltage	V_{ZS}	DA_{VDD}=3.3 V, DA_{VSS}=0 V D7 to D0=ALL "H"	-0.05	0.0	0.05	
5	Full scale output voltage	V_{FS}		3.24	3.29	3.34	
6	Analog output resistance (Minimum reference resistance)	R_{OAT}		6	10	14	kΩ
7	Non-linearity error	N_{LE}	DA_{VDD}=3.3 V, DA_{VSS}=0 V	-	± 2.0	± 3.0	LSB
8	Differential Non-linearity error	D_{NLE}	DA_{VDD}=3.3 V, DA_{VSS}=0 V	-	± 2.0	± 3.0	
9	Settling time	T_{SET}	External capacitor CL=35 pF All bits are set to ON or OFF.	-	1.5	3.0	ms
10	Reference voltage pin input leakage current			-	-	± 2.0	μA

Ratings of items 1, 4 to 9 are guaranteed at V_{DD1}=D_{AVDD}=3.3 V, DA_{VSS}=0.0 V.

1.6 Package Dimension

Package code: *QFP100-P-1818B Units: mm

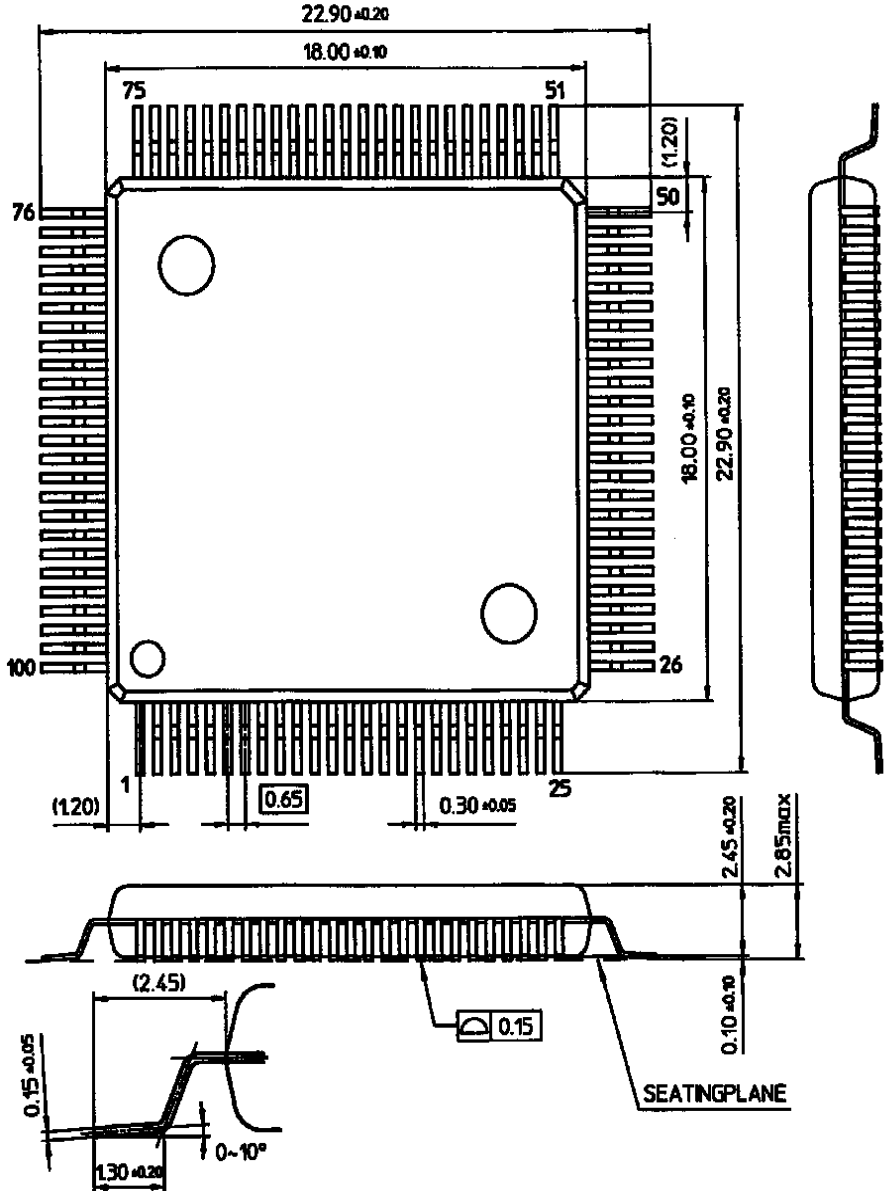


Figure:1.6.1 Package Dimension

The external dimensions of the package are subject to change. Before using this product, please obtain product specifications from the sales offices.

1.7 Cautions for Circuit Setup

1.7.1 General Usage

■ Connection of V_{DD} pin and V_{SS} pin

All of the VDD and VSS pins should be connected directly to the power source and ground in the external. Put them on printed circuit board after the location of LSI (package) pin is confirmed. Connection error may lead a fusion and breakdown of a micro controller.

■ Cautions for Operation

1. If you install the product close to high-field emissions (under the cathode ray tube, etc.), shield the package surface to ensure normal performance.
2. Operation temperature should be well considered. Each product has different condition. For example, if the operation temperature is over the condition, improper operation could be occurred.
3. Operation voltage should be also well considered. Each product has different operating range.
    - If the operation voltage is over the operating range, duration of the product could be shortened.
    - If the operation voltage is below the operating range, improper operation could be occurred.

1.7.2 Unused pins

■ Unused Pins (only for input)

Insert some 10 kΩ resistor to unused pins (only for input) for pull-up or pull-down.

If the input is unstable, Pch transistor and Nch transistor of input inverter are on, and through current goes to the input circuit. That increases current consumption and causes power supply noise.

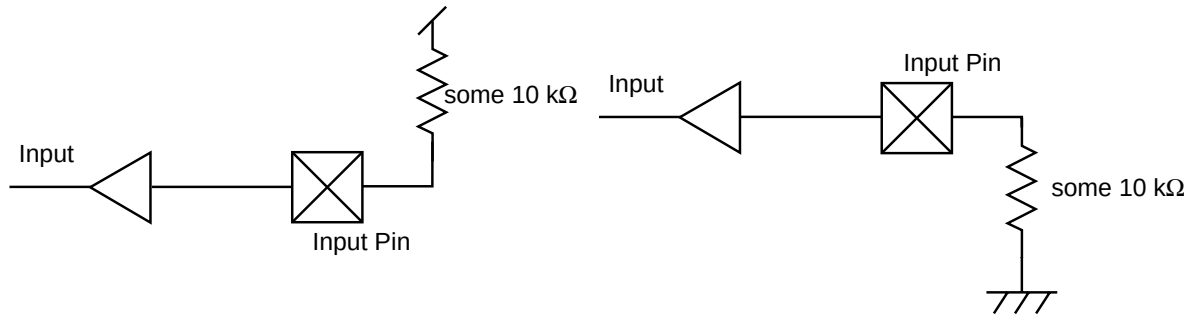
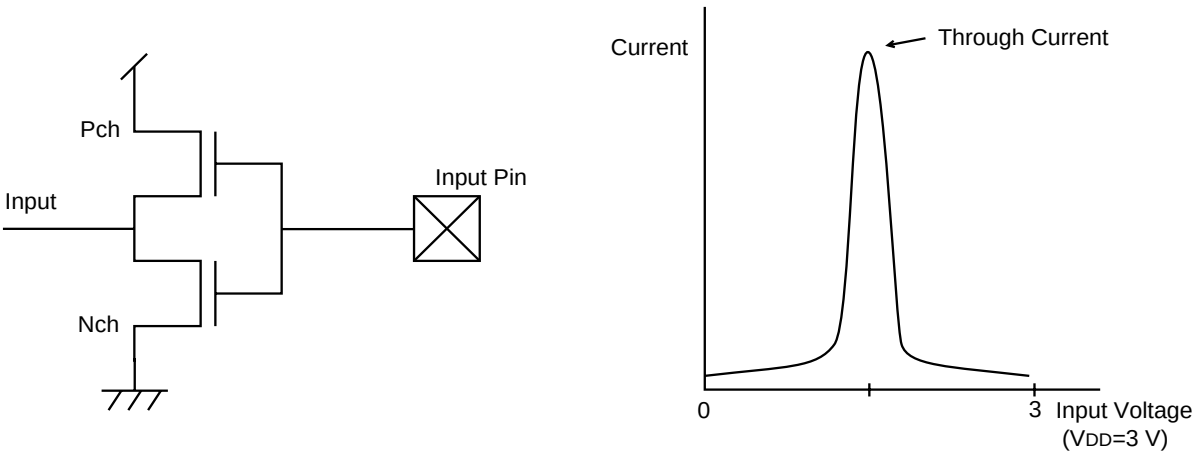


Figure:1.7.1 Unused Pins (only for input)



Input Inverter Organization

Input Inverter Characteristics

Figure:1.7.2 Input Inverter Organization and Characteristics

■ Unused Pins (for I/O)

Unused I/O pins should be set according to pins' condition at reset. If the output is high impedance (Pch / Nch transistor: output off) at reset, to stabilize input, set some 10 kΩ resistor to be pull-up or pull-down. If the output is on at reset, set them open. Pins used as both LCD and port pins should be set to open to be used as LCD output pins.

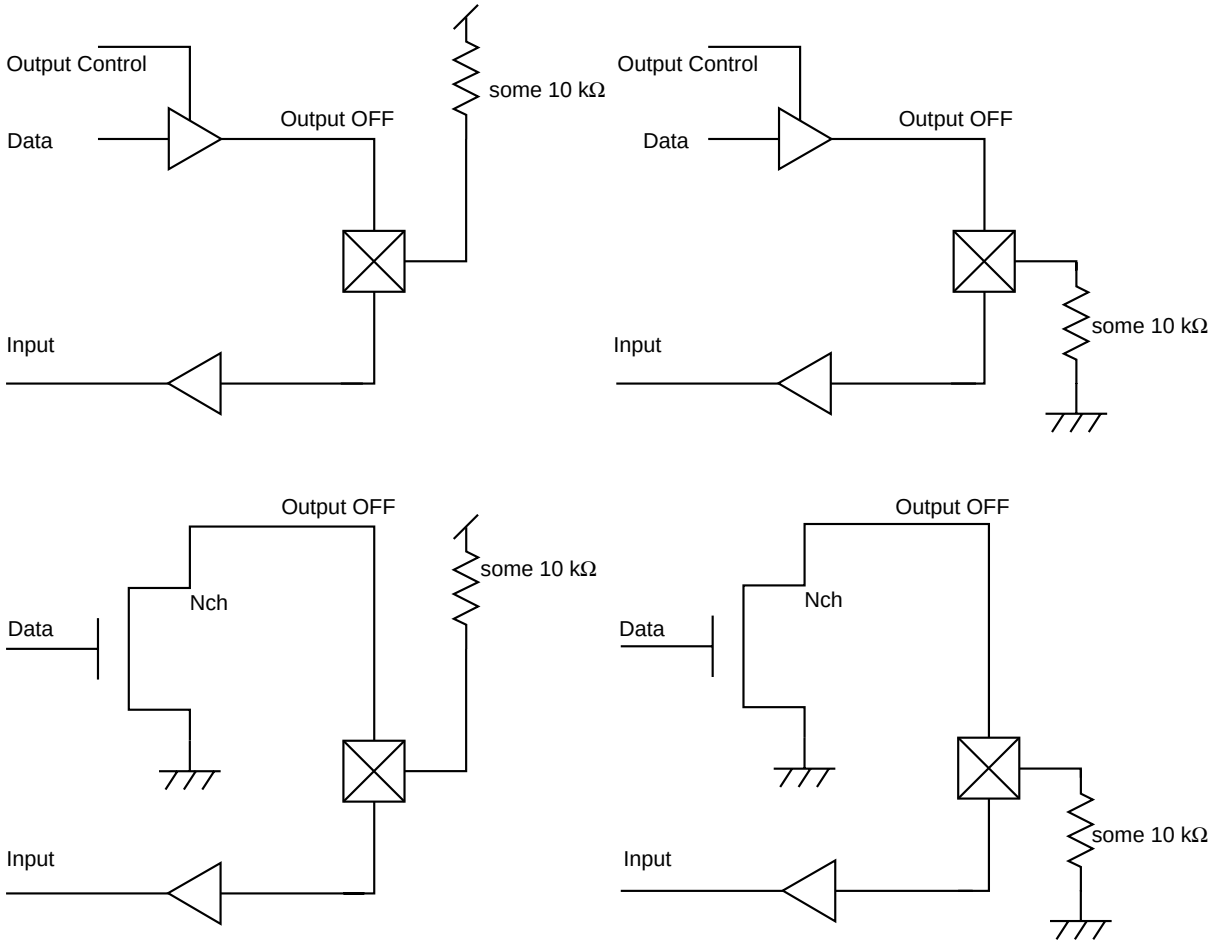


Figure:1.7.3 Unused I//O Pins (high impedance output at reset)

1.7.3 Power Supply

■ The Relation between Power Supply and Input Pin Voltage

Input pin voltage should be supplied only after power supply is on. If this order is reversed the destruction of micro controller by a large current flow could be occurred.

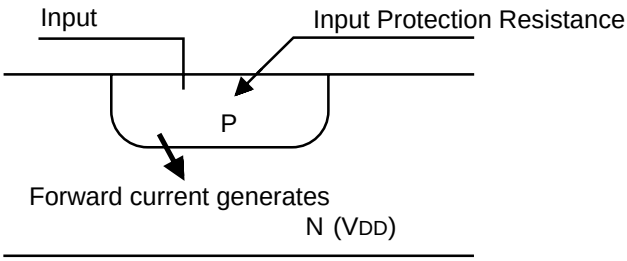


Figure:1.7.4 V_{DD} and Input Pin Voltage

■ The Relation between V_{DD} and Reset Input Voltage

After power supply is on, reset pin voltage should be low for sufficient time before rising, in order to be recognized as a reset signal.

[Refer to Chapter 2. 2.7.1 Reset Operation]

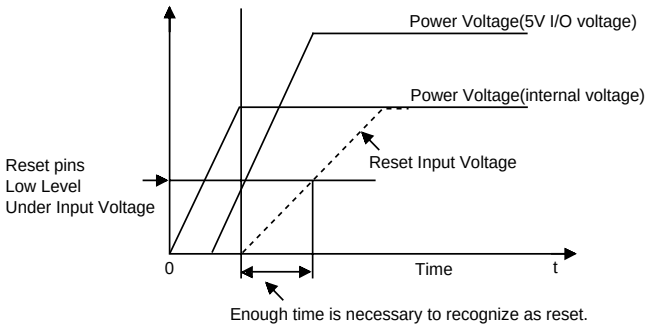


Figure:1.7.5 Power Supply and Reset Input Voltage

1.7.4 Power Supply Circuit

■ Cautions for Setting Circuit with V_{DD}

The MOS logic such a microcomputer is high speed and high density. So, the power circuit should be designed, taking into consideration of AC line noise, ripple caused by LED driver.

Figure:1.7.6 shows an example for a circuit with V_{DD} (Emitter follower type).

■ An Example for a Circuit with V_{DD} (Emitter follower type)

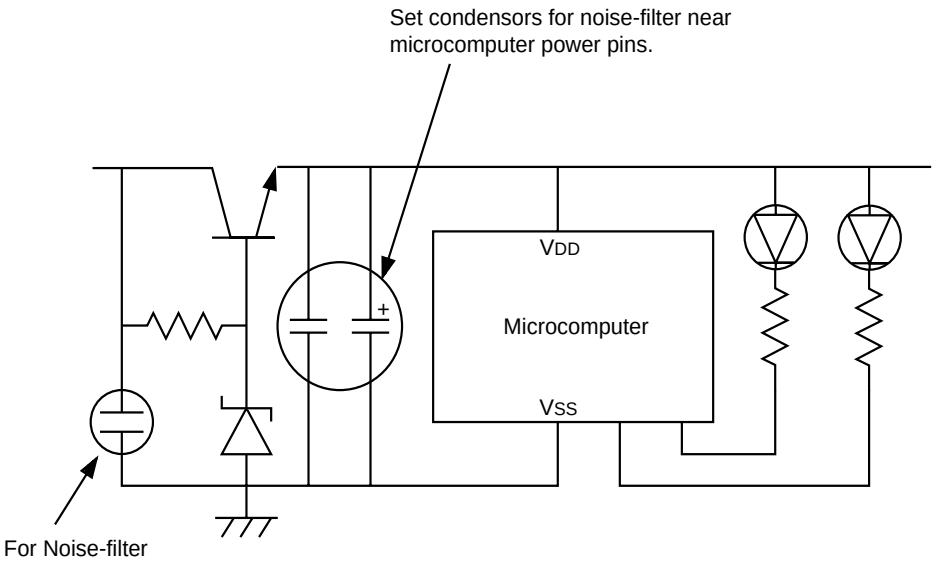


Figure:1.7.6 An Example for a Circuit of V_{DD} Supply (Emitter follower type)

Chapter 2 CPU Basics

2

2.1 Overview

The MN101E CPU has a flexible and optimized hardware configuration. It is a high speed CPU with a simple and efficient instruction set. Specific features are as follows:

1. Minimized code sizes with instruction lengths based on 4-bit increments:
   The series keeps code sizes down by adopting a basic instruction length of one byte and variable instruction lengths based on 4-bit increments.
2. Minimum execution instruction time is one system clock cycle. (62.5 ns)
3. Minimized register set that simplifies the architecture and supports C language :
   The instruction set has been determined, depending on the size and capacity of hardware, after on analysis of embedded application programing code and creation code by C language compiler. Therefore, the set is simple instruction using the minimal register set required for C language compiler.

Table:2.1.1 Basic Specifications

Structure	Load / store architecture	
	Six registers	Data : 8-bit x 4 Address : 16-bit x 2
	Others	PC : 21-bit PSW : 8-bit SP : 16-bit
Instructions	Number of instructions	39
	Addressing modes	9
	Instruction length	Basic portion : 1 byte (min.) Extended portion : 0.5-byte x n (0≤n≤9)
Basic performance	Internal operating frequency (max)	16 MHz
	Instruction execution	Min. 1 cycle
	Inter-register operation	Min. 2 cycle
	Load / store	Min. 2 cycle
	Conditional branch	2 to 3 cycles
Pipeline	3-stage (instruction fetch, decode, execution)	
Address space	1MB (max. 64 KB for data)	
	Instruction/data space	
External bus	Address	20-bit
	Data	8-bit
	Minimum bus cycle	1 system clock cycle
Interrupt	Vector interrupt	3 interrupt levels
Low-power consumption mode	STOP mode	
	HALT mode	

2.1.1 Block Diagram

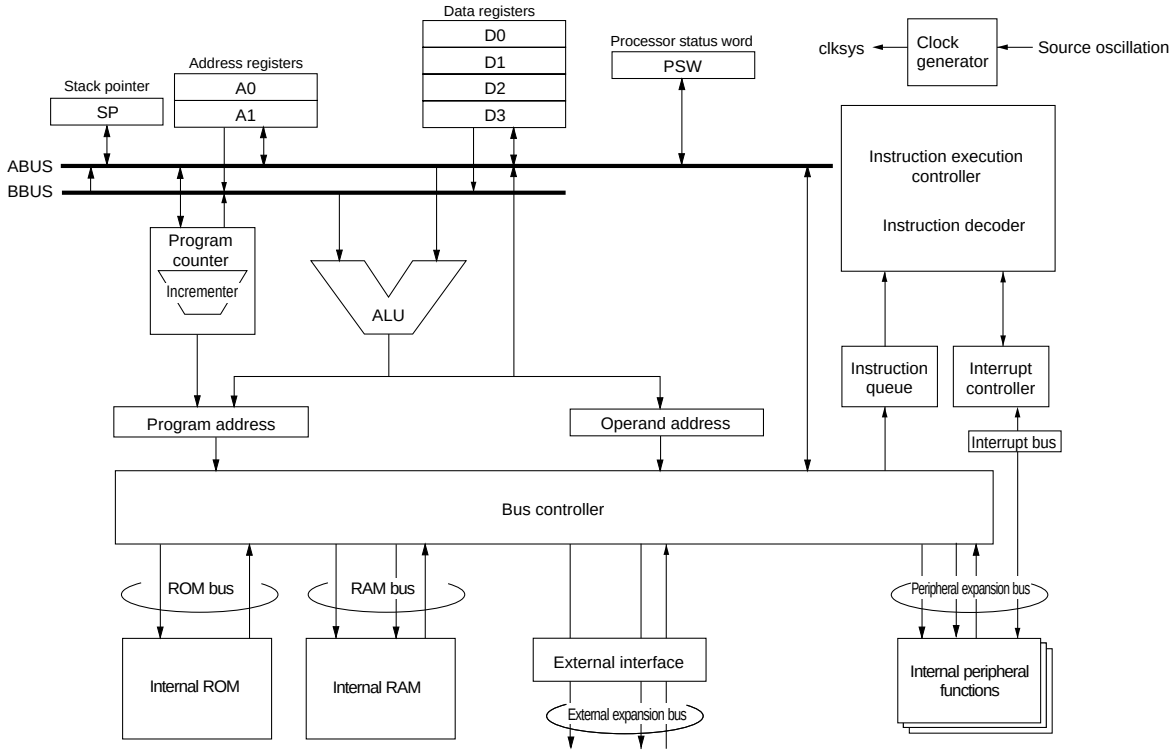


Figure:2.1.1 CPU Block Diagram

Table:2.1.2 Block Diagram and Function

Clock generator	Uses a clock oscillator circuit driven by an external crystal or ceramic resonator to supply clock signals to CPU blocks.
Program counter	Generates addresses for the instructions to be inserted into the instruction queue. Normally incremented by sequencer indication, but may be set to branch destination address or ALU operation result when branch instructions or interrupts occur.
Instruction queue	Stores up to 2 bytes of pre-fetched instructions.
Instruction decoder	Decodes the instruction queue, sequentially generates the control signals needed for instruction execution, and executes the instruction by controlling the blocks within the chip.
Instruction execution controller	Controls CPU block operations in response to the result decoded by the instruction decoder and interrupt requests.
ALU	Executes arithmetic operations, logic operations, shift operations, and calculates operand addresses for register relative indirect addressing mode.
Internal ROM, RAM	Assigned to the execution program, data and stack region.
Address register	Stores the addresses specifying memory for data transfer. Stores the base address for register relative indirect addressing mode.
Data register	Holds data for operations. Two 8-bit registers can be connected to form a 16-bit register.
Interrupt controller	Detects interrupt requests from peripheral functions and requests CPU shift to interrupt processing.
Bus controller	Controls connection of CPU internal bus and CPU external bus. Includes bus usage arbitration function.
Internal peripheral functions	Includes peripheral functions (timer, serial interface, A/D converter, D/A converter, etc.). Peripheral functions vary depending on the model.

2.1.2 CPU Control Registers

This LSI locates the peripheral circuit registers in memory space (0x03F00 to 0x03FFF) with memory mapped I/O. CPU control registers are also located in this memory space.

Table:2.1.3 CPU Control Registers

Registerss	Address	R/W	Function	Pages
CPUM	0x03F00	R/W *1	CPU mode control register	II-51
MEMCTR	0x03F01	R/W	Memory control register	II-38
Reserved	0x03F04	-	For test	-
RCCTR	0x03F09	R/W	ROM correction control register	II-30
SBNKR	0x03F0A	R/W	Bank register for source address	II-19
DBNKR	0x03F0B	R/W	Bank register for destination addres	II-20
Reserved	0x03F0F	-	(for test)	-
RCnAP	0x03FC0 to 0x03FC8	R/W	ROM correction address setting register	II-31 to 32
Reserved	0x03FE0	-	For debugger	-
NMICR	0x03FE1	R/W	Non - maskable interrupt control register	III-19
xxxICR	0x03FE2 to 0x03FFB	R/W	Maskable interrupt control register	III-20 to 45
Reserved	0x03FFF	-	Reserved (For reading interrupt vector data on interrupt process)	-

*1 a part of bit is for read only

2.1.3 Instruction Execution Controller

The instruction execution controller consists of four blocks: memory, instruction queue, instruction registers, and instruction decoder.

Instructions are fetched in 1-byte units, and temporarily stored in the 2-byte instruction queue. Transfer is made in 1-byte or half-byte units from the instruction queue to the instruction register to be decoded by the instruction decoder.

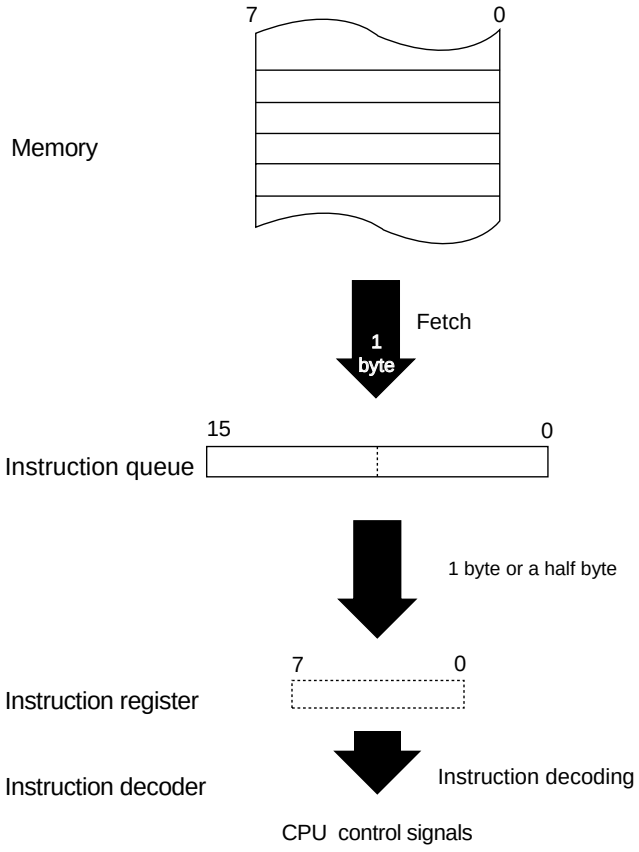


Figure:2.1.2 Instruction Execution Controller Configuration

2.1.4 Pipeline Process

Pipeline process means that reading and decoding are executed at the same time on different instructions, then instructions are executed without stopping. Pipeline process makes instruction execution continual and speedy. This process is executed with instruction queue and instruction decoder.

Instruction queue is buffer that fetches the second instruction in advance. That is controlled to fetch the next instruction when instruction queue is empty at each cycle on execution. At the last cycle of instruction execution, the first word (operation code) of executed instruction is stored to instruction register. At that time, the next operand or operation code is fetched to instruction queue, so that the next instruction can be executed immediately, even if register direct (da) or immediate data (imm) is needed at the first cycle of the next instruction execution. But on some other instruction such as branch instruction, instruction queue becomes empty on the time that the next operation code to be executed is stored to instruction register at the last cycle. Therefore, only when instruction queue is empty, and direct address (da) or immediate data (imm) are needed, instruction queue keeps waiting for a cycle.

Instruction queue is controlled automatically by hardware so that there is no need to be controlled by software. But when instruction execution time is estimated, operation of instruction queue should be into consideration. Instruction decoder generates control signal at each cycle of instruction execution by micro program control. Instruction decoder uses pipeline process to decode instruction queue at one cycle before control signal is needed.

2.1.5 Registers for Address

Registers for address include program counter (PC), address registers (A0, A1), and stack pointer (SP)

■ Program Counter (PC)

This register gives the address of the currently executing instruction. It is 21 bits wide to provide access to a 1 MB address space in half byte(4-bit increments). The LSB of the program counter is used to indicate half byte instruction. The program counter after reset is stored from the value of vector table at the address of 0x04000.

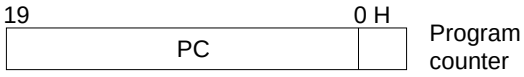


Figure:2.1.3 Program Counter

■ Address Registers (A0, A1)

These registers are used as address pointers specifying data locations in memory. They support the operations involved in address calculations (i.e. addition, subtraction and comparison). Those pointers are 2 bytes data. Transfers between these registers and memory are always in 16-bit units. Either odd or even address can be transferred. At reset, the value of address register is undefined.

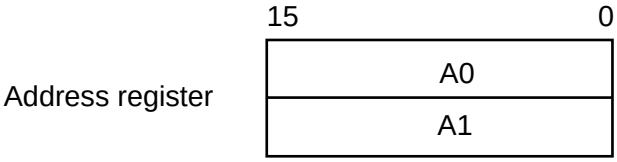


Figure:2.1.4 Address Registers

■ Stack Pointer (SP)

This register gives the address of the byte at the top of the stack. It is decremented during push operations and incremented during pop operations. Ar reset, the value of SP is undefined.

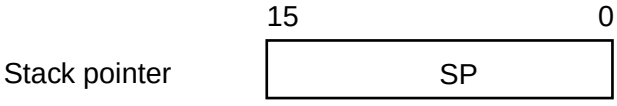


Figure:2.1.5 Stack Pointer

2.1.6 Registers for Data

Registers for data include four data registers (D0, D1, D2, D3).

■ Data Registers (D0, D1, D2, D3)

Data registers D0 to D3 are 8-bit general-purpose registers that support all arithmetic, logical and shift operations. All registers can be used for data transfers with memory.

The four data registers may be paired to form the 16-bit data registers DW0 (D0+D1) and DW1 (D2+D3). At reset, the value of Dn is undefined.

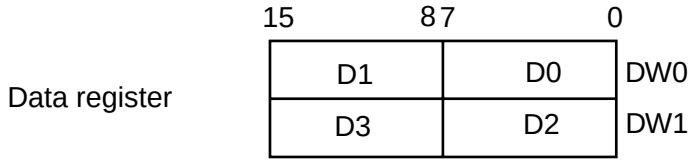


Figure:2.1.6 Data Registers

2.1.7 Processor Status Word

Processor status word (PSW) is an 8-bit register that stores flags for operation results, interrupt mask level, and maskable interrupt enable. PSW is automatically pushed onto the stack when an interrupt occurs and is automatically popped when return from the interrupt service routine.

Table:2.1.4 Processor Status Word(PSW)

bp	7	6	5	4	3	2	1	0
Flag	BKD	MIE	IM1	IM0	VF	NF	CF	ZF
At reset	0	0	0	0	0	0	0	0

bp	Flag	Description
7	BKD	Bank disable flag 0: Bank addressing is enabled. 1: Bank addressing is disabled.
6	MIE	Maskable interrupt enable 0: All maskable interrupts are disabled. 1: (xxxLVn,xxxIE) for each interrupt is enabled.
5-4	IM1 IM0	Interrupt mask level Controls maskable interrupt acceptance.
3	VF	Overflow flag 0: Overflow did not occur. 1: Overflow occured.
2	NF	Negative flag 0: MSB of operation results is "0". 1: MSB of operation results is "1".
1	CF	Carry flag 0: A carry or a borrow from MSB did not occur. 1: A carry or a borrow from MSB occured.
0	ZF	Zero flag 0: Operation result is not "0". 1: Operation result is "0".

■ Zero Flag (ZF)

Zero flag (ZF) is set to "1", when all bits are '0' in the operation result. Otherwise, zero flag is cleared to "0".

■ Carry Flag (CF)

Carry flag (CF) is set to "1", when a carry from or a borrow to the MSB occurs. Carry flag is cleared to "0", when no carry or borrow occurs.

■ Negative Flag (NF)

Negative flag (NF) is set to "1" when MSB is '1' and reset to "0" when MSB is '0'. Negative flag is used to handle a signed value.

■ Overflow Flag (VF)

Overflow flag (VF) is set to "1", when the arithmetic operation results overflow as a signed value. Otherwise, overflow flag is cleared to "0". Overflow flag is used to handle a signed value.

■ Interrupt Mask Level (IM1 and IM0)

Interrupt mask level (IM1 and IM0) controls the maskable interrupt acceptance in accordance with the interrupt factor interrupt priority for the interrupt control circuit in the CPU. The two-bit control flag defines levels '0' to '3'. Level 0 is the highest mask level. The interrupt request will be accepted only when the level set in the interrupt level flag (xxxLVn) of the interrupt control register (xxxICR) is higher than the interrupt mask level. When the interrupt is accepted, the level is reset to IM1-IM0, and interrupts whose mask levels are the same or lower are rejected during the accepted interrupt processing.

Table:2.1.5 Interrupt Mask Level and Interrupt Acceptance

	Interrupt mask level		Priority	Acceptable interrupt level
	IM1	IM0		
Mask level 0	0	0	Highest	Non-maskable interrupt (NMI) only
Mask level 1	0	1	High	NMI, level 0
Mask level 2	1	0	Low	NMI, level 0 to 1
Mask level 3	1	1	Lowest	NMI, level 0 to 2

■ Maskable Interrupt Enable (MIE)

Maskable interrupt enable flag (MIE) enables/disables acceptance of maskable interrupts by the CPU's internal interrupt acceptance circuit. A '1' enables maskable interrupts; a '0' disables all maskable interrupts regardless of the interrupt mask level (IM1-IM0) setting in PSW. This flag is not changed by interrupts.

■ Bank disable flag (BKD)

Bank disable flag (BKD) enables/disables bank addressing of 64 KB unit. When this flag is set to “0”, bank addressing is enabled and you can access to total 16 banks by setting the bank register value. When this flag is set to “1”, bank addressing is disabled and the only area you can access is the first 64 KB. On an interrupt generation, BKD flag is automatically set to “1” and bank addressing is disabled. At returning from interrupt service routine, the value of BKD flag is returned to the previous one. (before the interrupt generation)

To enable bank addressing in an interrupt service routine, reset the BKD flag to “0” before access to data.

2.1.8 Address Space

The address space of this LSI is 1 MB. (max.) The instruction and data areas are not separated.
The instruction area can be used as linear address space. The data area needs bank spscification in every 64 KB. (The inicial value is first 64 KB space). The data described in this section includes RAM data and ROM table data.
The data area consists of an area of 256 bytes that supports efficient access with RAM short addressing and an area of 256 bytes that supports efficient access with I/O short addressing.
The memory control register controls memory to be expanded.

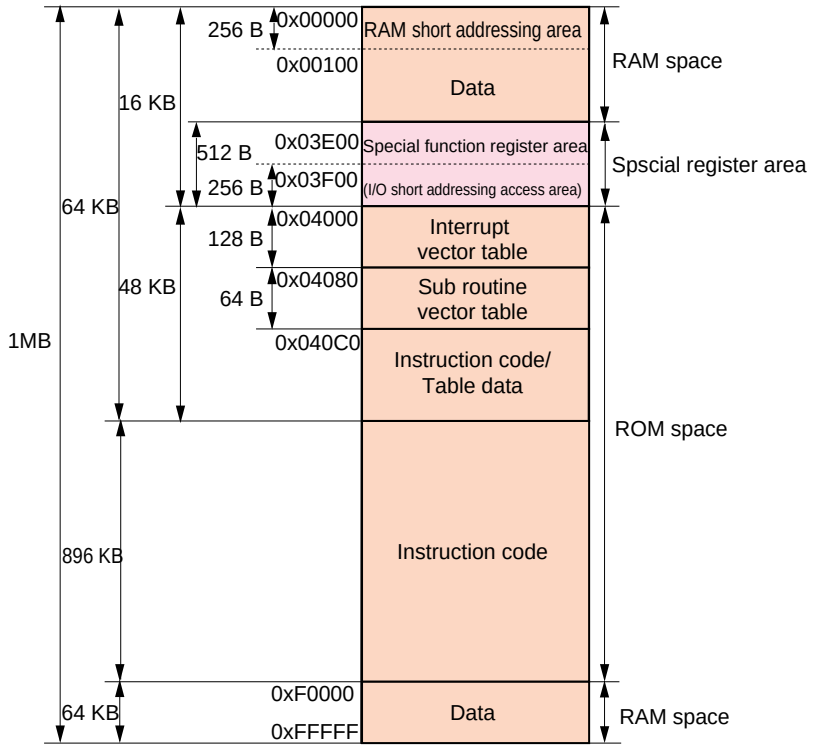


Figure:2.1.7 Address Space

2.1.9 Addressing Modes

This LSI supports the nine addressing modes.

Each instruction uses a combination of the following addressing

1) Register direct

2) Immediate

3) Register indirect

4) Register relative indirect

5) Stack relative indirect

6) Absolute

7) RAM short

8) I/O short

9) Handy

These addressing modes are well-suited for C language compilers. All of the addressing modes can be used for data transfer instructions. In modes that allow half-byte addressing, the relative value can be specified in half-byte (4-bit) increments, so that instruction length can be shorter. Handy addressing reuses the last memory address accessed and is only available with the MOV and MOVW instructions. Combining handy addresssing with absolute addressing reduces code size. For transfer data between memory, 8 addressing modes ; register indirect, register relative indirect, stack relative indirect, absolute, RAM short, I/O short, handy can be used. For operation instruction, register direct and immediate can be used. Refer to instruction's manual for the MN101E series.

This LSI is designed for 8-bit data access. It is possible to tranfer data in 16-bit increments with odd or all even addresses.

Addressing mode		Effective address	Explanation
Register direct	Dn/DWn An/SP PSW	-	Directly specifies the register. Only internal registers can be specified.
Immediate	imm4/imm8 imm16	-	Directly specifies the operand or mask value appended to the instruction code.
Register indirect	(An)	15 0 An	Specifies the address using an address register.
Register relative indirect	(d8, An)	15 0 An+d8	Specifies the address using an address register with 8-bit displacement.
	(d16, An)	15 0 An+d16	Specifies the address using an address register with 16-bit displacement.
	(d4, PC) (branch instructions only)	17 0 H PC+d4 * 1	Specifies the address using the program counter with 4-bit displacement and H bit.
	(d7, PC) (branch instructions only)	17 0 H PC+d7 * 1	Specifies the address using the program counter with 7-bit displacement and H bit.
	(d11, PC) (branch instructions only)	17 0 H PC+d11 * 1	Specifies the address using the program counter with 11-bit displacement and H bit.
	(d12, PC) (branch instructions only)	17 0 H PC+d12 * 1	Specifies the address using the program counter with 12-bit displacement and H bit.
	(d16, PC) (branch instructions only)	17 0 H PC+d16 * 1	Specifies the address using the program counter with 16-bit displacement and H bit.
Stack relative indirect	(d4, SP)	15 0 SP+d4	Specifies the address using the stack pointer with 4-bit displacement.
	(d8, SP)	15 0 SP+d8	Specifies the address using the stack pointer with 8-bit displacement.
	(d16, SP)	15 0 SP+d16	Specifies the address using the stack pointer with 16-bit displacement.
Absolute	(abs8)	7 0 abs8	Specifies the address using the operand value appended to the instruction code. Optimum operand length can be used to specify the address.
	(abs12)	11 0 abs12	
	(abs16)	15 0 abs16	
	(abs18) (branch instructions only)	17 0 H abs18 * 1	
	(abs 20) (branch instructions only)	19 0 H abs20 * 1	
RAM short	(abs8)	7 0 abs8	Specifies an 8-bit offset from the address x'00000'.
I/O short	(io8)	15 0 IOTOP+io8	Specifies an 8-bit offset from the top address (x'03F00') of the special function register area.
Handy	(HA)	-	Reuses the last memory address accessed and is only available with the MOV and MOVW instructions. Combined use with absolute addressing reduces code size.

* 1 H: half-byte bit

Figure:2.1.8 Address Space

2.1.10 Machine Clock

Machine clock is generated based on the system clock dividing the source oscillation frequency. The machine clock is the base timing for control of CPU.

■ Internal Memory Access (no wait cycle) (NORMAL mode)

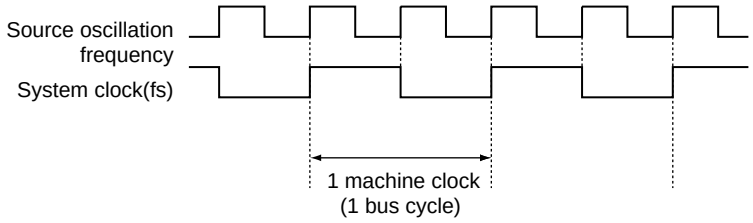


Figure:2.1.9 Machine Clock (no wait cycle)

■ External Memory Access (0, 1, 2, 3 wait cycle) (NORMAL mode)

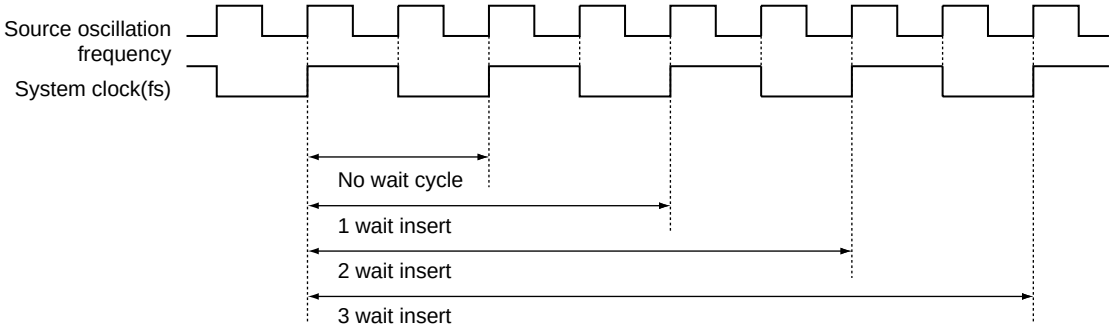


Figure:2.1.10 Machine Clock (memory wait cycle)

Wait cycle is set to fixed three wait cycle mode at reset start.

Oscillation frequency of system clock differs depending on the CPUM register settings.
[Chapter 2. 2.6 Clock Switching]

2.2 Memory Space

2.2.1 Memory Mode

ROM is the read only area and RAM is the memory area which contains readable/writable data. In addition to these, peripheral resources such as memory-mapped special registers are allocated. The MN101E series supports three memory modes (single chip mode, memory expansion mode, processor mode) in its memory model. This LSI supports three memory modes (single chip mode, memory expansion mode, processor mode) in its memory model. Setting of each mode is different.

In single chip mode, the system consists of only internal memory. In memory expansion mode, and processor mode, ROM, RAM and external device for operation can be connected. This LSI supports memory expansion mode and processor mode. (Processor mode is not available in Flash version MN101EF01M.)
Settings for each modes are as follows ;

Table:2.2.1 Mask ROM (MN101E01K / L / M)

Memory mode	MMOD pin	EXMEM flag (MEMCTR register)	EXADV3 to 1 flags (EXADV register)
Single chip mode	L	0	-
Memory expansion mode	L	1	1
Processor mode	H	-	-
(Loader program mode)	-		

Table:2.2.2 Flash EEPROM (MN101EF01M)

Memory mode	MMOD pin	EXMEM flag (MEMCTR register)	EXADV3 to 1 flags (EXADV register)
Single chip mode	L	0	-
Memory expansion mode	L	1	1
(Processor mode)	-		
Loader program mode	H	-	-

Fix the MMOD pin always to “L” or “H” level. Do not change the settings of this pin after reset release.

2.2.2 Bank Function

CPU of MN101E series has basically 64 KB memory address space. On this LSI, address space can be expanded up to 16 banks (1 MB) based on units of 64KB, by bank function. In the expanded space based on bank units, each memory mode (single chip mode, memory expansion mode, processor mode) has a different data access.

Bank function can be used by setting the proper bank area to the bank register for source address (SBNKR) or the bank register for destination address (DBNKR). At reset, both of the SBNKR register and the DBNKR register indicate bank 0. Bank function is valid after setting any value except "00" to the SBNKR register or the DBNKR register. When the both registers of SBNKR and DBNKR are operated at interrupt processing, pushing onto the stack or popping are necessary.

Table:2.2.3 Address Range

SBA3 (DBA3)	SBA2 (DBA2)	SBA1 (DBA1)	SBA0 (DBA0)	Bank area	Address range
0	0	0	0	bank 0	0x00000 to 0x0FFFF
0	0	0	1	bank 1	0x10000 to 0x1FFFF
0	0	1	0	bank 2	0x20000 to 0x2FFFF
0	0	1	1	bank 3	0x30000 to 0x3FFFF
0	1	0	0	bank 4	0x40000 to 0x4FFFF
0	1	0	1	bank 5	0x50000 to 0x5FFFF
0	1	1	0	bank 6	0x60000 to 0x6FFFF
0	1	1	1	bank 7	0x70000 to 0x7FFFF
1	0	0	0	bank 8	0x80000 to 0x8FFFF
1	0	0	1	bank 9	0x90000 to 0x9FFFF
1	0	1	0	bank 10	0xA0000 to 0xAFFFF
1	0	1	1	bank 11	0xB0000 to 0xBFFFF
1	1	0	0	bank 12	0xC0000 to 0xCFFFF
1	1	0	1	bank 13	0xD0000 to 0xDFFFF
1	1	1	0	bank 14	0xE0000 to 0xEFFFF
1	1	1	1	bank 15	0xF0000 to 0xFFFFF

When bank area is changed at interrupt processing, pushing onto the stack or popping must be done by program, if it necessary.

During bank function is valid, I/O short instruction should be used for access to the special function register area (0x03F00 to 0x03FFF). For access to the memory space 0x13F00 to 0x13FFF, 0x23F00 to 0x23FFF, 0x33F00 to 0x33FFF, 0x43F00 to 0x43FFF, 0x53F00 to 0x53FFF, 0x63F00 to 0x63FFF, 0x73F00 to 0x73FFF, 0x83F00 to 0x83FFF, 0x93F00 to 0x93FFF, 0xA3F00 to 0xA3FFF, 0xB3F00 to 0xB3FFF, 0xC3F00 to 0xC3FFF, 0xD3F00 to 0xD3FFF, 0xE3F00 to 0xE3FFF, 0xF3F00 to 0xF3FFF, both instructions of register indirect and register relative indirect should be used.
[Chapter 2 2-1-9. Addressing Modes]

Set the stack area to bank 0. Provided C-compiler for this series does not support the bank function.

Our linker supports the function that prevents data straddling over bank boundaries. See “MN101C Series Cross-assembler User’s Manual” for details.

■ Bank Register for Source Address

The SBNKR register is used to specify bank area for loading instruction from memory to register. Once this register is specified, bank control is valid for all addressing modes except I/O short instruction and stack relative indirect instruction.
[Chapter 2 2-1-9. Addressing modes]

Table:2.2.4 Bank Register for Source Address (SBNKR:0x03F0A)

bp	7	6	5	4	3	2	1	0
Flag	-	-	-	-	SBA3	SBA2	SBA1	SBA0
At reset	-	-	-	-	0	0	0	0

bp	Flag	Description
7-4	-	-
3-0	SBA3 SBA2 SBA1 SBA0	Bank for source address selection 0000: bank 0 0001: bank 1 0010: bank 2 0011: bank 3 0100: bank 4 0101: bank 5 0110: bank 6 0111: bank 7 1000: bank 8 1001: bank 9 1010: bank 10 1011: bank 11 1100: bank 12 1101: bank 13 1110: bank 14 1111: bank 15

■ Bank Register for Destination Address

The DBNKR register is used to specify bank area for storing instruction from register to memory. Once this register is specified, bank control is valid for all addressing modes except I/O short instruction,stack relative indirect instruction and bit manipulation instruction.
[Chapter 2 2.1.9. Addressing modes]

Table:2.2.5 Bank Register for Destination Address (DBNKR:0x03F0B)

bp	7	6	5	4	3	2	1	0
Flag	-	-	-	-	DBA3	DBA2	DBA1	DBA0
At reset	-	-	-	-	0	0	0	0

bp	Flag	Description
7-4	-	-
3-0	DBA3 DBA2 DBA1 DBA0	Bank for source address selection 0000: bank 0 0001: bank 1 0010: bank 2 0011: bank 3 0100: bank 4 0101: bank 5 0110: bank 6 0111: bank 7 1000: bank 8 1001: bank 9 1010: bank A 1011: bank B 1100: bank C 1101: bank D 1110: bank E 1111: bank F

Read, modify, write instruction such as bit manipulation (BSET, BCLR, BTST) depend on the value of the SBNKR register, both of for reading and writing.

2.2.3 RAM Space

■ RAM Space

MN101E series has maximum 64 KB of RAM space.

RAM space is devided to be allocated to the address space. Mirror RAM space is provided for effective utilization of the devided RAM spaces.

RAM space: 0x00000 to 0x03DFF (15.5 KB) + 0xF3E00 to 0xFFFFF (48.5 KB) (maximum 64KB)
Mirror RAM space: 0xF0000 to 0xF3DFF = 0x00000 to 0x03DFF (Mapped to same RAM space)

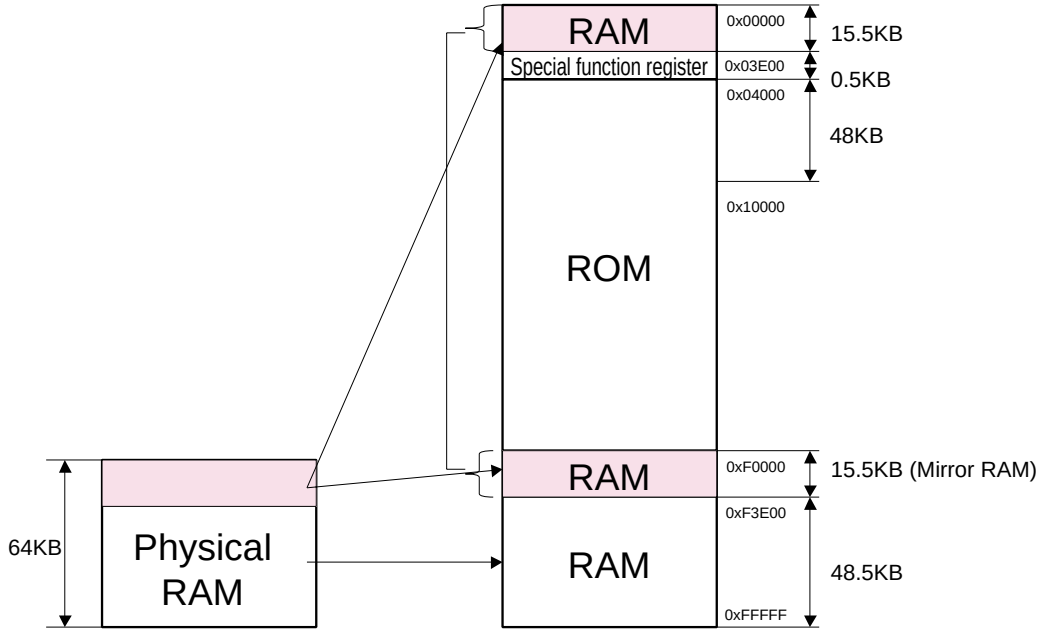


Figure:2.2.1 RAM Space

■ How to use mirror RAM Space

Sub routine A
Address bank 15
mov x'0F', (SBNKR) : Source side
mov x'0F', (DBNKR) : Distination side
Transfer data 15 between memories (1)
mov (x'XYZZ'), dn
mov dn, (x'ABCD') : x'XYZZ' → x'ABCD'
(x'ABCD', x'XYZZ' are address of abs16.)

Sub routine B (Address bank 0)
mov (x'ABCD', d1) : Use mirror function (2)

Execute the same access ignoring the upper 4 bits.

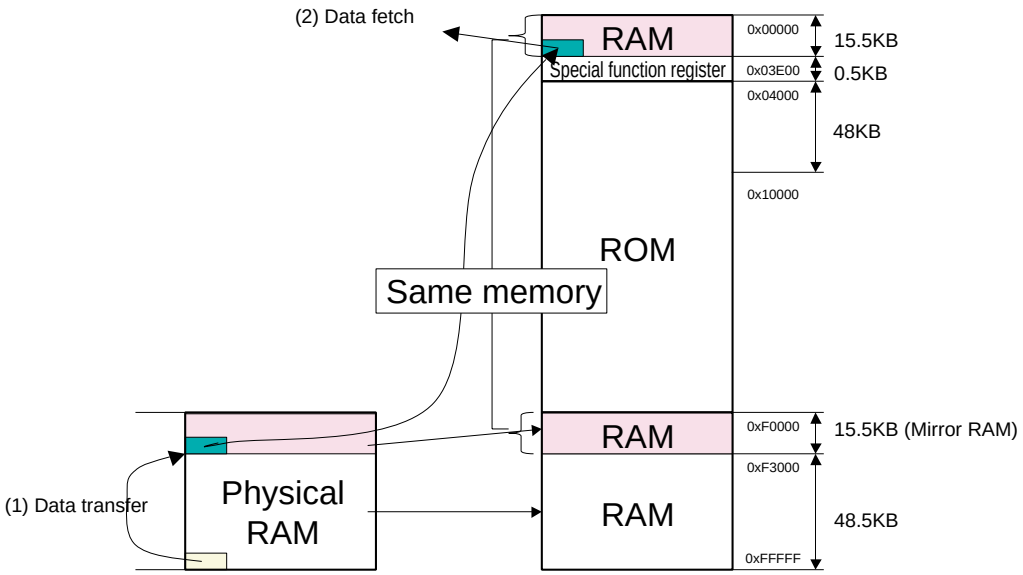


Figure:2.2.2 How to use mirror RAM Space

2.2.4 Single-chip Mode

In single-chip mode, the system consists of only internal memory. This is the optimized memory mode and allows construction of systems with the highest performance. The single-chip mode uses only internal ROM and internal RAM. The MN101E series devices offer up to 64 KB of RAM and up to 944 KB of ROM. This LSI offers 14 KB of RAM and 320 KB of ROM.

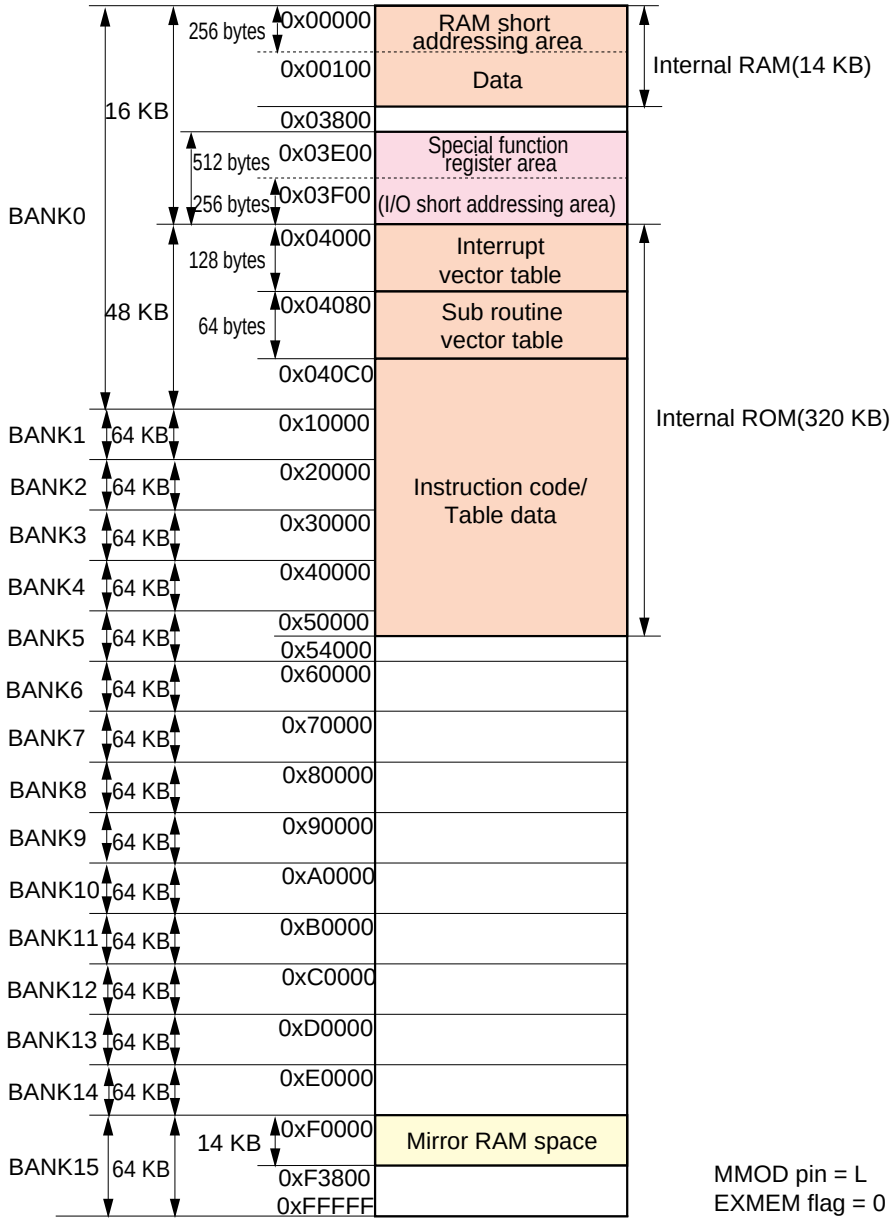


Figure:2.2.3 Single-chip Mode

The value of internal RAM is uncertain when power is applied to it.
It needs to be initialized before used.

2.2.5 Memory Expansion Mode

The MN101E series can connect external ROM, RAM and external devices for operation in memory expansion mode. This is the mode to expand to external memory while using internal ROM and RAM.

The memory expansion mode is set by assigning EXMEM flag (bp4) of the memory control register (MEMCTR), on single chip mode. The address expansion control register(EXADV) controls address output to pins.

Memory areas can be externally expanded as follows :

ROM: 0x70000-0xEFFFF (512 KB)

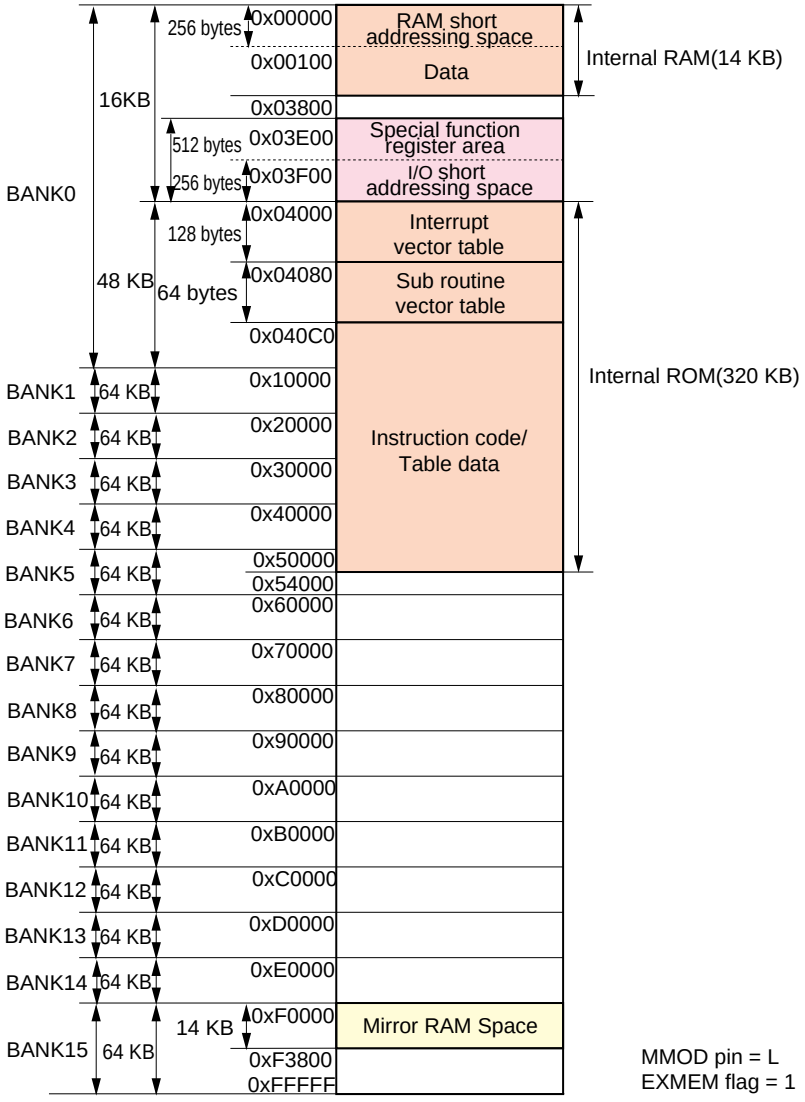


Figure:2.2.4 Memory Expansion Mode

The value of internal RAM is uncertain when power is applied to it.
It needs to be initialized before used.

2.2.6 Processor Mode

In processor mode, internal RAM and externaly expanded ROM, RAM can be used. Internal ROM cannot be used in this mode. (This mode is not available in Flash version MN101EF01M.)

Setting MMOD pin to “H” sets the processor mode.

Memory areas can be externally expanded as follows :

ROM: 0x04000-0x3FFFF (944 KB)

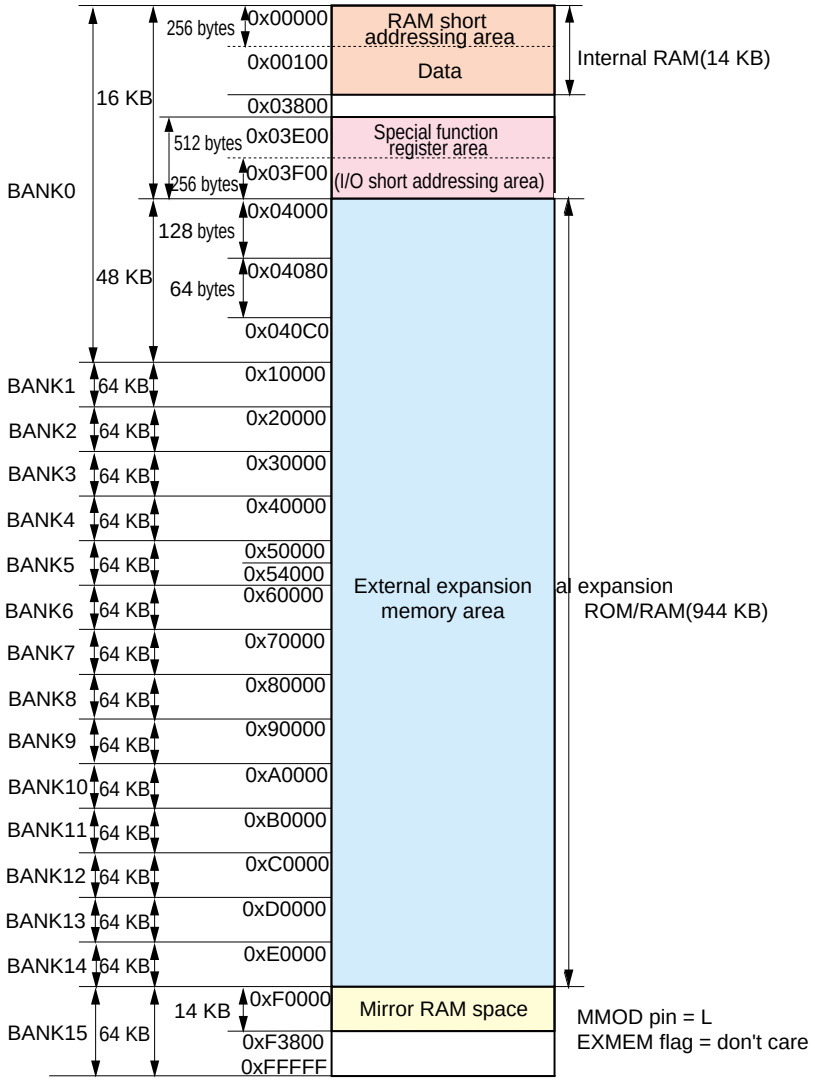


Figure:2.2.5 Memory Expansion Mode

Processor mode is not available in Flash version MN101EF01M

The value of internal RAM is uncertain when power is applied to it.
It needs to be initialized before used.

2.2.7 Special Function Registers

The MN101E series locates the special function registers (I/O spaces) at the addresses 0x03F00 to 0x03FFF in memory space. The special function registers of this LSI are located as shown below.

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
03EFX to 03F0X																Reserved
03F0X	CPUM	MEMCTR	WDCTR	DLYCTR	Reserved					RCCTR	SBNKR	DBNKR			EXADV	Reserved	CPU mode, memory control
03F1X	P0OUT	P1OUT	P2OUT	P3OUT	P4OUT	P5OUT	P6OUT	P7OUT	P8OUT	P9OUT	PAOUT	PDOMD	P0ODC	PDOUT	EDGDT	P7SYO	I/O Port control
03F2X	P0IN	P1IN	P2IN	P3IN	P4IN	P5IN	P6IN	P7IN	P8IN	P9IN	PAIN	P1OMD	P3ODC	PDIN	NFCTR	P7SEV	
03F3X	P0DIR	P1DIR	P2DIR	P3DIR	P4DIR	P5DIR	P6DIR	P7DIR	P8DIR	P9DIR	PADIR	PAIMD	P4ODC	PDDIR	KEYT3-1 IMD	TMSEL	
03F4X	P0PLU	P1PLU	P2PLU	P3PLU	P4PLU	P5PLU	P6PLU	P7PLU	P8PLU	P9PLU	PAPLU	SELUD	P9ODC	PDPLU	IRQSEL	SCSEL	
03F5X	TM0BC	TM1BC	TM0OC	TM1OC	TM0MD	TM1MD	CK0MD	CK1MD	TM2BC	TM3BC	TM2OC	TM3OC	TM2MD	TM3MD	CK2MD	CK3MD	Timer control
03F6X	TM4BC	TM5BC	TM4OC	TM5OC	TM4MD	TM5MD	CK4MD	CK5MD	TM6BC	TM6OC	TM6MD	TBCLR	TM6BEN	LVLMD	IOCTR	PSCMD	
03F7X	TM7BCL	TM7BCH	TM7OC1	TM7OC1	TM7PR1	TM7PR1	TM7ICL	TM7ICH	TM7MD1	TM7MD2	TM7OC2	TM7OC2	TM7PR2	TM7PR2	P1CNT0	RMCTR	
03F8X															SCCKSE	SC0MD0	
03F9X	SC0MD1	SC0MD2	SC0MD3	SC0STR	RXBUF0	TXBUF0	SC2MD0	SC2MD1	SC2MD3	SC2STR	SC2TRB	TXBUF2	SC2CTR	SC1MD0	SC1MD1	SC1MD2	Serial I/F control
03FAX	SC1MD3	SC1STR	RXBUF1	TXBUF1	SC3MD0	SC3MD1	SC3MD3	SC3STR	SC3TRB	TXBUF3	SC3CTR	SC4MD0	SC4MD1	SC4MD2	SC4MD3	SC4STR	
03FBX	RXBUF4	TXBUF4	ANCTR0	ANCTR1	ANCTR2	ANBUF0	ANBUF1								DA2CTR	DA2DR0	Analog I/F control
03FCX	RC0APL	RC0APM	RC0APH	RC1APL	RC1APM	RC1APH	RC2APL	RC2APM	RC2APH								ROM correction control
03FDX	AT1CNT	AT1CNT	AT1TRC	AT1 MAP0L	AT1 MAP0M	AT1 MAP0H	AT1 MAP1L	AT1 MAP1M	AT1 MAP1H						Reserved	Reserved	ATC control
03FEX	Reserved	NMICR	IRQ0ICR	IRQ1ICR	IRQ2ICR	IRQ3ICR	IRQ4ICR	IRQ5ICR	TM0ICR	TM1ICR	TM2ICR	TM3ICR	TM4ICR	TM5ICR	TM6ICR	TBICR	Interrupt control
03FFX	TM7ICR	T7OC2ICR	SC0RICR	SC0TICR	SC1RICR	SC1TICR	SC2ICR	SC3ICR	SC4RICR	SC4TICR	ADICR	ATC1ICR				Reserved	

Figure:2.2.6 Register Map

2.3 ROM Correction

2.3.1 Overview

This LSI can correct and change max. 3 parts in a program on mask ROM with ROM correction function. The correct program is read from the external to the RAM space by using the external EEPROM or by using the serial transmission. This function is valid to the system with the external EEPROM.

2.3.2 Correction Sequence

Program is corrected as following steps.

(1) The instruction execution address is compared to the correction address.

(2) Program counter is branched indirectly to the RAM address (the head address of the correct program) stored to the RC vector table (RCnV(L), RCnV(H)), after matching the above addresses. This instruction needs 6 cycle.

(3) The corrected program at the RAM area is executed.

(4) Program counter is branched back to the program at ROM area.

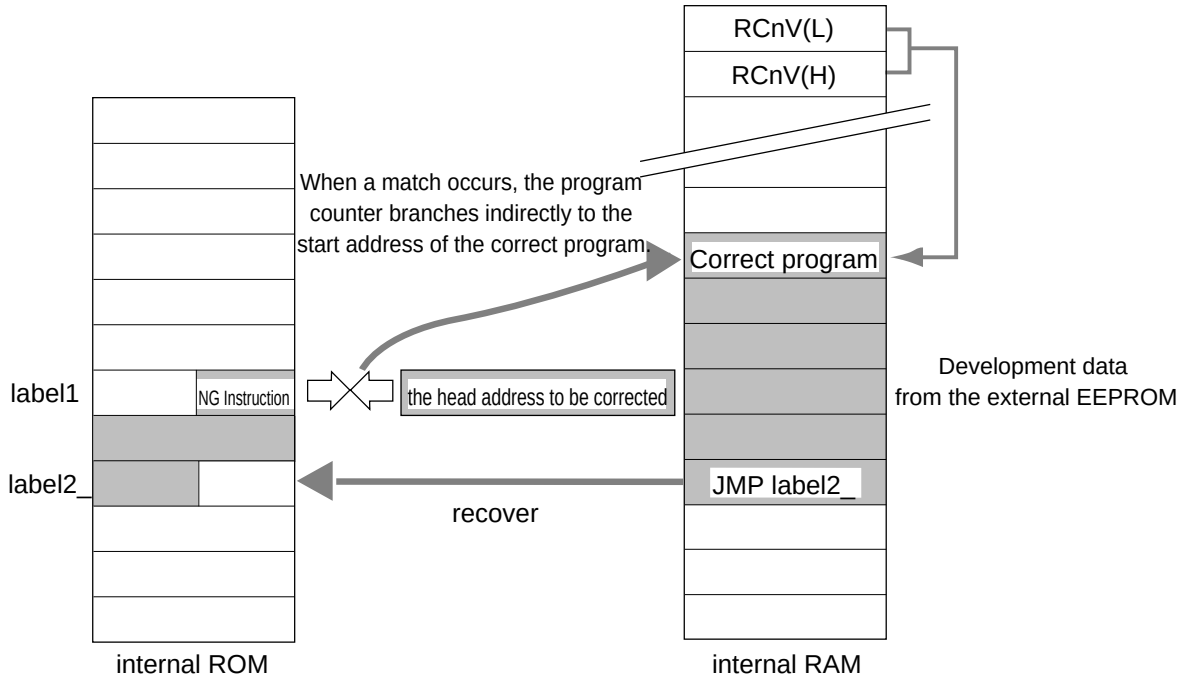


Figure:2.3.1 ROM Correction

The ROM correction setup procedure is as follows.

(1) Set the head address of the program to be corrected to the ROM correction address setting register (RCnAPH/M/L).

(2) Set the correct program at RAM area.

(3) Set the head address of the correct program to RC vector table (RCnV(L), RCnV(H)).

(4) Set the RCnEN flag of ROM correction control register (RCCTR) to enable the ROM correction.

When the instruction of the corrected program head address is the half-byte instruction, the ROM correction checks the execution instruction of the half-byte. Therefore, set the address by a byte to the ROM correction address setting register.

When the instruction of the corrected program last address is the half-byte instruction, the recover address should be set by half byte.

2.3.3 ROM Correction Control Register

ROM correction control register (RCCTR) and ROM correction address setting register (RCnAPL, RCnAPM, RCnAPH) control the ROM correction.

ROM correction control register (RCCTR) enables/disables the ROM correction function to 3 parts of the program to be corrected. When the RCnEN flag is set, the ROM correction is activated. And when the ROM address (the instruction execution address) reaches the set address to the ROM correction address setting register, it branches indirectly to the RAM address set on the RC vector table (RCnV(L), RCnV(H)). Set the RCnEN flag after setting the ROM correction address setting register.

■ ROM Correction Control Register(RCCTR)

Table:2.3.1 ROM Correction Control Regiser (RCCTR : 0x03F09)

bp	7	6	5	4	3	2	1	0
Flag	-	-	-	-	-	RC2EN	RC1EN	RC0EN
At reset	-	-	-	-	-	0	0	0
Access	R/W							

bp	Flag	Description
7-3	-	-
2	RC2EN	3rd address ROM correction control 0: disable 1: enable
1	RC1EN	2nd address ROM correction control 0: disable 1: enable
0	RC0EN	1st address ROM correction control 0: disable 1: enable

This register set the head address, which instructions to be corrected are stored to. Once the instruction execution address reaches to the set value to this register, program counter branches indirectly to the set address to the RC vector table (RCnV(L), RCnV(H)). When the ROM correction should be valid, set the RCnEN flag of the ROM correction control register (RCCTR) after setting the address to this register,.

■ ROM Correction Address 0 Setting Register (RC0AP)

Table:2.3.2 ROM Correction Address 0 Setting Register (lower 8 bits) (RC0APL : 0x03FC0)

bp	7	6	5	4	3	2	1	0
Flag	RC0APL7	RC0APL6	RC0APL5	RC0APL4	RC0APL3	RC0APL2	RC0APL1	RC0APL0
At reset	0	0	0	0	0	0	0	0
Access	R/W							

Table:2.3.3 ROM Correction Address 0 Setting Register (middle 8 bits) (RC0APM : 0x03FC1)

bp	7	6	5	4	3	2	1	0
Flag	RC0APM7	RC0APM6	RC0APM5	RC0APM4	RC0APM3	RC0APM2	RC0APM1	RC0APM0
At reset	0	0	0	0	0	0	0	0
Access	R/W							

Table:2.3.4 ROM Correction Address 0 Setting Register (upper 2 bits) (RC0APH : 0x03FC2)

bp	7	6	5	4	3	2	1	0
Flag	-	-	-	-	RC0APH3	RC0APH2	RC0APH1	RC0APH0
At reset	-	-	-	-	0	0	0	0
Access	R/W							

■ ROM Correction Address 1 Setting Register (RC1AP)

Table:2.3.5 ROM Correction Address 1 Setting Register (lower 8 bits) (RC1APL : 0x03FC3)

bp	7	6	5	4	3	2	1	0
Flag	RC1APL7	RC1APL6	RC1APL5	RC1APL4	RC1APL3	RC1APL2	RC1APL1	RC1APL0
At reset	0	0	0	0	0	0	0	0
Access	R/W							

Table:2.3.6 ROM Correction Address 1 Setting Register (middle 8 bits) (RC1APM : 0x03FC4)

bp	7	6	5	4	3	2	1	0
Flag	RC1APM7	RC1APM6	RC1APM5	RC1APM4	RC1APM3	RC1APM2	RC1APM1	RC1APM0
At reset	0	0	0	0	0	0	0	0
Access	R/W							

Table:2.3.7 ROM Correction Address 1 Setting Register (upper 2 bits) (RC1APH : 0x03FC5)

bp	7	6	5	4	3	2	1	0
Flag	-	-	-	-	RC1APH3	RC1APH2	RC1APH1	RC1APH0
At reset	-	-	-	-	0	0	0	0
Access	R/W							

■ ROM Correction Address 2 Setting Register (RC2AP)

Table:2.3.8 ROM Correction Address 2 Setting Register (lower 8 bits) (RC2APL : 0x03FC6)

bp	7	6	5	4	3	2	1	0
Flag	RC2APL7	RC2APL6	RC2APL5	RC2APL4	RC2APL3	RC2APL2	RC2APL1	RC2APL0
At reset	0	0	0	0	0	0	0	0
Access	R/W							

Table:2.3.9 ROM Correction Address 2 Setting Register (middle 8 bits) (RC2APM : 0x03FCE7)

bp	7	6	5	4	3	2	1	0
Flag	RC2APM7	RC2APM6	RC2APM5	RC2APM4	RC2APM3	RC2APM2	RC2APM1	RC2APM0
At reset	0	0	0	0	0	0	0	0
Access	R/W							

Table:2.3.10 ROM Correction Address 2 Setting Register (upper 2 bits) (RC2APH : 0x03FC8)

bp	7	6	5	4	3	2	1	0
Flag	-	-	-	-	RC2APH3	RC2APH2	RC2APH1	RC2APH0
At reset	-	-	-	-	0	0	0	0
Access	R/W							

Do not set the same address to more than two RCnAP (H/M/L) register. If there are several registers set the same address, the order of priority is as follows :

RC0AP > RC1AP > RC2AP

Here is the correspondence of the ROM correction address setting register, a ROM correction control flag of ROM correction control register and the RC vector table.

	ROM Correction address setting register		ROM correction control flag	RC-vector table	
	Register	address		vector	address
1st correction	RC0APL	0x3FC0	RC0EN	RC0V(L)	0x0010
	RC0APM	0x3FC1		RC0V(H)	0x0011
	RC0APH	0x3FC2			
2nd correction	RC1APL	0x3FC3	RC1EN	RC1V(L)	0x0012
	RC1APM	0x3FC4		RC1V(H)	0x0013
	RC1APH	0x3FC5			
3rd correction	RC2APL	0x3FC6	RC2EN	RC2V(L)	0x0014
	RC2APM	0x3FC7		RC2V(H)	0x0015
	RC2APH	0x3FC8			

2.3.4 ROM Correction Setup Example

■ Initial Routine with ROM Correction

The following routine should be set to correct the program. Also store the ROM correction setup and the correct program to the external EEPROM, in advance.

Here is the steps for ROM correction execution.

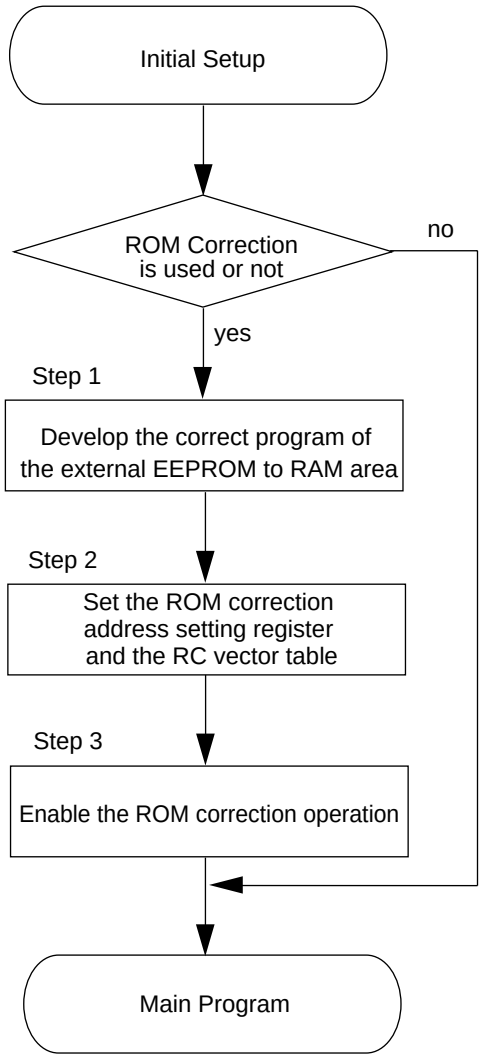
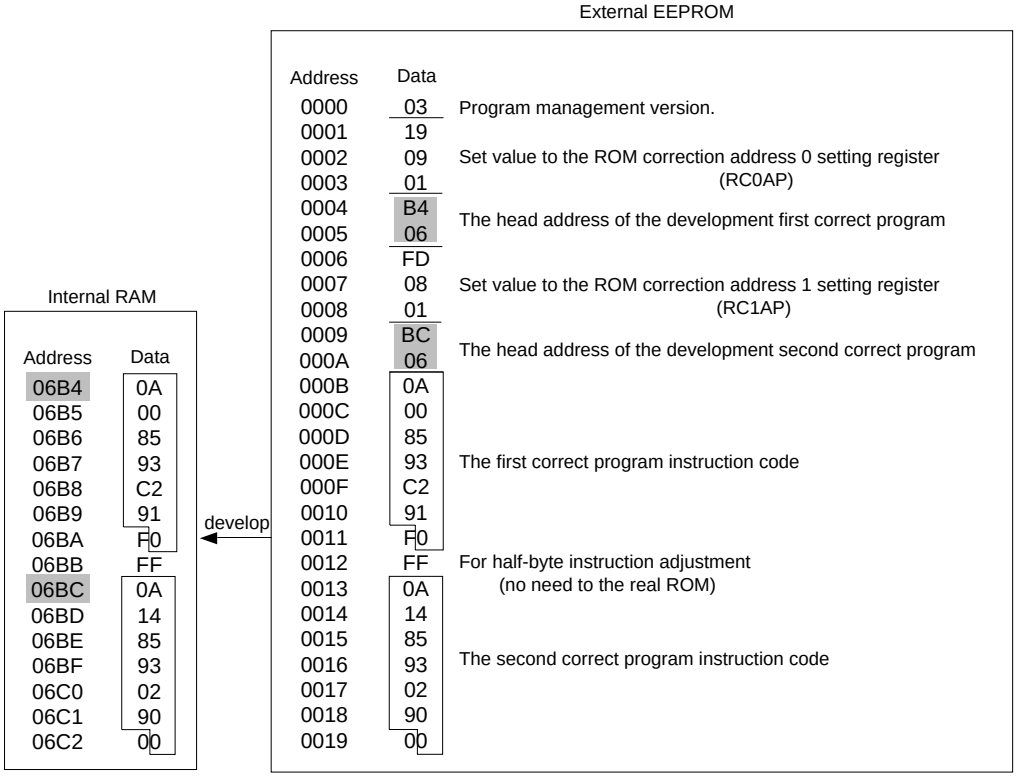


Figure:2.3.2 Initial Routine for ROM Correction

■ ROM Correction Setup Example

The setup procedure with ROM correction to correct 2 parts of the program is shown below. For the step to execute the ROM correction, refer to figure 2.3.2. Initial Routine for ROM correction on the previous page.

(STEP 1) Develop the correct program of the external EEPROM to RAM area.

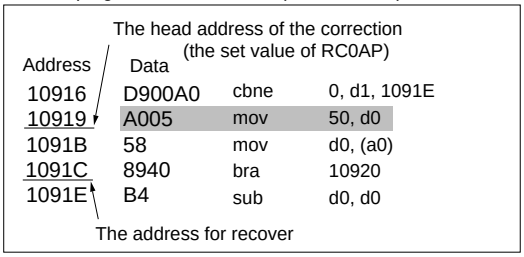


(STEP 2) Set the ROM correction address setting register and the RC vector table.

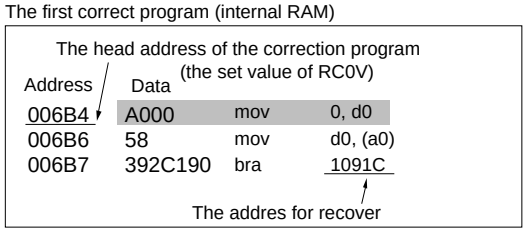
[Setup for the first correction]
Set the head address of the program to be corrected at first to the ROM correction address setting register (RC0AP).
RC0APL=0x19
RC0APM=0x09
RC0APH=0x01

Set the internal RAM address 0x06B4 that stored first correct program to the RC vector table address (RC0V(L), RC0V(H).
RC0V(L)=0xB4
RC0V(H)=0x06

The first program to be corrected (internal ROM)


The head address of the correction
(the set value of RC0AP)
Address
Data
10916 D900A0 cbne 0, d1, 1091E
10919 A005 mov 50, d0
1091B 58 mov d0, (a0)
1091C 8940 bra 10920
1091E B4 sub d0, d0
The address for recover

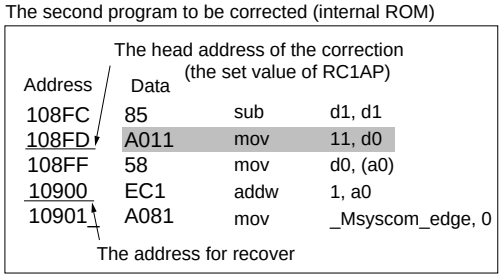
The first correct program (internal RAM)


The head address of the correction program
(the set value of RC0V)
Address
Data
006B4 A000 mov 0, d0
006B6 58 mov d0, (a0)
006B7 392C190 bra 1091C
The addres for recover

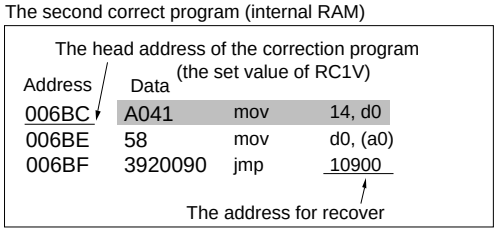
[Setup for the second correction]
Set the head address of the program to be corrected at second to the ROM correction address 1 setting register (RC1AP).
RC1APL=0xFD
RC1APM=0x08
RC1APH=0x01

Set the internal RAM address 0x06BC that stored second correct program to the RC vector table address (RC1V(L), RC1V(H).
RC1V(L)=0xBC
RC1V(H)=0x06

The second program to be corrected (internal ROM)


The head address of the correction
(the set value of RC1AP)
Address
Data
108FC 85 sub d1, d1
108FD A011 mov 11, d0
108FF 58 mov d0, (a0)
10900 EC1 addw 1, a0
10901 A081 mov _Msyscom_edge, 0
The address for recover

The second correct program (internal RAM)


The head address of the correction program
(the set value of RC1V)
Address
Data
006BC A041 mov 14, d0
006BE 58 mov d0, (a0)
006BF 3920090 jmp 10900
The address for recover

(STEP 3) Set the bit 0 (RC0EN) and the bit 1 (RC1EN) of the ROM correction control register (RCCTR) to "1".

After the main program is started, the instruction fetched address and the set address to the ROM correction address setting register (RCnAP) are always compared, then once they are matched program counter indirectly branches to the address in RAM area, that are stored to the RC vector table (RCnV).

The correction program in RAM area is executed.

Program counter recovers to the program in ROM area.

2.4 Bus Interface

2.4.1 Bus Controller

The MN101E series provides separate buses to the internal memory and internal peripheral circuits to reduce bus line loads and thus realize faster operation.

There are four such buses: ROM bus, RAM bus, peripheral expansion bus, and external expansion bus. They connect to the internal ROM, internal RAM, internal peripheral circuits, and external interfaces respectively. The bus control block controls the parallel operation of instruction read and data access, the access speed adjustment for low-speed external devices, and arbitration of bus access when using master devices on the external bus lines. A functional block diagram of the bus controller is given below.

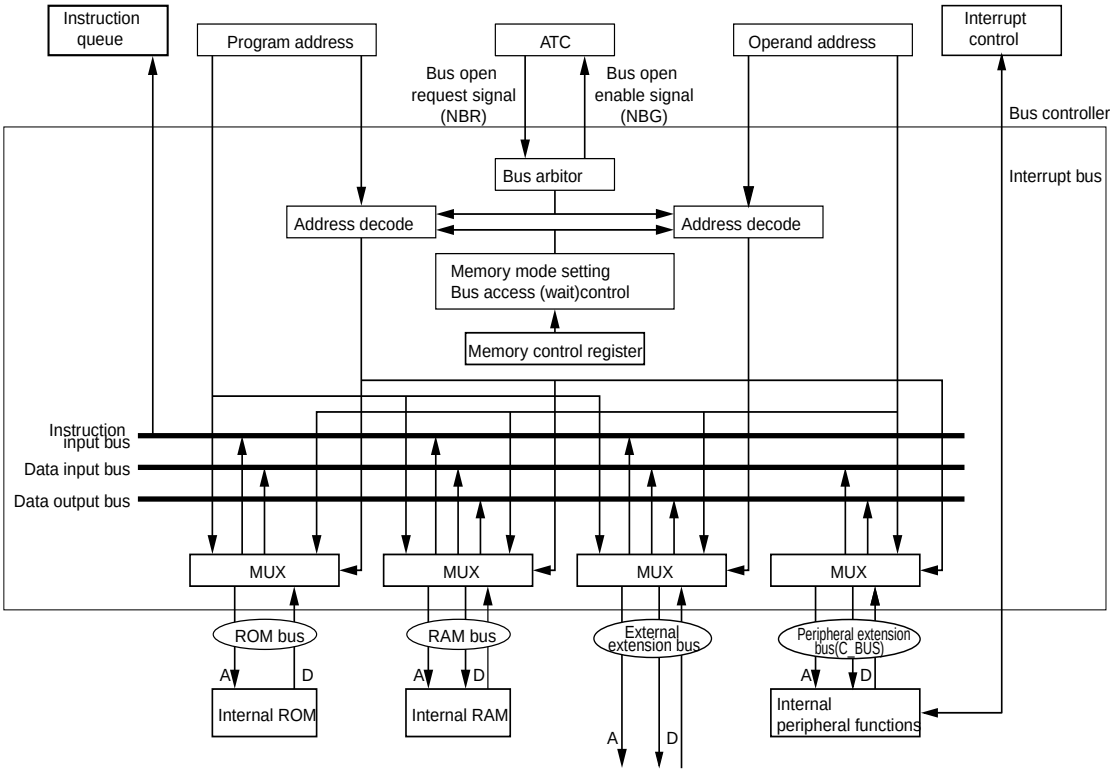


Figure:2.4.1 Functional Block Diagram of the Bus Controller

In memory expansion mode or processor mode, the external expansion bus can access external device. Memory control register (MEMCTR) can be used to select the access mode, B fixed wait cycle mode or B handshake mode. Wait cycle setting to peripheral expansion bus, connected to internal peripheral circuits is available.

2.4.2 Control Registers

Bus interface is controlled by 2 registers : the memory control register (MEMCTR) and the expansion address control register (EXADV).

■ Memory Control Register (MEMCTR)

Table:2.4.1 Memory Control Register (MEMCTR: 0x03F01)

bp	7	6	5	4	3	2	1	0
Flag	IOW1	IOW0	IVBM	EXMEM	EXWH	IRWE	EXW1	EXW0
At reset	1	1	0	0	1	0	1	1
Access	R/W							

bp	Flag	Description
7-6	IOW1 IOW0	Wait cycles when accessing special register area 00: No wait cycles 01: 1 wait cycle 10: 2 wait cycles 11: 3 wait cycles
5	IVBN	Base address setting for interrupt vector table Interrupt vector base = 0x04000 Interrupt vector base = 0x00100
4	EXMEM	Memory expansion mode Do not expand external memory Expand external memory
3	EXWH	Fixed wait cycle mode or handshake mode Handshake mode Fixed wait cycle mode
2	IRWE	Software write enable flag for interrupt request flag Software write disable Even if data is written to each interrupt control (register (xxxICR), the state of the interrupt request flag (xxxIR) will not change.
1-0	EXW1 EXW0	Fixed wait cycles 00: No wait cycles 01: 1 wait cycle 10: 2 wait cycles 11: 3 wait cycles

The EXW1-EXW0 wait settings affect accesses to external devices in the processor mode and memory expansion mode. After reset, MEMCTR specifies the fixed wait cycle mode with three wait cycles.

The IOW1-IOW0 wait settings affect accesses to the special registers located at the addresses 0x3E00-0x3FFF. After reset, MEMCTR specifies the fixed wait cycle mode with three wait cycles. Wait setting of IOW is a function, which CPU supports for special use, for example, when special function register or I/O is expanded to external. For this LSI, wait cycle setting is not always necessary. Select "no-wait cycle" for high performance system construction.

Automatic data trasnsfer function (ATC1) that accesses an external memory cannot be used in processsor mode and memory expansion mode.

To use the automatic data trasnsfer function (ATC1) in processsor mode and memory expansion mode at internal memory setting (internal ROM, internal RAM, special register setting), set the NCS(P74), NRE(P75), NWE(P76) pins to 1 “output” and pull-up.

■ Expansion Address Control Register (EXADV)

Table:2.4.2 Expansion Address Control Register (EXADV: 0x03F0E)

bp	7	6	5	4	3	2	1	0
Flag	EXADV3	EXADV2	EXADV1	-	-	-	-	-
At reset	0	0	0	-	-	-	-	-
Access	R/W							

bp	Flag	Description
7	EXADV3	"A19 to 16" address output during memory expansion mode. 0: General port 1: "A19 to 16" address output
6	EXADV2	"A15 to 12" address output during memory expansion mode. 0: General port 1: "A15 to 12" address output
5	EXADV1	"A11 to 8" address output during memory expansion mode. 0: General port 1: "A11 to 8" address output
4-0	-	-

In memory expansion mode, unused address pins can be used as general ports.

2.4.3 Fixed Wait Cycle Mode

This mode accesses ROM, RAM, or other low-speed devices connected to the external expansion bus by inserting the number of wait cycles specified in the external fixed wait counter (EXW) field of the memory control register (MEMCTR).

Fixed wait cycle mode is used to automatically insert the number of wait cycles specified by the fixed wait counter (EXW1-0) in the MEMCTR.

After reset, MEMCTR specifies the fixed wait cycle to three wait cycles. To change to handshake mode or to use a different number, modify the appropriate bits in MEMCTR.

2.4.4 Handshake Mode

Handshake mode uses the interlock control method in the data transfer sequence , with a transfer enable signals (NRE, NWE) and a data acknowledge signal (NDK).

Handshake mode adjusts the wait cycle for each external device that has a different access speed when the DK generation circuit is provided for each device. CPU of this LSI keeps waiting until the reception of data acknowledge signal to ensure sufficient wait time so that external device can reception data with no error.

During single-chip mode, do not set handshake mode.

Automatic data trasnsfer function (ATC1) that accesses an external memory cannot be used in handshake mode.

■ Access Timing with No Wait Cycles

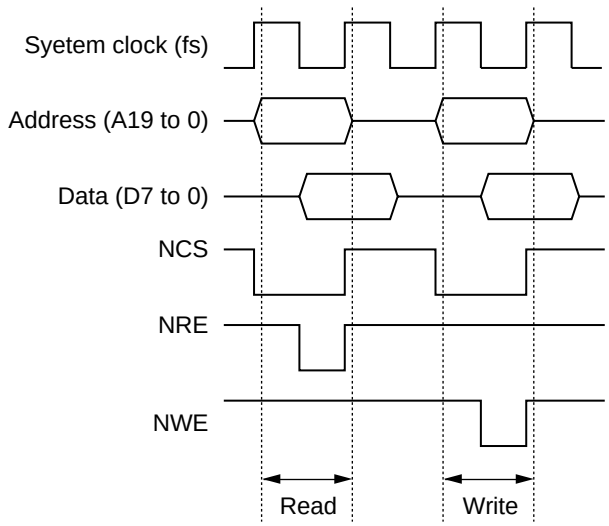


Figure:2.4.2 ROM and RAM Access Timing with No Wait Cycles

■ Access Timing with 1 Wait Cycle

Access timing with 2 or 3 wait cycles follows the same pattern. The latter part of the cycle is extended and the timing is the same.

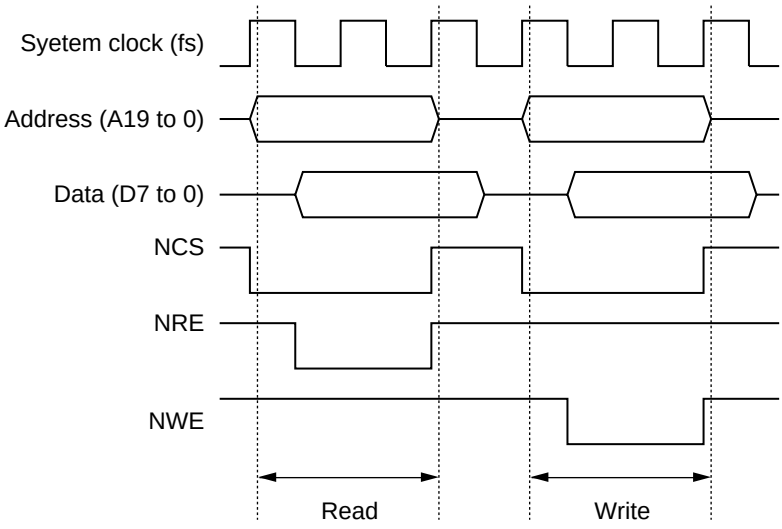


Figure:2.4.3 ROM and RAM Access Timing with 1 Wait Cycle

2.4.5 External Memory Connection Example

■ ROM Connection Example (memory expansion mode)

This example shows connection to 128 KB ROM.

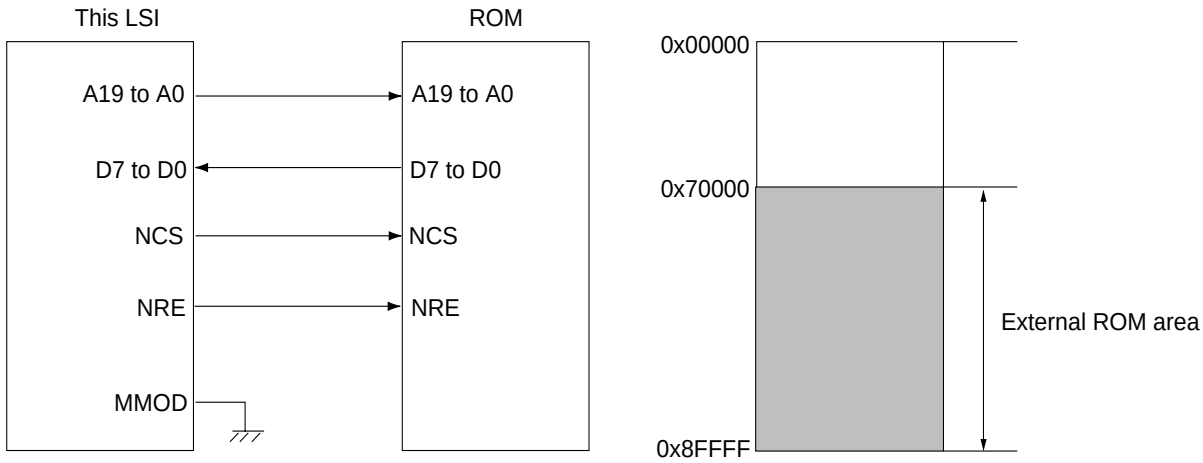


Figure:2.4.4 ROM Connection Example

■ ROM Connection Example (processor mode)

This example shows connection to ROM.

The external expansion RAM area is 0x02F00 to 0x3EFF.

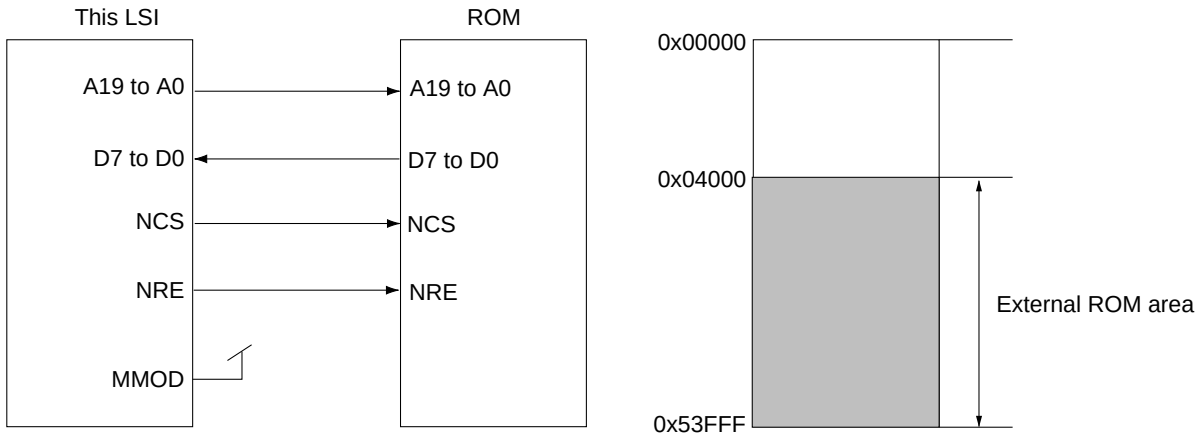


Figure:2.4.5 ROM Connection Example (processor mode)

2.5 Standby Function

2.5.1 Overview

This LSI has two sets of system clock oscillator (high speed oscillation, low speed oscillation) for two CPU operating modes (NORMAL and SLOW), each with two standby modes (HALT and STOP). Power consumption can be decreased with using those modes.

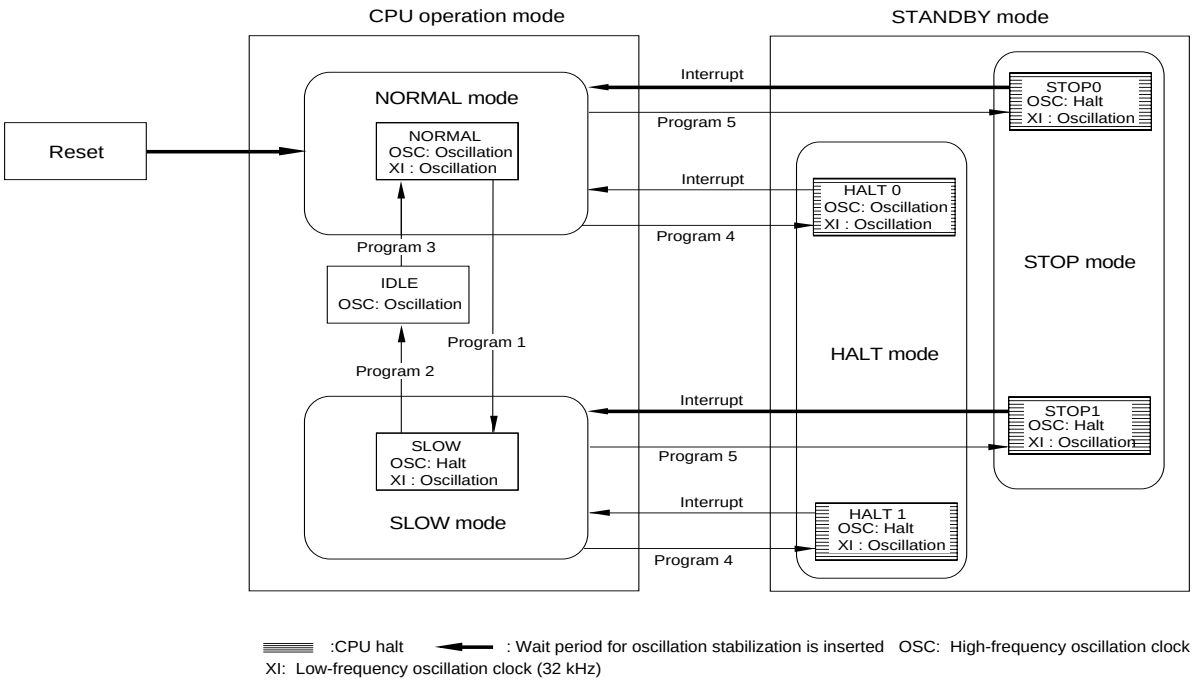


Figure:2.5.1 Transition Between Operation Modes

■ HALT Modes (HALT0, HALT1)

The CPU stops operating. But both of the oscillators remain operational in HALT0 and only the high-frequency oscillator stops operating in HALT1.

An interrupt returns the CPU to the previous CPU operating mode that is, to NORMAL from HALT0 or to SLOW from HALT1.

■ STOP Modes (STOP0, STOP1)

The CPU and both of the oscillators stop operating.

An interrupt restarts the oscillators and, after allowing time for them to stabilize, returns the CPU to the previous CPU operating mode - that is, to NORMAL from STOP0 or to SLOW from STOP1.

■ SLOW Mode

This mode executes the software using the low-frequency clock. Since the high-frequency oscillator is turned off, the device consumes less power while executing the software.

■ IDLE Mode

This mode allows time for the high-frequency oscillator to stabilize when the software is changing from SLOW to NORMAL mode.

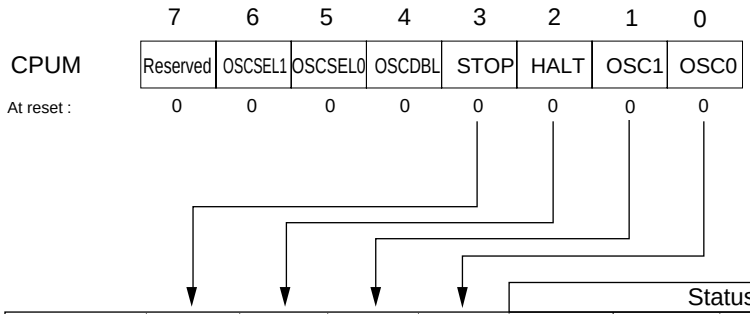
To reduce power dissipation in STOP and HALT modes, it is necessary to check the stability of both the output current from pins and port level of input pins. For output pins, the output level should match the external level or direction control should be changed to input mode. For input pins, the external level should be fixed.

This LSI has two system clock oscillation circuits. OSC is for high-frequency operation (NORMAL mode) and XI is for low-frequency operation (SLOW mode). Transition between NORMAL and SLOW modes or to standby mode is controlled by the CPU mode control register (CPUM). Reset and interrupts are the return factors from standby mode. A wait period is inserted for oscillation stabilization at reset and when returning from STOP mode, but not when returning from HALT mode. High/low-frequency oscillation mode is automatically returned to the same state as existed before entering standby mode.

To stabilize the synchronization at the moment of switching clock speed between high speed oscillation (fosc) and low speed oscillation (fx), fosc should be set to 2.5 times or higher

2.5.2 CPU Mode Control Register

Transition from one mode to another mode is controlled by the CPU mode control register (CPUM).



Operation mode	STOP	HALT	OSC1	OSC0	Status: OSCI /OSCO	Status: XI/XO	Status: System clock	Status: CPU
NORMAL	0	0	0	0	Oscillation	Oscillation	OSCI	Operating
IDLE	0	0	0	1	Oscillation	Oscillation	XI	Operating
SLOW	0	0	1	1	Halt	Oscillation	XI	Operating
HALT0	0	1	0	0	Oscillation	Oscillation	OSCI	Halt
HALT1	0	1	1	1	Halt	Oscillation	XI	Halt
STOP0	1	0	0	0	Halt	Halt	Halt	Halt
STOP1	1	0	1	1	Halt	Halt	Halt	Halt

Figure:2.5.2 Operating Mode and Clock Oscillation (CPUM : 0x3F00)

The procedure for transition from NORMAL to HALT or STOP mode is given below.

(1) If the return factor is a maskable interrupt, set the MIE flag in the PSW to "1" and set the interrupt mask (IM) to a level permitting acceptance of the interrupt.

(2) Clear the interrupt request flag (xxxIR) in the maskable interrupt control register (xxxICR) , set the interrupt enable flag (xxxIE) for the return factor, and set the IE flag in the PSW.

(3) Set CPUM to HALT or STOP mode.

Do not set STANDBY function (STOP, HALT, OSC1 and OSC2 flags) and clock swiching function (OSCDBL, OSCSEL1 and OSCSEL2 flags) at the same time.

Set the IRWE flag of the memory control register (MEMCTR) to clear interrupt request flag by software.

2.5.3 Transition between SLOW and NORMAL

This LSI has two CPU operating modes, NORMAL and SLOW. Transition from SLOW to NORMAL requires passing through IDLE mode.

A sample program for transition from NORMAL to SLOW mode is given below.

```
Program 1
        MOV     x'3',     D0              ; Set SLOW mode.
        MOV     D0, (CPUM)
```

Transition from NORMAL to SLOW mode, when the low-frequency clock has fully stabilized, can be done by writing to the CPU mode control register. In this case, transition through IDLE is not needed.

For transition from SLOW to NORMAL mode, the program must maintain the idle state until high-frequency clock oscillation is fully stable. In IDLE mode, the CPU operates on the low-frequency clock.

For transition from SLOW to NORMAL, oscillation stabilization waiting time is required same as that after reset. Software must count that time. We recommend selecting the oscillation stabilization time after consulting with oscillator manufacturers.

In transition from SLOW to NORMAL, execute following program 1 or 2.
1. Set the clock frequency more than four before transition from SLOW to NORMAL (IDLE state) mode.
2. Use the RAM space for transition from SLOW to NORMAL NORMAL (IDLE state) mode

Sample program for transition from SLOW to NORMAL mode is given below.

```
Program 2
        MOV    x'33',   D
        ADD     D0, (CPUM)
        BNE     x'31',   D0
        SUB     D0, D0
        MOV     D0, (CPUM)
```

Program 3

```
        MOV   x'05',   D0          ; A loop to keep approx. 6.7ms with low-frequency clock (32 kHz)
LOOP    ADD    -1,  D0             ; operation when changed to high-frequency clock (20 MHz).
        BNE    LOOP                ;
        SUB    D0, D0              ;
        MOV   x'30',   D0
        MOV    D0,(CPUM)           ;  Set NORMAL mode.
        MOV   x'00',   D0
        MOV    D0,(CPUM)
```

2.5.4 Transition to STANDBY Modes

The program initiates transitions from a CPU operating mode to the corresponding STANDBY (HALT/STOP) modes by specifying the new mode in the CPU mode control register (CPUM). Interrupts initiate the return to the former CPU operating mode.

Before initiating a transition to a STANDBY mode, however, the program must

(1) Set the maskable interrupt enable flag (MIE) in the processor status word (PSW) to '0' to disable all maskable interrupts temporarily.

(2) Set the interrupt enable flags (xxxIE) in the interrupt control registers (xxxICR) to '1' or '0' to specify which interrupts do and do not initiate the return from the STANDBY mode. Set MIE '1' to enable those maskable interrupts.

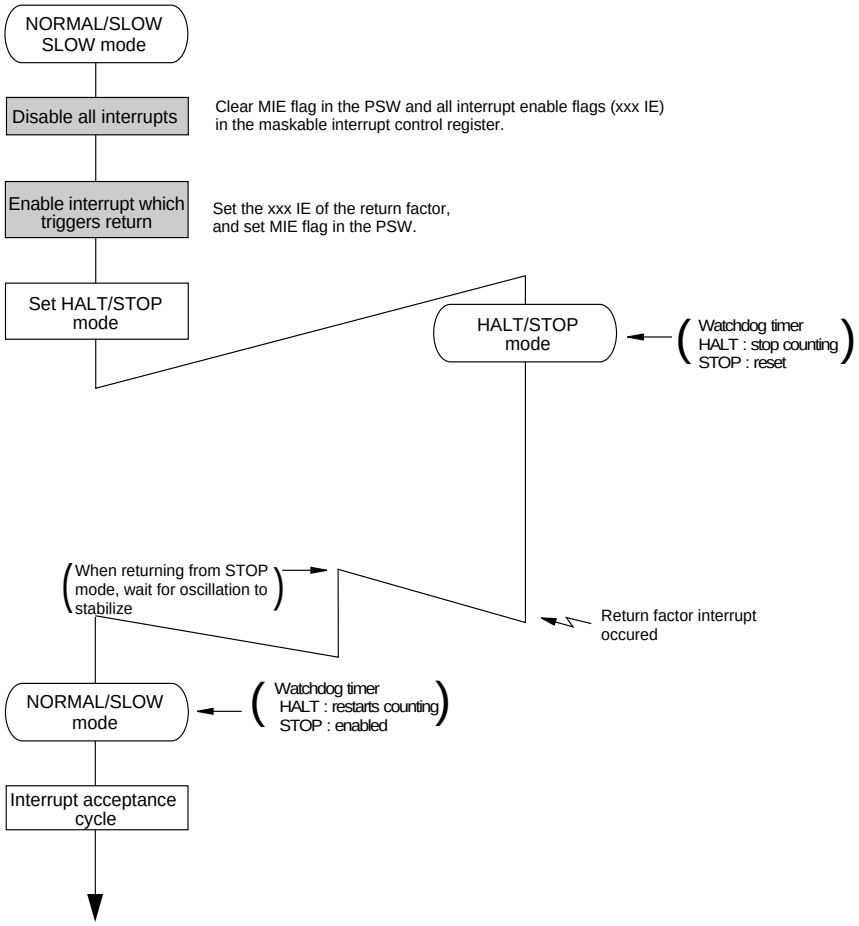


Figure:2.5.3 Transition to/from STANDBY Mode

If the interrupt is enabled but interrupt priority level of the interrupt to be used is not equal to or higher than the mask level in PSW before transition to HALT or STOP mode, it is impossible to return to CPU operation mode by maskable interrupt.

■ Transition to HALT modes

The system transfers from NORMAL mode to HALT0 mode, and from SLOW mode to HALT1 mode. The CPU stops operating, but the oscillators remain operational. There are two ways to leave a HALT mode: a reset or an interrupt. A reset produces a normal reset; an interrupt, an immediate return to the CPU state prior to the transition to the HALT mode. The watchdog timer, if enabled, resumes counting.

```
Program 4
MOV   x'4',   D0                ; Set HALT mode.
MOV   D0,  (CPUM)
NOP                             ; After written in CPUM, some NOP
NOP                             ; instructions (three or less) are
NOP                                   ; executed.
```

■ Transition to STOP mode

The system transfers from NORMAL mode to STOP0 mode, and from SLOW mode to STOP1 mode. In both cases, oscillation and the CPU are both halted. There are two ways to leave a STOP mode: a reset or an interrupt.

```
Program 5
MOV   x'8',   D0                ; Set STOP mode.
MOV   D0,  (CPUM)
NOP                             ; After written in CPUM, some NOP
NOP                             ; instructions (three or less) are
NOP                                   ; executed.
```

Insert three NOP instructions right after the instruction of the transition to HALT, STOP mode.

2.6 Clock Switching

This LSI can select the best operation clock for system by switching clock cycle division factor by program. Division factor is determined by flag of the CPU mode control register (CPUM) . At the highest-frequency, CPU can be operated in the same clock cycle to the external clock hence providing wider operating frequency range.

■ CPU Mode Control Register (CPUM)

Table:2.6.1 CPU Mode Control Register (CPUM : 0x03F00)

bp	7	6	5	4	3	2	1	0
Flag	Reserved	OSCSEL1	OSCSEL0	OSCDBL	STOP	HALT	OSC1	OSC0
At reset	0	0	0	0	0	0	0	0
Access	R/W							

bp	Flag	Description
7	Reserved	Set always to "0" .
6-5	OSCSEL1 OSCSEL0	Clock Frequency 00: 1 01: 4 10: 16 11: 64
4	OSCDBL	Internal System Clock 0: Standard (Input the oscillation clock cycle divided by 2) 1: 2x-speed (Input the oscillation clock cycle)

See Fig. 2.5.2 for setup of bp3-0 flags of the CPU mode control register (CPUM).

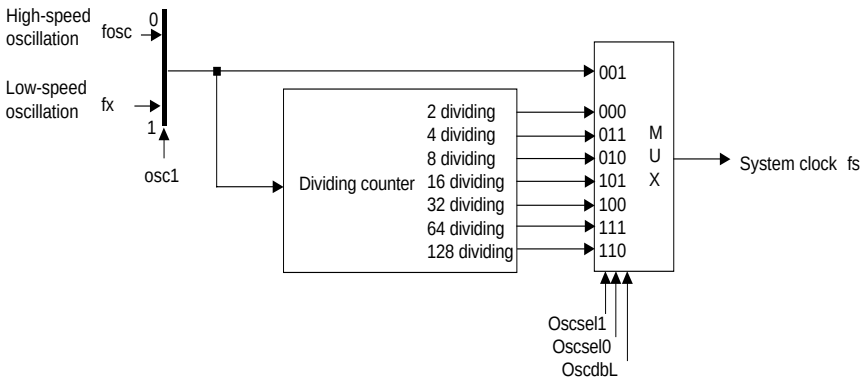


Figure:2.6.1 Clock Switching Circuit

OSCSEL1	OSCSEL0	OSCDBL	Oscillating frequency
0	0	0	2
0	0	1	1
0	1	0	8
0	1	1	4
1	0	0	32
1	0	1	16
1	1	0	128
1	1	1	64

Figure:2.6.2 Setting Division Factor at NORMAL mode by combination of OSCSEL and OSCDBL

Do not set STANDBY function (STOP, HALT, OSC1 and OSC2 flags) and clock swiching function (OSCDBL, OSCSEL1 and OSCSEL2 flags) at the same time.

OSCDBL, OSCSEL1 and OSCSEL0 flags can be set at the same time.

2.7 Reset

2.7.1 Reset operation

The CPU contents are reset and registers are initialized when the NRST pin is pulled to low.

■ Initiating a Reset

There are two methods to initiate a reset.
(1) Drive the NRST pin low.
NRST pin should be held "low" for more than OSC 4 clock cycles (100 ns at a 10 MHz).

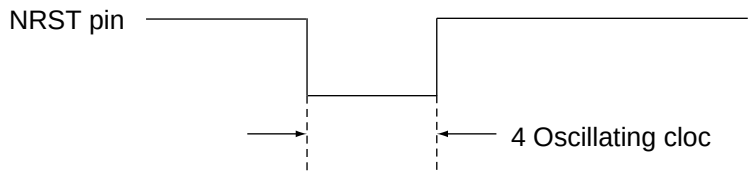


Figure:2.7.1 Minimum Reset Pulse Width

(2) Setting the P2OUT7 flag of the P2OUT register to "0" outputs low level at P27 (NRST) pin. And transferring to reset by program (software reset) can be executed. If the internal LSI is reset and register is initiated, the P2OUT7 flag becomes "1" and reset is released.

This LSI is activated in NORMAL mode in which the base clock is high frequency.

When NRST pin is connected to low power voltage detection circuit that gives pulse for enough low level time at sudeen unconnected. And reset can be generated even if NRST pin is held "low" for less than OSC 4 clock cycles, take notice of noise.

In this LSI, the oscillation (High speed oscillation, Low speed oscillation) is stopped.

■ Sequence at Reset

(1) When reset pin comes to high level from low level, the innternal 14-bit counter (It can be used as watchdog timer, too.) starts its operation by system clock. The period from starting its count from its overflow is called oscillation stabilization wait time.

(2) During reset, internal register and special function register are initiated.

Register	Address	R/W	Description	Initial value
PSW	-		Processor status word	0x00
PC	-		Program counter	Addresss stored in 0x04000
An	-		Address register	undefined
Dn	-		Data register	undefined
CPUM	0x03F00	R/W	CPU mode control register	0x00
MEMCTR	0x03F01	R/W	Memory control register	0xCB
xxxICR	0x03FE2 to 0x03FEF	R/W	Maskable interrupt control register	0x00

(3) After oscillation stabilization wait time, internal reset is released and program is started from the address writen at address 0x4000 at interrupt rector table.

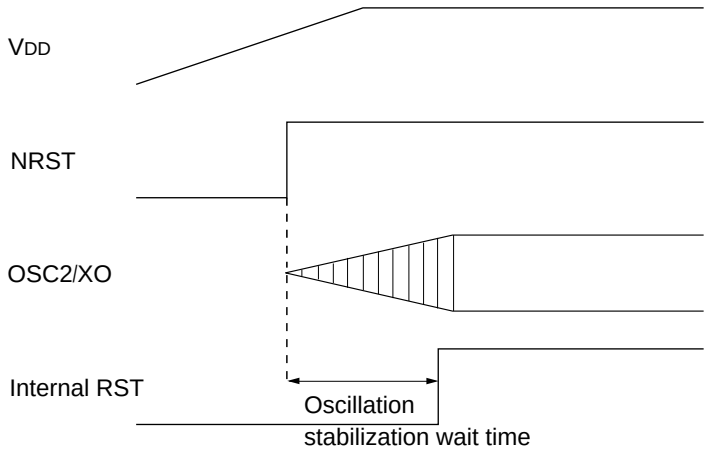


Figure:2.7.2 Reset Released Sequence

The value of internal RAM is uncertain when power is applied to it.
It needs to be initialized before used.

2.7.2 Oscillation Stabilization Wait time

Oscillation stabilization wait time is the period from the stop of oscillation circuit to the stablization for oscillation. Oscillation stabilization wait time is automatically inserted at releasing from reset and at recovering from STOP mode. At recovering from STOP mode the oscillation stabilization wait time control register (DLYCTR) is set to select the oscillation stabilization wait time. At releasing from reset, oscillation stabilization wait time is fixed.
The timer that counts oscillation stabilization wait time is also used as a watchdog timer. That is used as a runaway detective timer at anytime except at releasing from reset and at recovering from STOP mode. Watchdog timer is initiated at reset and at STOP mode and starts counting from the initialize value (0x0000) when system clock (fs) is as clock source. After oscillation stabilization wait time, it continues counting as a watchdog timer.

■ Block Diagram of Oscillation Stabilization Wait Time (watchdog timer)

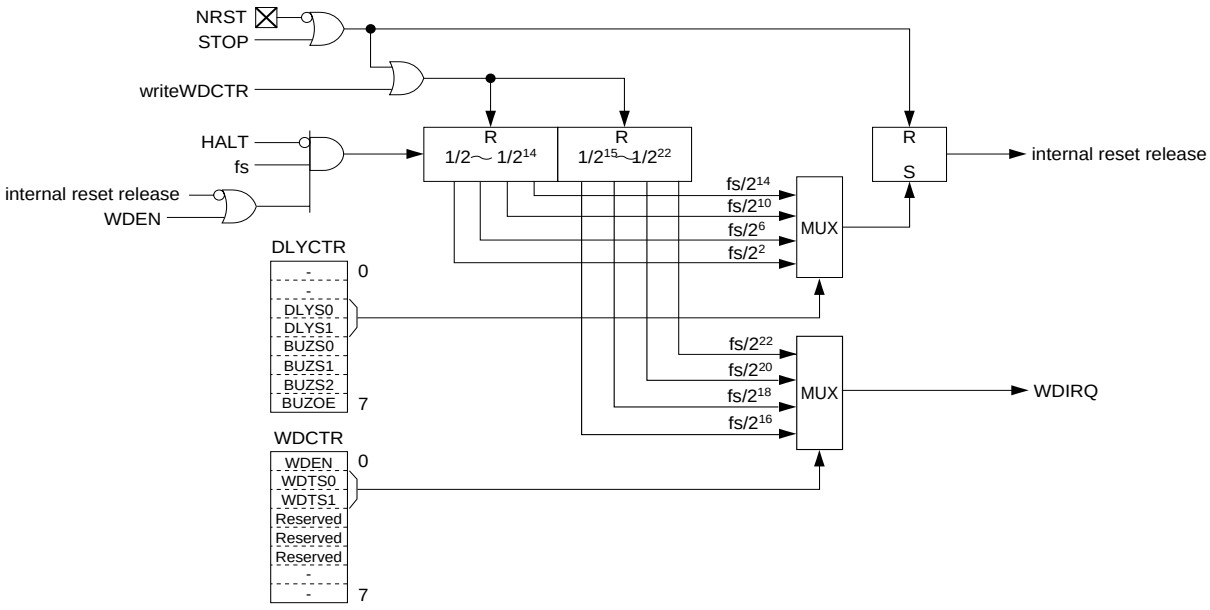


Figure:2.7.3 Block Diagram of Osillation Stabilization Wait Time (watchdog timer)

■ Oscillation Stabilization Wait Time Control Register

Table:2.7.1 Oscillation Stabilization Wait Time Control Register (DLYCTR : 0x03F03)

bp	7	6	5	4	3	2	1	0
Flag	BUZOE	BUZS2	BUZS1	BUZS0	DLYS1	DLYS0	-	-
At reset	0	0	0	0	0	0	-	-
Access	R/W							

bp	Flag	Description
7	BUZOE	Output selection 0: Port data output 1: Buzzer output
6-4	BUZS2 BUZS1 BUZS0	Buzzer output frequency selection 000: fosc/2^{14} 001: fosc/2^{13} 010: fosc/2^{12} 011: fosc/2^{11} 100: fosc/2^{10} 101: fosc/2^{9} 110: fx/2^{4} 111: fx/2^{3}
3-2	DLYS1 DLYS0	Oscillation stabilization wait period selection 00: fs/2^{14} 01: fs/2^{10} 10: fs/2^{6} *1 11: fs/2 *1
1-0	-	-

*1 Do not use in high-speed operation (NORMAL mode).
Use in low-speed operation (SLOW mode).

■ Control the Oscillation Stabilization Wait Time
At recovering from STOP mode, the bit 3-2 (DLYS1, DLYS0) of the oscillation stabilization wait time control register can be set to select the oscillation stabilization wait time from 214, 210, 26, 22 x system clock. The DLYCTR register is also used for controlling of buzzer functions.

At releasing from reset, the oscillation stabilization wait time is fixed to "2^{14} x system clock". System clock is determined by the CPU mode control register (CPUM).

Table:2.7.2 Oscillation Stabilization Wait Time

DLYS1	DLYS0	Oscillation stabilization wait time
0	0	2^{14} x System clock
0	1	2^{10} x System clock
1	0	2^{6} x System clock *1
1	1	2^{2} x System clock *1

*1 Do not use in high-speed operation (NORMAL mode).
Use in low-speed operation (SLOW mode).

Chapter 3 Interrupts

3

3.1 Overview

This LSI speeds up interrupt response with circuitry that automatically loads the branch address to the corresponding interrupt service routine from an interrupt vector table:reset, non-maskable interrupts (NMI), 20 maskable peripheral interrupts, and 6 external interrupts.

For interrupts other than reset, the interrupts processing sequence consists of interrupt request, interrupt acceptance, and hardware processing. After the interrupt is accepted, the program counter (PC) and processor status word (PSW) and handy addressing data (HA) are saved onto the stack. And an interrupts handler ends by restoring, using the POP instruction and other means, the contents of any registers used during processing and then executing the return from interrupt (RTI) instruction to return to the point at which execution was interrupted. Max. 12 machine cycles before execution, and max 11 machine cycles after execution.

Each interrupt has a interrupt control register, which controls the interrupts. Interrupt control register consists of the interrupt level field (LV1 to 0), interrupt enable flag (IE), and interrupt request flag (IR).

Interrupt request flag (IR) is set to “1” by an interrupt request, and cleared to “0” by the interrupt acceptance. This flag is managed by hardware, but can be rewritten by software.

Interrupt enable flag (IE) is the flag that enables interrupts in the group. There is no interrupt enable flag in non-maskable interrupt (NMI). Once this interrupt request flag is set, it is accepted without any conditions. Interrupts enable flag is set in maskable interrupt. Interrupt enable flag of maskable interrupt is valid when the maskable interrupt enable flag (MIE flag) of PSW is “1”.

Maskable interrupts have had vector numbers by hardware, but their priority can be changed by setting interrupts level field. There are three hierarchical interrupt levels. If multiple interrupts have the same priority, the one with the lowest vector number takes priority. Maskable interrupts are accepted when its level is higher than the interrupt mask level (IM1 to 0) of PSW. Non-maskable interrupts are always accepted, regardless of the interrupt mask level.

3.1.1 Functions

Table:3.1.1 Interrupt Functions

Interrupt type	Reset (interrupt)	Non-maskable interrupt	Maskable interrupt
Vector number	0	1	2 to 27
Table address	0x04000	0x04004	0x04008 to 0x0406C
Starting address	Address specified by vector address		
Interrupt level	-	-	Can be set to levels 0 to 2 by software
Interrupt factor	External RST pin input	Errors detection, PI interrupt	External pin input internal peripheral function
Generated operation	Direct input to CPU core	Input to CPU core from non-maskable interrupt control register (NMICR)	Input interrupt request level set in interrupt level flag (xxxL Vn) of maskable interrupt control register (xxxICR) to CPU core.
Accept operation	Always accepts	Always accepts	Acceptance only by the interrupt control of the register (xxxICR) and the interrupt mask level in PSW.
Machine cycles until accepted	12	12	12
PWS status after acceptance	All flags are cleared to “0”	The interrupt mask level flag in PSW is cleared to “00”	Values of the interrupt level flag (xxxLVn) are set to the interrupt mask level (masking all interrupt requests with the same or the lower priority).

3.1.2 Block Diagram

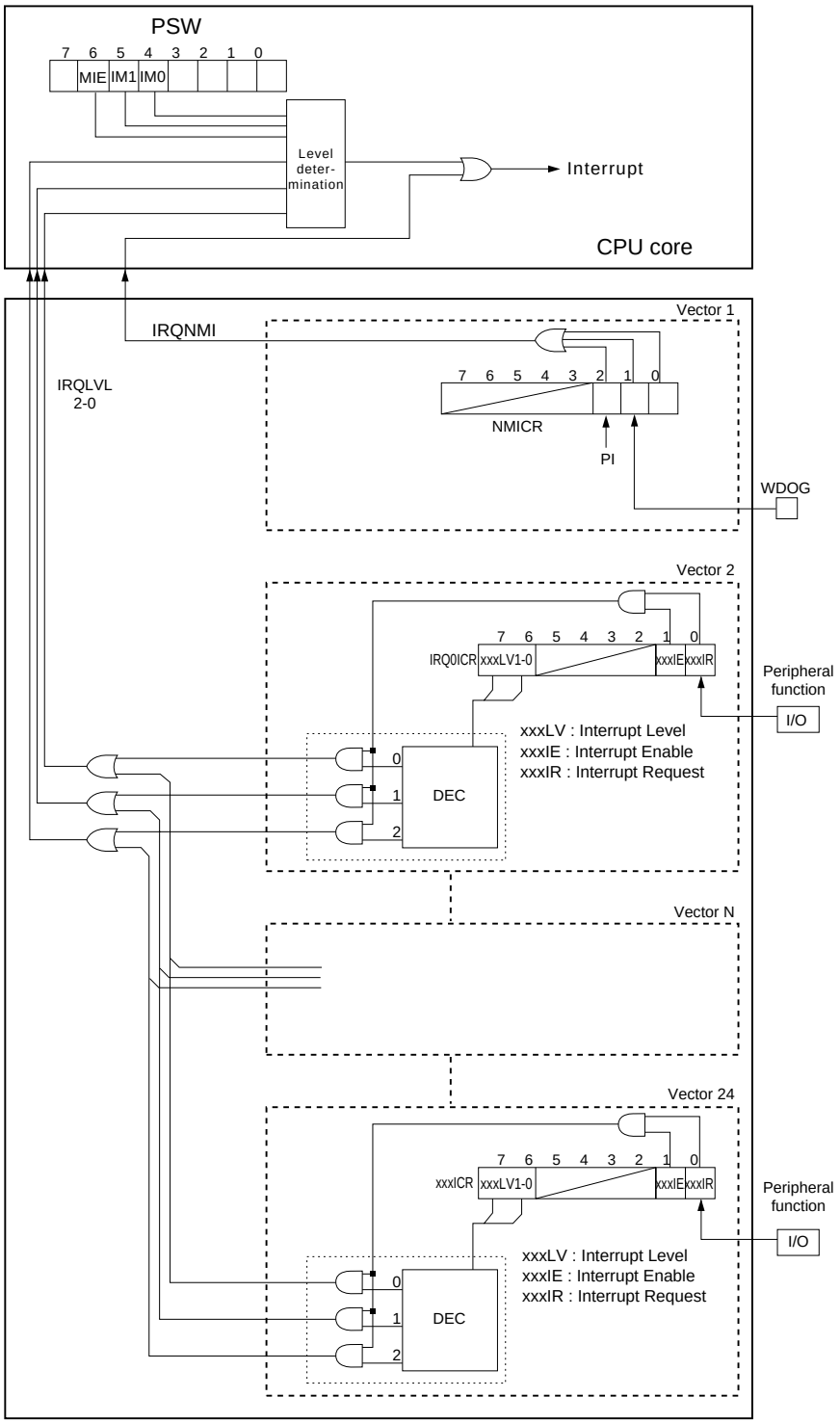


Figure:3.1.1

3.1.3 Operation

■ Interrupt Processing Sequence

For interrupts other than reset, the interrupt processing sequence consists of interrupt request, interrupt acceptance, and hardware processing. The program counter (PC) and processor status word (PSW) and hard addressing data (HA) are saved onto the stack, and program is branched to the address specified by the corresponding interrupt vector. An interrupt handler ends by restoring the contents of any registers used during processing and then executing the return from interrupt (RTI) instruction to return to the point at which execution was interrupted.

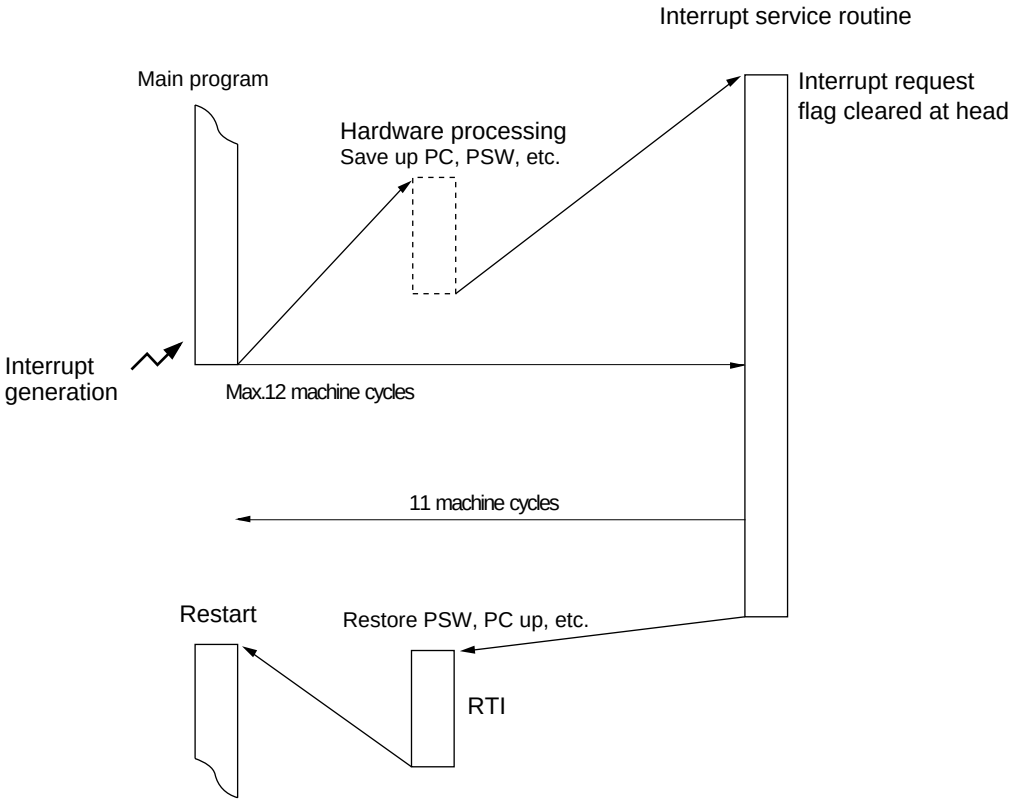


Figure:3.1.2 Interrupt Processing Sequence (maskable interrupts)

■ Interrupt Group and Vector Addresses

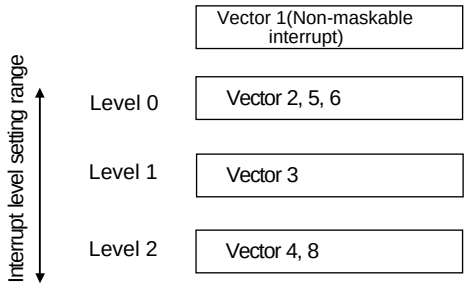
Table:3.1.2 shows the list of interrupt vector addresses and interrupt group.

Table:3.1.2 Interrupt Vector Addresses and Interrupt Group

Vector number	Vector addresses	Interrupt group (interrupt factor)		Control register (address)	
0	0x04000	Reset	-	-	-
1	0x04004	Non-maskable interrupt	NMI	NMICR	0x03FE1
2	0x04008	External interrupt 0	IRQ0	IRQ0ICR	0x03FE2
3	0x0400C	External interrupt 1	IRQ1	IRQ1ICR	0x03FE3
4	0x04010	External interrupt 2	IRQ2	IRQ2ICR	0x03FE4
5	0x04014	External interrupt 3	IRQ3	IRQ3ICR	0x03FE5
6	0x04018	External interrupt 4	IRQ4	IRQ4ICR	0x03FE6
7	0x0401C	External interrupt 5	IRQ5	IRQ5ICR	0x03FE7
8	0x04020	Timer 0 interrupt	TM0IRQ	TM0ICR	0x03FE8
9	0x04024	Timer 1 interrupt	TM1IRQ	TM1ICR	0x03FE9
10	0x04028	Timer 2 interrupt	TM2IRQ	TM2ICR	0x03FEA
11	0x0402C	Timer 3 interrupt	TM3IRQ	TM3ICR	0x03FEB
12	0x04030	Timer 4 interrupt	TM4IRQ	TM4ICR	0x03FEC
13	0x04034	Timer 5 interrupt	TM5IRQ	TM5ICR	0x03FED
14	0x04038	Timer 6 interrupt	TM6IRQ	TM6ICR	0x03FEE
15	0x0403C	Time base interrupt	TBIRQ	TBICR	0x03FEF
16	0x04040	Timer 7 interrupt	TM7IRQ	TM7ICR	0x03FF0
17	0x04044	Timer 7 compare 2 -match interrupt	T7OC2IRQ	T7OC2ICR	0x03FF1
18	0x04048	Serial 0UART reception interrupt	SC0RIRQ	SC0RICR	0x03FF2
19	0x0404C	Serial 0/UART transmission interrupt	SC0TIRQ	SC0TICR	0x03FF3
20	0x04050	Serial 1UART reception interrupt	SC1RIRQ	SC1RICR	0x03FF4
21	0x04054	Serial 1/UART transmission inter-rupt	SC1TIRQ	SC1TICR	0x03FF5
22	0x04058	Serial 2 interrupt	SC2IRQ	SC2ICR	0x03FF6
23	0x0405C	Serial 3 interrupt	SC3IRQ	SC3ICR	0x03FF7
24	0x04060	Serial 4UART reception interrupt	SC4RIRQ	SC4RICR	0X03FF8
25	0x04064	Serial 4/UART transmission interrupt	SC4TIRQ	SC4TICR	0X03FF9
26	0x04068	A/D conversion interrupt	ADIRQ	ADICR	0X03FFA
27	0x0406C	ATC1 interrupt	ATC1IRQ	ATC1IRC	0X03FFB

■ Interrupt Level and Priority

This LSI allocated vector numbers and interrupt control registers (except reset interrupt) to each interrupt. The interrupt level (except reset interrupt, non-maskable interrupt) can be set by software, per each interrupt group. There are three hierarchical interrupt levels. If multiple interrupts have the same priority, the one with the lowest vector number takes priority. For example, if a vector 3 set to level 1 and a vector 4 set to level 2 request interrupt simultaneously, vector 3 will be accepted.



Priority	Interrupt vector No.
1	Vector 1
2	Vector 2
3	Vector 5
4	Vector 6
5	Vector 3
6	Vector 4
7	Vector 8

Figure:3.1.3 Interrupt Priority Outline

■ Determination of Interrupt Acceptance

The following is the procedure from interrupt request input to acceptance.

1. The interrupt request flag (xxxR) in the corresponding external interrupt control register (IRQnICR) and internal interrupt control register (xxxICR) are set to “1”.
2. An interrupt request is input to the CPU. (If the interrupt enable flag (xxxIE) of the same register is “1”.)
3. The interrupt request signal is set for each interrupt. The interrupt level (IL) is input to the CPU.
4. The interrupt request is accepted. (If IL has higher priority than IM and MIE is “1”.)
5. Acceptance of an interrupt does not reset the corresponding interrupt enable flag (xxxIE) to “0”.

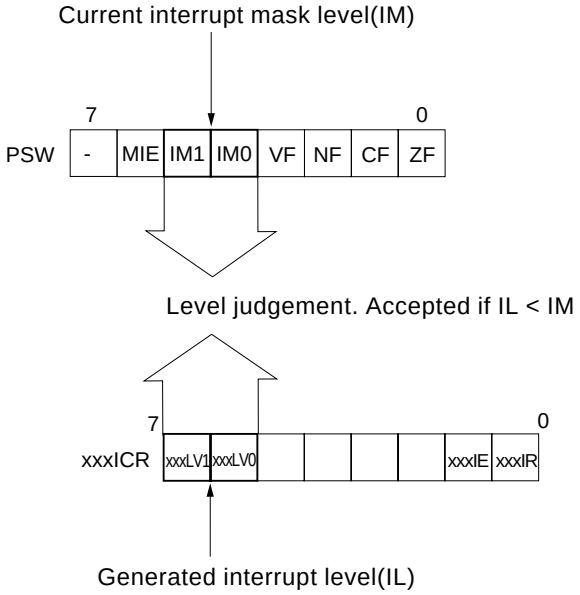


Figure:3.1.4 Determination of Interrupt Acceptance

Acceptance of an interrupt does not reset the corresponding interrupt enable flag (xxxIE) to “0”.

MIE = “0” and interrupts are disabled when:

- MIE of the PSW is set to “0” by a program and when BE instruction is executed. (BKD is reset and MIE is set)
- Reset is input.

MIE = “1” and interrupts are enabled when:

- MIE of the PSW is set to “1” by a program, and BD instruction is executed. (BKD is set and MIE is set)

The interrupt mask level (IM1-0) in the processor status word (PSW) changes when:

- The program alters it directly,
- A reset initializes it to 0 (00b),
- Maskable interrupt is accepted (the interrupt level becomes the interrupt mask level).
- Execution of the RTI instruction at the end of an interrupt service routine restores the processor status word (PSW) and thus the previous interrupt mask level.

The MN101C series does not reset the maskable interrupt enable (MIE) flag of the processor status word (PSW) to “0” when accepting interrupts.

Non maskable interrupt is prior to maskable interrupt when they are generated at the same time.

Non-maskable interrupts have priority over maskable ones.
Refer to appendices(19.1 Instruction set) for BE instruction and BD instruction.

■ Interrupt Acceptance Operation

When accepting an interrupt, this LSI hardware saves the handy address register, the return address from the program counter, and the processor status word (PSW) to the stack and branches program to the interrupt handler using the starting address in the vector table. The following is the hardware processing sequence invoked by interrupt acceptance.

1. the stack pointer (SP) is updated.
   (SP-6) ⟶ (SP)
2. The contents of the handy address register (HA) are saved to the stack.
   Upper half of HA ⟶ (SP + 5)
   Lower half of HA ⟶ (SP + 4)
3. The contents of the program counter (PC) -i.e., the return address- are saved to the stack.
   PC bits 19-16, H ⟶ (SP + 3)
   PC bits 15-8 ⟶ (SP + 2)
   PC bits 7-0 ⟶ (SP + 1)
4. The contents of the PSW are saved to the stack.
   PSW ⟶ (SP)
5. The interrupt level (xxxLVn) for the interrupt is copied to the interrupt mask (IMn) in the PSW.
   Interrupt level (xxxLVn) ⟶ IMn
6. BKD flag of the PSW is reset. (During interrupt acceptance, bank register always address the first 64KB. The bank register can be rewritten.)
7. The hardware branches program to the address in the vector table.

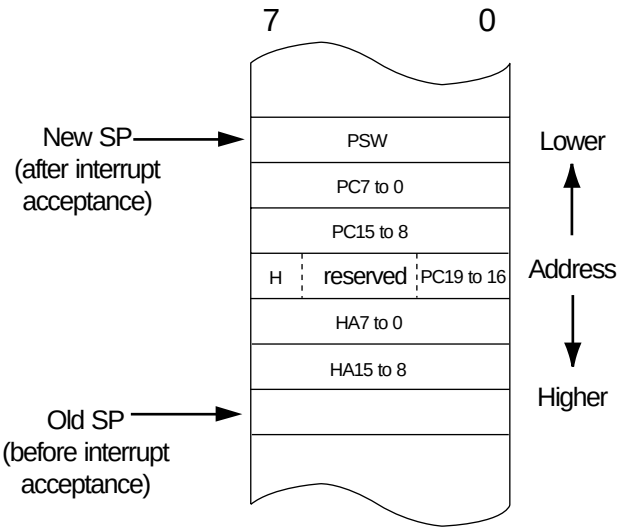


Figure:3.1.5 Stack Operation during Interrupt Acceptance

■ Interrupt Return Operation

An interrupt handler ends by restoring the contents of any registers saved to the stack during processing by the POP instruction and other means, and the RTI instruction restores the program to the point at execution was interrupted.

The following is the processing sequence invoked by the RTI instruction.

1. The contents of the PSW are restored from the stack. (SP)
2. The contents of the program counter (PC) -i.e., then return address- are restored from the stack. (SP + 1 to SP + 3)
3. The contents of the handy address register (HA) are restored from the stack. (SP + 4, SP+ 5)
4. The stack pointer is updated. (SP +6 $\rightarrow$ SP)
5. Execution branches program to the address in the program counter.

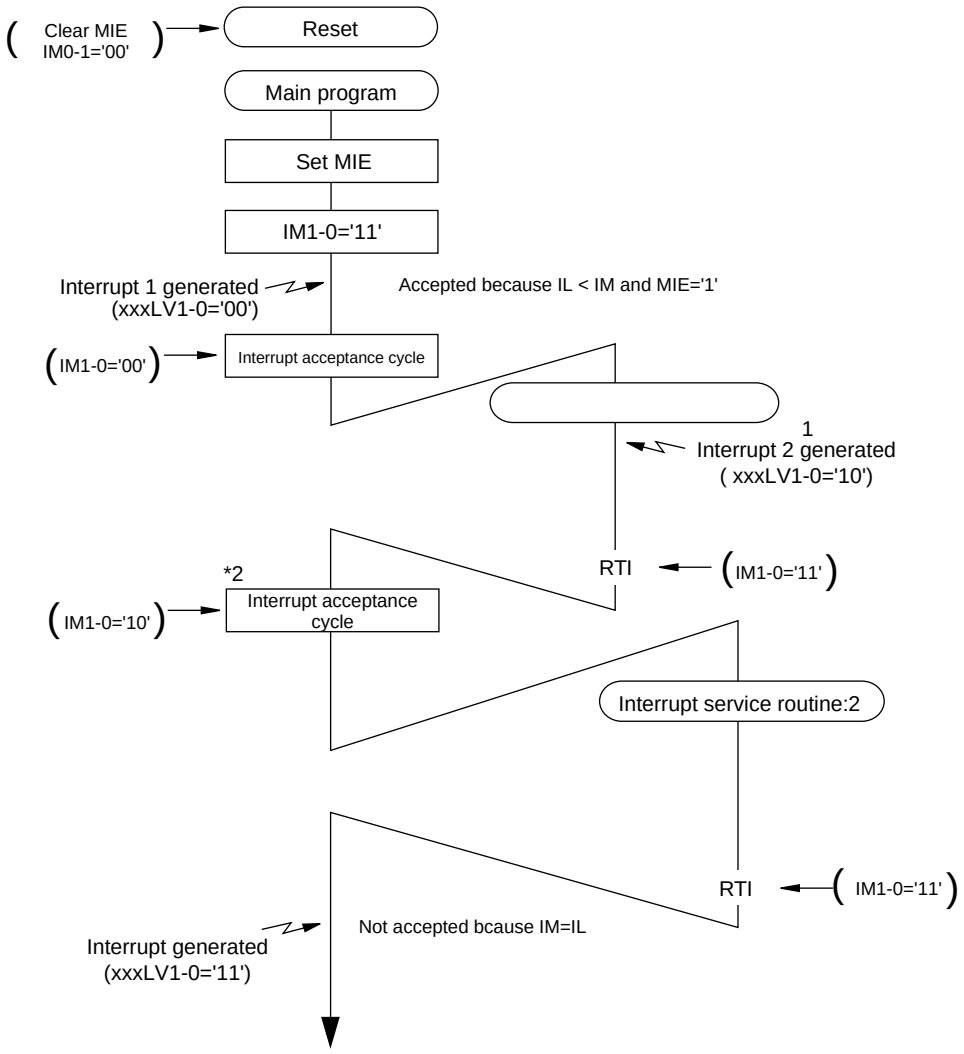
The handy address register is an internal register used by the handy addressing function. The hardware saves its contents to the stack to prevent the interrupt from interfering with operation of the function.

Registers such as data register, or address register are not saved, so that PUSH instruction from program should be used to save them onto stack, if necessary.

The address bp6 to bp4, when program counter (PC19-16,H) are saved to the stack, are reserved. Do not change it by program.

■ Maskable Interrupt

Figure 3-1-6 shows the processing flow when a second interrupt with a lower priority level (xxxLV1 - xxxLV0 = “10”) arrives during the processing of the with a higher priority level (xxxLV1 - xxxLV0 = “00”).



Parentheses ( ) indicates hardware processing.

*1 If during the processing of the first interrupt, an interrupt request with an interrupt level (IL) numerically lower than the interrupt mask (IM) arrives, it is accepted as a nested interrupt. If IL > IM, however, the interrupt is not accepted.
*2 The second interrupt, postponed because its interrupt level (IL) was numerically greater than the interrupt mask (IM) for the first interrupt service routine, is accepted when the first interrupt handler returns.

Figure:3.1.6 Processing Sequence for Maskable Interrupts

■ Multiplex Interrupt of Maskable Interrupt

When this LSI accepts an interrupt, it automatically disables acceptance of subsequent interrupts with the same or lower priority level. When the hardware accepts an interrupt, it copies the interrupt level (xxxLVn) for the interrupt to the interrupt mask (IM) in the PSW. As a result, subsequent interrupts with the same or lower priority levels are automatically masked. Only interrupts with higher priority levels are accepted. The net result is that interrupts are normally processed in decreasing order of priority. It is, however, possible to alter this arrangement.

1. To disable interrupt nesting
    - Reset the MIE bit in the PSW to “0”.
    - Raise the priority level of the interrupt mask (IM) in the PSW.
2. To enable interrupts with lower priority than the currently accepted interrupt
    - Lower the priority level or the interrupt mask (IM) in the PSW.

Multiplex interrupts are only enables for interrupts with levels higher than the PSW interrupt mask level (IM).

It is possible to forcibly rewrite IM to accept an interrupt with a priority lower than the interrupt being processed, but the careful of stack overflow.

Do not operate the maskable interrupt control register (xxxICR) when multiple interrupts are enabled. If operation is necessary, first clear the PSW MIE flag.

■ Multiple Interrupt of Non-maskable

On the acceptance of nim interrupt, when other nmi interrupt factor is generated, this interrupt is processed right away. Also, when the same nmi interrupt factor is generated before nmi interrupt flag is be soft cleared, it is not accepted. (Unless nmi interrupt clears the flag by the soft, the following same nmi interrupt is not accepted and valid.)

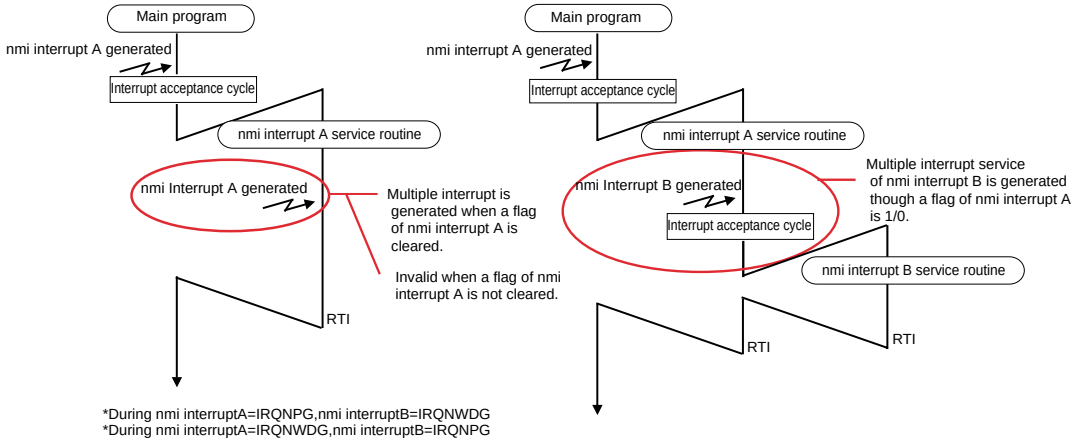

Main program
nmi interrupt A generated
Interrupt acceptance cycle
nmi interrupt A service routine
nmi Interrupt A generated
Multiple interrupt is generated when a flag of nmi interrupt A is cleared.
Invalid when a flag of nmi interrupt A is not cleared.
RTI
Main program
nmi interrupt A generated
Interrupt acceptance cycle
nmi interrupt A service routine
nmi Interrupt B generated
Multiple interrupt service of nmi interrupt B is generated though a flag of nmi interrupt A is 1/0.
Interrupt acceptance cycle
nmi interrupt B service routine
RTI
RTI
*During nmi interruptA=IRQNPG,nmi interruptB=IRQNWDG
*During nmi interruptA=IRQNWDG,nmi interruptB=IRQNPG

Figure 3-1-7 shows the processing sequence of the multiple interrupt.
(multiple interrupt:xxxLV1 to 0 = “10”, xxxLV1 to 0 = “00”)

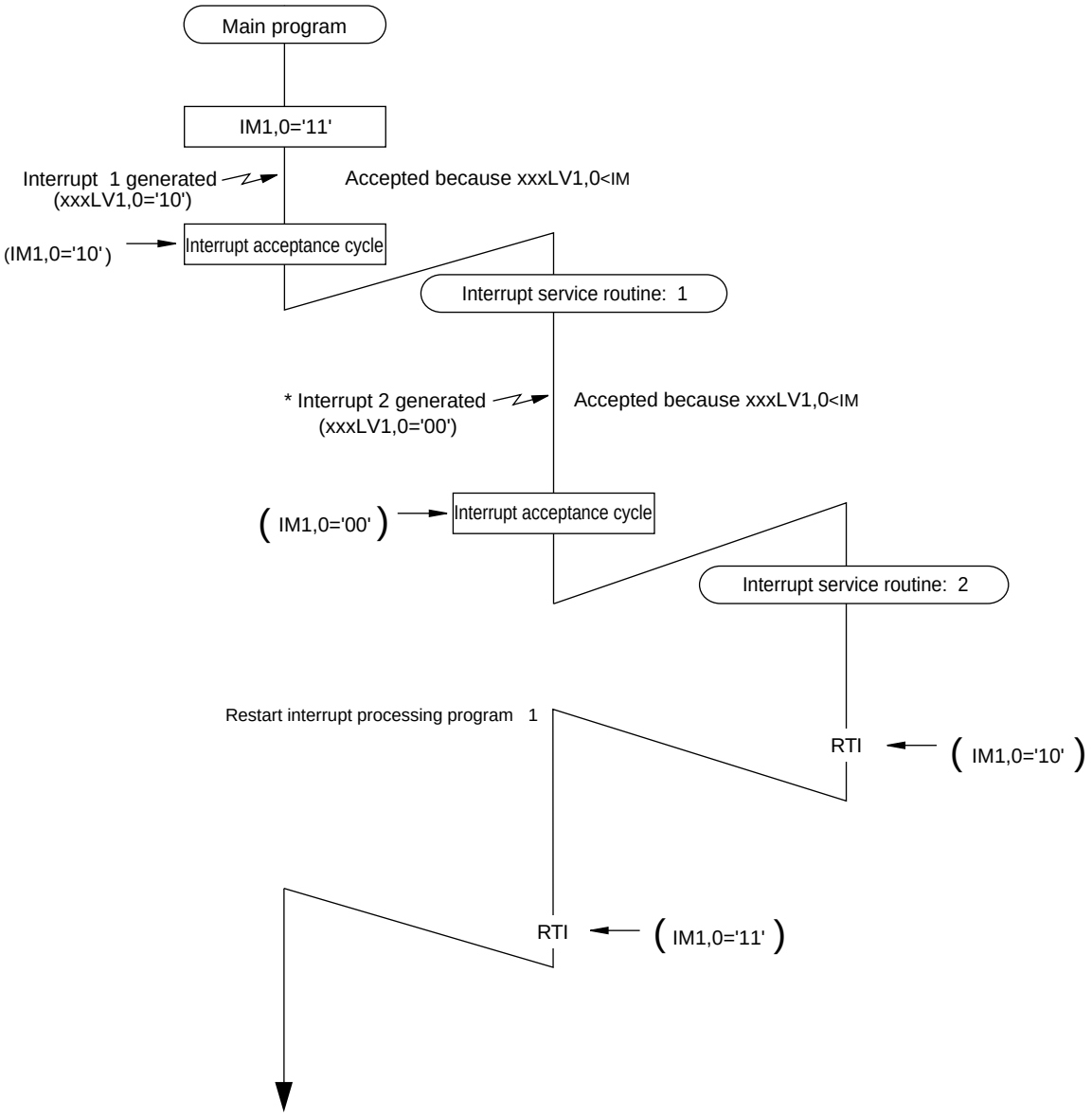


Figure:3.1.7 Processing Sequence for Non-Maskable Multiple Interrupt

3.1.4 Interrupt Flag Setup

■ Interrupt Request Flag (IR) Setup by the Software

The interrupt request flag is operated by the hardware. That is set to “1” when any interrupt factor is generated, and cleared to “0” when the interrupt is accepted. If you want to operate it by the software, the IRWE flag of MEMCTR should be set to “1”.

■ Interrupt Flag Setup Procedure

A setup procedure of the interrupt request flag set by the hardware and the software shows as follows;

Setup Procedure	Description
(1)Disable all maskable interrupts. PSW bp6:MIE =0	(1)Clear the MIE flag of PSW to disable all maskable interrupts. This is necessary, especially when the interrupt control register is changed.
(2)Select the interrupt factor.	(2)Select the interrupt doctor such as interrupt edge selection, or timer interrupt cycle change.
(3)Enable the interrupt request flag to be rewritten. MEMCTR(0x03F01) bp2:IRWE =1	(3)Set the IRWE flag of MEMCTR to enable the interrupt request flag to be rewritten. This is necessary only when the interrupt request flag is changed by the software.
(4)Rewrite the interrupt request flag. xxxICR bp0:xxxIR	(4)Rewrite the interrupt request flag (xxxIR) of the interrupt control register (xxxICR).
(5)Disable the interrupt request flag to be rewritten. MEMCTR(0x) bp2:IRWE =0	(5)Clear the IRWE flag so that interrupt request flag can not be rewritten by the software.
(6)Set the interrupt level. xxxICR bp7-6:xxxLV1-0 PSW bp5-4:IM1-0	(6)Set the interrupt level by the xxxLV1 - 0 flag of the interrupt control register (xxxICR). Set the IM1 - 0 flag of PSW then the interrupt acceptance level of CPU should be changed.
(7)Enable the interrupt. xxxICR bp1:xxxIE =1	(7)Set the xxxIE flag of the interrupt control register (xxxICR) to enable the interrupt.
(8)Enable all maskable interrupts. PSW bp6:MIE =1	(8)Set the MIE flag of PSW to enable maskable interrupts.

3.2 Control Registers

3.2.1 Registers List23

Table:3.2.1 Interrupt Control Registers

Register	Address	R/W	Functions	Page
NMICR	0x03FE1	R/W	Non-maskable interrupt control register	III-19
IRQ0ICR	0x03FE2	R/W	External interrupt 0 control register	III-20
IRQ1ICR	0x03FE3	R/W	External interrupt 1 control register	III-21
IRQ2ICR	0x03FE4	R/W	External interrupt 2 control register	III-22
IRQ3ICR	0x03FE5	R/W	External interrupt 3 control register	III-23
IRQ4ICR	0x03FE6	R/W	External interrupt 4 control register	III-24
IRQ5ICR	0x03FE7	R/W	External interrupt 5 control register	III-25
TM0ICR	0x03FE8	R/W	Timer 0 interrupt control register (Timer 0 compare-match)	III-26
TM1ICR	0x03FE9	R/W	Timer 1 interrupt control register (Timer 1 compare-match)	III-27
TM2ICR	0x03FEA	R/W	Timer 2 interrupt control register (Timer 2 compare-match)	III-28
TM3ICR	0x03FEB	R/W	Timer 3 interrupt control register (Timer 3 compare-match)	III-29
TM4ICR	0x03FEC	R/W	Timer 4 interrupt control register (Timer 4 compare-match)	III-30
TM5ICR	0x03FED	R/W	Timer 5 interrupt control register (Timer 5 compare-match)	III-31
TM6ICR	0x03FEE	R/W	Timer 6 interrupt control register (Timer 6 compare-match)	III-32
TBICR	0x03FEF	R/W	Time base interrupt control register (Time base period)	III-33
TM7ICR	0x03FF0	R/W	Timer 7 interrupt control register (Timer 7 compare-match)	III-34
T7OC2ICR	0x03FF1	R/W	Timer 7 compare register 2-match interrupt control register	III-35
SC0RICR	0x03FF2	R/W	Serial 0 UART reception interrupt control register (SC0UART reception completion)	III-36
SC0TICR	0x03FF3	R/W	Serial 0/UART transmission interrupt control register (SC0UART transmission completion)	III-37
SC1RICR	0x03FF4	R/W	Serial 1 UART reception interrupt control register (SC1UART reception completion)	III-38
SC1TICR	0x03FF5	R/W	Serial 1/UART transmission interrupt control register (SC1UART transmission completion)	III-39
SC2ICR	0x03FF6	R/W	Serial 2 interrupt control register (SC2 transfer completion)	III-40
SC3ICR	0x03FF7	R/W	Serial 3 interrupt control register (SC3 transfer completion)	III-41
SC4RICR	0x03FF8	R/W	Serial 4 UART reception interrupt control register (SC4UART reception completion)	III-42

SC4TICR	0x03FF9	R/W	Serial 4/UART transmission interrupt control register (SC4UART transmission completion)	III-43
ADICR	0x03FFA	R/W	A/D conversion interrupt control register (A/D conversion completion)	III-44
ATC1ICR	0x03FFB	R/W	ATC1 interrupt control register (ATC1 transmission completion)	III-45

If the interrupt level flag (xxxLVn) is set to “level 3”, its vector is disabled, regardless of interrupt enable flag and interrupt request flag.

Writing to the interrupt control register should be done after that all maskable interrupts are set to be disable by the MIE flag of the PSW register.

3.2.2 Interrupt Control Registers

The interrupt control registers include the non-maskable interrupt control register (NMICTR), the external interrupt control register and the internal interrupt control registers (xxxICR).

■ Non-maskable Interrupt Control Register (NMICR:0x03FE1)

The non-maskable interrupt control register (NMICR) is stored the non-maskable interrupt request. When the non-maskable interrupt request is generated, the interrupt is accepted regardless of the interrupt mask level (IMn) of PSW. The hardware then branches program to the address stored at location 0x04004 in the interrupt vector table. The watchdog timer overflow interrupt request flag (IRQNWDG) is set to “1” when the watchdog timer overflows. The program interrupt request flag (IRQNPG) is set to “1” when the undefined instruction is executed. Setting PIR or WDIR flag to be “1” enable non-maskable interrupt request to be set compulsory.

Table:3.2.2 Non-maskable Interrupt Control Register (NMICR:0x03FE1)

bp	7	6	5	4	3	2	1	0
Flag	-	-	-	-	-	IRQNPG	IRQNWDG	Reserved
At reset	-	-	-	-	-	0	0	0
Access	R/W							

bp	Flag	Description
7-6	-	-
2	IRQNPG	Program interrupt request flag 0:No interrupt request 1:Interrupt request generated
1	IRQNWDG	Watchdog interrupt request flag 0:No interrupt request 1:Interrupt request generated
0	Reserved	Set always to “0”

When the undefined instruction is going to be executed, this LSI generates the non-maskable interrupt at the same time of the setting of the program interrupt request flag IRQNPG. When the setting of the IRQNPG flag is confirmed by the non-maskable interrupt process program, the softreset is recommended by outputting “0” to the reset pin (P27).

■ External Interrupt 0 Control Register (IRQ0ICR)

The external interrupt 0 control register (IRQ0ICR) controls interrupt level of the external interrupt 0, valid edge, interrupt enable and interrupt request. Interrupt control register should be operated when the maskable interrupt enable flag (MIE) of PSW is “0”.

Table:3.2.3 External Interrupt 0 Control Register (IRQ0ICR:0x03FE2)

bp	7	6	5	4	3	2	1	0
Flag	IRQ0LV1	IRQ0LV0	REDG0	-	-	-	IRQ0IE	IRQ0IR
At reset	0	0	0	-	-	-	0	0
Access	R/W							

bp	Flag	Description
7-6	IRQ0LV1 IRQ0LV0	External interrupt level flag The CPU has interrupt levels from 0 to 3. This flag sets the interrupt level for interrupt requests.
5	REDG0	External interrupt valid edge flag (at the standby mode) 0:Falling edge 1:Rising edge
4-2	-	-
1	IRQ0IE	External interrupt enable flag 0:Disable interrupt 1:Enable interrupt
0	IRQ0IR	External interrupt request flag 0:No interrupt request 1:Interrupt request generated

■ External Interrupt 1 Control Register (IRQ1ICR)

The external interrupt 1 control register (IRQ1ICR) controls interrupt level of external interrupt 1, valid edge, interrupt enable and interrupt request. Interrupt control register should be operated when the maskable interrupt enable flag (MIE) of PSW is “0”.

Table:3.2.4 External Interrupt 1 Control Register (IRQ1ICR:0x03FE3)

bp	7	6	5	4	3	2	1	0
Flag	IRQ1LV1	IRQ1LV0	REDG1	-	-	-	IRQ1IE	IRQ1IR
At reset	0	0	0	-	-	-	0	0
Access	R/W							

bp	Flag	Description
7-6	IRQ1LV1 IRQ1LV0	External interrupt level flag The CPU has interrupt levels from 0 to 3. This flag sets the interrupt level for interrupt requests.
5	REDG1	External interrupt valid edge flag 0:Falling edge 1:Rising edge
4-2	-	-
1	IRQ1IE	External interrupt enable flag 0:Disable interrupt 1:Enable interrupt
0	IRQ1IR	External interrupt request flag 0:No interrupt request 1:Interrupt request generated

■ External Interrupt 2 Control Register (IRQ2ICR)

The external interrupt 2 control register (IRQ2ICR) controls interrupt level of external interrupt 2, valid edge, interrupt enable and interrupt request. Interrupt control register should be operated when the maskable interrupt enable flag (MIE) of PSE is “0”.

Table:3.2.5 External Interrupt 2 Control Register (IRQ2ICR:0x03FE4)

bp	7	6	5	4	3	2	1	0
Flag	IRQ2LV1	IRQ2LV0	REDG2	-	-	-	IRQ2IE	IRQ2IR
At reset	0	0	0	-	-	-	0	0
Access	R/W							

bp	Flag	Description
7-6	IRQ2LV1 IRQ2LV0	External interrupt level flag The CPU has interrupt levels from 0 to 3. This flag sets the interrupt level for interrupt requests.
5	REDG2	External interrupt valid edge flag 0:Falling edge 1:Rising edge
4-2	-	-
1	IRQ2IE	External interrupt enable flag 0:Disable interrupt 1:Enable interrupt
0	IRQ2IR	External interrupt request flag 0:No interrupt request 1:Interrupt request generated

■ External Interrupt 3 Control Register (IRQ3ICR)

The external interrupt 3 control register (IRQ3ICR) controls interrupt level of external interrupt 3, valid edge, interrupt enable and interrupt request. Interrupt control register should be operated when the maskable interrupt enable flag (MIE) of PSE is “0”.

Table:3.2.6 External Interrupt 3 Control Register (IRQ3ICR:0x03FE5)

bp	7	6	5	4	3	2	1	0
Flag	IRQ3LV1	IRQ3LV0	REDG3	-	-	-	IRQ3IE	IRQ3IR
At reset	0	0	0	-	-	-	0	0
Access	R/W							

bp	Flag	Description
7-6	IRQ3LV1 IRQ3LV0	External interrupt level flag The CPU has interrupt levels from 0 to 3. This flag sets the interrupt level for interrupt requests.
5	REDG3	External interrupt valid edge flag 0:Falling edge 1:Rising edge
4-2	-	-
1	IRQ3IE	External interrupt enable flag 0:Disable interrupt 1:Enable interrupt
0	IRQ3IR	External interrupt request flag 0:No interrupt request 1:Interrupt request generated

■ External Interrupt 4 Control Register (IRQ4ICR)

The external interrupt 4 control register (IRQ4ICR) controls interrupt level of external interrupt 4, valid edge, interrupt enable flag and interrupt request. Interrupt control register should be operated when the maskable interrupt enable flag (MIE) of PSW is “0”.

Table:3.2.7 External Interrupt 4 Control Register (IRQ4ICR:0x03FE6)

bp	7	6	5	4	3	2	1	0
Flag	IRQ4LV1	IRQ4LV0	REDG4	-	-	-	IRQ4IE	IRQ4IR
At reset	0	0	0	-	-	-	0	0
Access	R/W							

bp	Flag	Description
7-6	IRQ4LV1 IRQ4LV0	External interrupt level flag The CPU has interrupt levels from 0 to 3. This flag sets the interrupt level for interrupt requests.
5	REDG4	External interrupt valid edge flag 0:Falling edge 1:Rising edge
4-2	-	-
1	IRQ4IE	External interrupt enable flag 0:Disable interrupt 1:Enable interrupt
0	IRQ4IR	External interrupt request flag 0:No interrupt request 1:Interrupt request generated

■ External Interrupt 5 Control Register (IRQ5ICR)

The external interrupt 5 control register (IRQ5ICR) controls interrupt level of external interrupt 5, valid edge, interrupt enable and interrupt request. Interrupt control register should be operated when the maskable interrupt enable flag (MIE) of PSE is “0”.

Table:3.2.8 External Interrupt 5 Control Register (IRQ5ICR:0x03FE7)

bp	7	6	5	4	3	2	1	0
Flag	IRQ5LV1	IRQ5LV0	REDG5	-	-	-	IRQ5IE	IRQ5IR
At reset	0	0	0	-	-	-	0	0
Access	R/W							

bp	Flag	Description
7-6	IRQ5LV1 IRQ5LV0	External interrupt level flag (at the standby mode) The CPU has interrupt levels from 0 to 3. This flag sets the interrupt level for interrupt requests.
5	REDG5	External interrupt valid edge flag 0:Falling edge (low level) 1:Rising edge (high level)
4-2	-	-
1	IRQ5IE	External interrupt enable flag 0:Disable interrupt 1:Enable interrupt
0	IRQ5IR	External interrupt request flag 0:No interrupt request 1:Interrupt request generated

■ Timer 0 Interrupt Control Register (TM0ICR)

The timer 0 interrupt control register (TM0ICR) controls interrupt level of timer 0 interrupt, interrupt enable flag and interrupt request. Interrupt control register should be operated when the maskable interrupt enable flag (MIE) or PSW is “0”.

Table:3.2.9 Timer 0 Interrupt Control Register (TM0ICR:0x03FE8)

bp	7	6	5	4	3	2	1	0
Flag	TM0LV1	TM0LV0	-	-	-	-	TM0IE	TM0IR
At reset	0	0	-	-	-	-	0	0
Access	R/W							

bp	Flag	Description
7-6	TM0LV1 TM0LV0	Interrupt level flag This 2-bit flag sets the interrupt level by assigning an interrupt level of 0 to 3 to interrupt requests.
5-2	-	-
1	TM0IE	Interrupt enable flag 0:Disable interrupt 1:Enable interrupt
0	TM0IR	Interrupt request flag 0:No interrupt request 1:Interrupt request generated

■ Timer 1 Interrupt Control Register (TM1ICR)

The timer 1 interrupt control register (TM1ICR) controls interrupt level of timer 1 interrupt, interrupt enable flag and interrupt request. Interrupt control register should be operated when the maskable interrupt enable flag (MIE) or PSW is “0”.

Table:3.2.10 Timer 1 Interrupt Control Register (TM1ICR:0x03FE9)

bp	7	6	5	4	3	2	1	0
Flag	TM1LV1	TM1LV0	-	-	-	-	TM1IE	TM1IR
At reset	0	0	-	-	-	-	0	0
Access	R/W							

bp	Flag	Description
7-6	TM1LV1 TM1LV0	Interrupt level flag This 2-bit flag sets the interrupt level by assigning an interrupt level of 0 to 3 to interrupt requests.
5-2	-	-
1	TM1IE	Interrupt enable flag 0:Disable interrupt 1:Enable interrupt
0	TM1IR	Interrupt request flag 0:No interrupt request 1:Interrupt request generated

■ Timer 2 Interrupt Control Register (TM2ICR)

The timer 2 interrupt control register (TM2ICR) controls interrupt level of timer 2 interrupt, interrupt enable flag and interrupt request. Interrupt control register should be operated when the maskable interrupt enable flag (MIE) or PSW is “0”.

Table:3.2.11 Timer 2 Interrupt Control Register (TM2ICR:0x03FEA)

bp	7	6	5	4	3	2	1	0
Flag	TM2LV1	TM2LV0	-	-	-	-	TM2IE	TM2IR
At reset	0	0	-	-	-	-	0	0
Access	R/W							

bp	Flag	Description
7-6	TM2LV1 TM2LV0	Interrupt level flag This 2-bit flag sets the interrupt level by assigning an interrupt level of 0 to 3 to interrupt requests.
5-2	-	-
1	TM2IE	Interrupt enable flag 0:Disable interrupt 1:Enable interrupt
0	TM2IR	Interrupt request flag 0:No interrupt request 1:Interrupt request generated

■ Timer 3 Interrupt Control Register (TM3ICR)

The timer 3 interrupt control register (TM3ICR) controls interrupt level of timer 3 interrupt, interrupt enable flag and interrupt request. Interrupt control register should be operated when the maskable interrupt enable flag (MIE) or PSW is “0”.

Table:3.2.12 Timer 3 Interrupt Control Register (TM3ICR:0x03FEB)

bp	7	6	5	4	3	2	1	0
Flag	TM3LV1	TM3LV0	-	-	-	-	TM3IE	TM3IR
At reset	0	0	-	-	-	-	0	0
Access	R/W							

bp	Flag	Description
7-6	TM3LV1 TM3LV0	Interrupt level flag This 2-bit flag sets the interrupt level by assigning an interrupt level of 0 to 3 to interrupt requests.
5-2	-	-
1	TM3IE	Interrupt enable flag 0:Disable interrupt 1:Enable interrupt
0	TM3IR	Interrupt request flag 0:No interrupt request 1:Interrupt request generated

■ Timer 4 Interrupt Control Register (TM4ICR)

The timer 4 interrupt control register (TM4ICR) controls interrupt level of timer 4 interrupt, interrupt enable flag and interrupt request. Interrupt control register should be operated when the maskable interrupt enable flag (MIE) or PSW is “0”.

Table:3.2.13 Timer 4 Interrupt Control Register (TM4ICR:0x03FEC)

bp	7	6	5	4	3	2	1	0
Flag	TM4LV1	TM4LV0	-	-	-	-	TM4IE	TM4IR
At reset	0	0	-	-	-	-	0	0
Access	R/W							

bp	Flag	Description
7-6	TM4LV1 TM4LV0	Interrupt level flag This 2-bit flag sets the interrupt level by assigning an interrupt level of 0 to 3 to interrupt requests.
5-2	-	-
1	TM4IE	Interrupt enable flag 0:Disable interrupt 1:Enable interrupt
0	TM4IR	Interrupt request flag 0:No interrupt request 1:Interrupt request generated

■ Timer 5 Interrupt Control Register (TM5ICR)

The timer 5 interrupt control register (TM5ICR) controls interrupt level of timer 5 interrupt, interrupt enable flag and interrupt request. Interrupt control register should be operated when the maskable interrupt enable flag (MIE) or PSW is “0”.

Table:3.2.14 Timer 5 Interrupt Control Register (TM5ICR:0x03FED)

bp	7	6	5	4	3	2	1	0
Flag	TM5LV1	TM5LV0	-	-	-	-	TM5IE	TM5IR
At reset	0	0	-	-	-	-	0	0
Access	R/W							

bp	Flag	Description
7-6	TM5LV1 TM5LV0	Interrupt level flag This 2-bit flag sets the interrupt level by assigning an interrupt level of 0 to 3 to interrupt requests.
5-2	-	-
1	TM5IE	Interrupt enable flag 0:Disable interrupt 1:Enable interrupt
0	TM5IR	Interrupt request flag 0:No interrupt request 1:Interrupt request generated

■ Timer 6 Interrupt Control Register (TM6ICR)

The timer 6 interrupt control register (TM6ICR) controls interrupt level of timer 6 interrupt, interrupt enable flag and interrupt request. Interrupt control register should be operated when the maskable interrupt enable flag (MIE) or PSW is “0”.

Table:3.2.15 Timer 6 Interrupt Control Register (TM6ICR:0x03FEE)

bp	7	6	5	4	3	2	1	0
Flag	TM6LV1	TM6LV0	-	-	-	-	TM6IE	TM6IR
At reset	0	0	-	-	-	-	0	0
Access	R/W							

bp	Flag	Description
7-6	TM6LV1 TM6LV0	Interrupt level flag This 2-bit flag sets the interrupt level by assigning an interrupt level of 0 to 3 to interrupt requests.
5-2	-	-
1	TM6IE	Interrupt enable flag 0:Disable interrupt 1:Enable interrupt
0	TM6IR	Interrupt request flag 0:No interrupt request 1:Interrupt request generated

■ Time Base Interrupt Control Register (TBICR)

The time base interrupt control register (TBICR) controls interrupt level of time base interrupt, interrupt enable flag and interrupt request. Interrupt control register should be operated when the maskable interrupt enable flag (MIE) of PSW is “0”.

Table:3.2.16 Time Base Interrupt Control Register (TBICR:0x03FEF)

bp	7	6	5	4	3	2	1	0
Flag	TBLV1	TBLV0	-	-	-	-	TBIE	TBIR
At reset	0	0	-	-	-	-	0	0
Access	R/W							

bp	Flag	Description
7-6	TBLV1 TBLV0	Interrupt level flag This 2-bit flag sets the interrupt level by assigning an interrupt level of 0 to 3 to interrupt requests.
5-2	-	-
1	TBIE	Interrupt enable flag 0:Disable interrupt 1:Enable interrupt
0	TBIR	Interrupt request flag 0:No interrupt request 1:Interrupt request generated

■ Timer 7 Interrupt Control Register (TM7ICR)

The timer 7 interrupt control register (TM7ICR) controls interrupt level of timer 7 interrupt, interrupt enable flag and interrupt request. Interrupt control register should be operated when the maskable interrupt enable flag (MIE) of PSW is “0”.

Table:3.2.17 Timer 7 Interrupt Control Register (TM7ICR:0x03FF0)

bp	7	6	5	4	3	2	1	0
Flag	TM7LV1	TM7LV0	-	-	-	-	TM7IE	TM7IR
At reset	0	0	-	-	-	-	0	0
Access	R/W							

bp	Flag	Description
7-6	TM7LV1 TM7LV0	Interrupt level flag This 2-bit flag sets the interrupt level by assigning an interrupt level of 0 to 3 to interrupt requests.
5-2	-	-
1	TM7IE	Interrupt enable flag 0:Disable interrupt 1:Enable interrupt
0	TM7IR	Interrupt request flag 0:No interrupt request 1:Interrupt request generated

■ Timer 7 Compare Register 2-match Interrupt Control Register (T7OC2ICR)

The timer 7 compare register 2-match interrupt control register (T7OC2ICR) controls interrupt level of timer 7 compare register 2-match interrupt, interrupt enable flag and interrupt request. Interrupt control register should be operated when the maskable interrupt enable flag (MIE) of PSW is “0”.

Table:3.2.18 Timer 7 Compare Register 2-match Interrupt Control Register (T7OC2ICR:0x03FF1)

bp	7	6	5	4	3	2	1	0
Flag	T7OC2LV1	T7OC2LV0	-	-	-	-	T7OC2IE	T7OC2IR
At reset	0	0	-	-	-	-	0	0
Access	R/W							

bp	Flag	Description
7-6	T7OC2LV1 T7OC2LV0	Interrupt level flag This 2-bit flag sets the interrupt level by assigning an interrupt level of 0 to 3 to interrupt requests.
5-2	-	-
1	T7OC2IE	Interrupt enable flag 0:Disable interrupt 1:Enable interrupt
0	T7OC2IR	Interrupt request flag 0:No interrupt request 1:Interrupt request generated

■ Serial 0 UART Reception Interrupt Control Register (SC0RICR)

The serial 0 UART reception interrupt control register (SC0RICR) controls interrupt level of serial 0 interrupt, interrupt enable flag and interrupt request. Interrupt control register should be operated when the maskable interrupt enable flag (MIE) of PSW is “0”.

Table:3.2.19 Serial 0 UART Reception Interrupt Control Register (SC0RICR:0x03FF2)

bp	7	6	5	4	3	2	1	0
Flag	SC0RLV1	SC0RLV0	-	-	-	-	SC0RIE	SC0RIR
At reset	0	0	-	-	-	-	0	0
Access	R/W							

bp	Flag	Description
7-6	SC0RLV1 SC0RLV0	Interrupt level flag This 2-bit flag sets the interrupt level by assigning an interrupt level of 0 to 3 to interrupt requests.
5-2	-	-
1	SC0RIE	Interrupt enable flag 0:Disable interrupt 1:Enable interrupt
0	SC0RIR	Interrupt request flag 0:No interrupt request 1:Interrupt request generated

■ Serial 0/UART Transmission Interrupt Control Register (SC0TICR)

The serial 0/UART transmission interrupt control register (SC0TICR) controls interrupt level of serial 0 interrupt, interrupt enable flag and interrupt request. Interrupt control register should be operated when the maskable interrupt enable flag (MIE) of PSW is “0”.

Table:3.2.20 Serial 0/UART Transmission Interrupt Control Register (SC0TICR:0x03FF3)

bp	7	6	5	4	3	2	1	0
Flag	SC0TLV1	SC0TLV0	-	-	-	-	SC0TIE	SC0TIR
At reset	0	0	-	-	-	-	0	0
Access	R/W							

bp	Flag	Description
7-6	SC0TLV1 SC0TLV0	Interrupt level flag This 2-bit flag sets the interrupt level by assigning an interrupt level of 0 to 3 to interrupt requests.
5-2	-	-
1	SC0TIE	Interrupt enable flag 0:Disable interrupt 1:Enable interrupt
0	SC0TIR	Interrupt request flag 0:No interrupt request 1:Interrupt request generated

■ Serial 1 UART Reception Interrupt Control Register (SC1RICR)

The serial 1 UART reception interrupt control register (SC1RICR) controls interrupt level of serial 1 interrupt, interrupt enable flag and interrupt request. Interrupt control register should be operated when the maskable interrupt enable flag (MIE) of PSW is “0”.

Table:3.2.21 Serial 1 UART Reception Interrupt Control Register (SC1RICR:0x03FF4)

bp	7	6	5	4	3	2	1	0
Flag	SC1RLV1	SC1RLV0	-	-	-	-	SC1RIE	SC1RIR
At reset	0	0	-	-	-	-	0	0
Access	R/W							

bp	Flag	Description
7-6	SC1RLV1 SC1RLV0	Interrupt level flag This 2-bit flag sets the interrupt level by assigning an interrupt level of 0 to 3 to interrupt requests.
5-2	-	-
1	SC1RIE	Interrupt enable flag 0:Disable interrupt 1:Enable interrupt
0	SC1RIR	Interrupt request flag 0:No interrupt request 1:Interrupt request generated

■ Serial 1/UART Transmission Interrupt Control Register (SC1TICR)

The serial 1/UART transmission interrupt control register (SC1TICR) controls interrupt level of serial 1 interrupt, interrupt enable flag and interrupt request. Interrupt control register should be operated when the maskable interrupt enable flag (MIE) of PSW is “0”.

Table:3.2.22 Serial 1 UART Transmission Interrupt Control Register (SC1TICR:0x03FF5)

bp	7	6	5	4	3	2	1	0
Flag	SC1TLV1	SC1TLV0	-	-	-	-	SC1TIE	SC1TIR
At reset	0	0	-	-	-	-	0	0
Access	R/W							

bp	Flag	Description
7-6	SC1TLV1 SC1TLV0	Interrupt level flag This 2-bit flag sets the interrupt level by assigning an interrupt level of 0 to 3 to interrupt requests.
5-2	-	-
1	SC1TIE	Interrupt enable flag 0:Disable interrupt 1:Enable interrupt
0	SC1TIR	Interrupt request flag 0:No interrupt request 1:Interrupt request generated

■ Serial 2 Interrupt Control Register (SC2ICR)

The serial 2 interrupt control register (SC2ICR) controls interrupt level of serial 2 interrupt, interrupt enable flag and interrupt request. Interrupt control register should be operated when the maskable interrupt enable flag (MIE) of PSW is “0”.

Table:3.2.23 Serial 2 Interrupt Control Register (SC2ICR:0x03FF6)

bp	7	6	5	4	3	2	1	0
Flag	SC2LV1	SC2LV0	-	-	-	-	SC2IE	SC2IR
At reset	0	0	-	-	-	-	0	0
Access	R/W							

bp	Flag	Description
7-6	SC2LV1 SC2LV0	Interrupt level flag This 2-bit flag sets the interrupt level by assigning an interrupt level of 0 to 3 to interrupt requests.
5-2	-	-
1	SC2IE	Interrupt enable flag 0:Disable interrupt 1:Enable interrupt
0	SC2IR	Interrupt request flag 0:No interrupt request 1:Interrupt request generated

■ Serial 3 Interrupt Control Register (SC3ICR)

The serial 3 interrupt control register (SC3ICR) controls interrupt level of serial 3 interrupt, interrupt enable flag and interrupt request. Interrupt control register should be operated when the maskable interrupt enable flag (MIE) of PSW is “0”.

Table:3.2.24 Serial 3 Interrupt Control Register (SC3ICR:0x03FF7)

bp	7	6	5	4	3	2	1	0
Flag	SC3LV1	SC3LV0	-	-	-	-	SC3IE	SC3IR
At reset	0	0	-	-	-	-	0	0
Access	R/W							

bp	Flag	Description
7-6	SC3LV1 SC3LV0	Interrupt level flag This 2-bit flag sets the interrupt level by assigning an interrupt level of 0 to 3 to interrupt requests.
5-2	-	-
1	SC3IE	Interrupt enable flag 0:Disable interrupt 1:Enable interrupt
0	SC3IR	Interrupt request flag 0:No interrupt request 1:Interrupt request generated

■ Serial 4 UART Reception Interrupt Control Register (SC4RICR)

The serial 4 UART reception interrupt control register (SC4RICR) controls interrupt level of serial 4 interrupt, interrupt enable flag and interrupt request. Interrupt control register should be operated when the maskable interrupt enable flag (MIE) of PSW is “0”.

Table:3.2.25 Serial 4 UART Reception Interrupt Control Register (SC4RICR:0x03FF8)

bp	7	6	5	4	3	2	1	0
Flag	SC4RLV1	SC4RLV0	-	-	-	-	SC4RIE	SC4RIR
At reset	0	0	-	-	-	-	0	0
Access	R/W							

bp	Flag	Description
7-6	SC4RLV1 SC4RLV0	Interrupt level flag This 2-bit flag sets the interrupt level by assigning an interrupt level of 0 to 3 to interrupt requests.
5-2	-	-
1	SC4RIE	Interrupt enable flag 0:Disable interrupt 1:Enable interrupt
0	SC4RIR	Interrupt request flag 0:No interrupt request 1:Interrupt request generated

■ Serial 4/UART Transmission Interrupt Control Register (SC4TICR)

The serial 4 UART transmission interrupt control register (SC4TICR) controls interrupt level of serial 4 interrupt, interrupt enable flag and interrupt request. Interrupt control register should be operated when the maskable interrupt enable flag (MIE) of PSW is “0”.

Table:3.2.26 Serial 4/UART Transmission Interrupt Control Register (SC4TICR:0x03FF9)

bp	7	6	5	4	3	2	1	0
Flag	SC4TLV1	SC4TLV0	-	-	-	-	SC4TIE	SC4TIR
At reset	0	0	-	-	-	-	0	0
Access	R/W							

bp	Flag	Description
7-6	SC4TLV1 SC4TLV0	Interrupt level flag This 2-bit flag sets the interrupt level by assigning an interrupt level of 0 to 3 to interrupt requests.
5-2	-	-
1	SC4TIE	Interrupt enable flag 0:Disable interrupt 1:Enable interrupt
0	SC4TIR	Interrupt request flag 0:No interrupt request 1:Interrupt request generated

■ A/D Conversion Interrupt Control Register (ADICR)

The A/D conversion interrupt control register (ADICR) controls interrupt level of A/D conversion interrupt, interrupt enable flag and interrupt request. Interrupt control register should be operated when the maskable interrupt enable flag (MIE) of PSW is “0”.

Table:3.2.27 A/D Conversion Interrupt Control Register (ADICR:0x03FFA)

bp	7	6	5	4	3	2	1	0
Flag	ADLV1	ADLV0	-	-	-	-	ADIE	ADIR
At reset	0	0	-	-	-	-	0	0
Access	R/W							

bp	Flag	Description
7-6	ADLV1 ADLV0	Interrupt level flag This 2-bit flag sets the interrupt level by assigning an interrupt level of 0 to 3 to interrupt requests.
5-2	-	-
1	ADIE	Interrupt enable flag 0:Disable interrupt 1:Enable interrupt
0	ADIR	Interrupt request flag 0:No interrupt request 1:Interrupt request generated

■ ATC11 Interrupt Control Register (ATC1ICR)

The ATC1 interrupt control register (ATC1ICR) controls interrupt level of ATC1 interrupt, interrupt enable flag and interrupt request. Interrupt control register should be operated when the maskable interrupt enable flag (MIE) of PSW is “0”.

Table:3.2.28 ATC1 Interrupt Control Register (ATC1ICR:0x03FFB)

bp	7	6	5	4	3	2	1	0
Flag	ATCLV1	ATCLV0	-	-	-	-	ATCIE	ATCIR
At reset	0	0	-	-	-	-	0	0
Access	R/W							

bp	Flag	Description
7-6	ATCLV1 ATCLV0	Interrupt level flag This 2-bit flag sets the interrupt level by assigning an interrupt level of 0 to 3 to interrupt requests.
5-2	-	-
1	ATCIE	Interrupt enable flag 0:Disable interrupt 1:Enable interrupt
0	ATCIR	Interrupt request flag 0:No interrupt request 1:Interrupt request generated

3.3 External Interrupts

There are 6 external interrupts in this LSI. The circuit (external interrupt interface), operates the external interrupt input signal, is built-in between the external interrupt input pin and the external interrupt block. This external interrupt interface can manage to do with any kind of external interrupts.

3.3.1 Overview

Table 3-3-1 shows the list of functions which external interrupts 0 to 5 are used.

Table:3.3.1 External Interrupt Functions

	External interrupt input pin	Programmable active edge	Both edges interrupt	Noise filter built-in	AC zero cross detection	Key input interrupt
External interrupt 0	P20	O		O		
External interrupt 1	P21	O		O		
External interrupt 2	P22	O	O			O
External interrupt 3	P23	O	O			O
External interrupt 4	P24	O			O	
External interrupt 5	P25	O	O			O

Because the external interrupt event acknowledged by the rising of the system clock, the pulse which is shorter than the system clock cycle is neglected.

System clock × 2 for the interrupt factor generation is needed at the maximum against the external interrupt event from the pin because all synchronous circuits are inserted.

3.3.2 Block Diagram

■ External Interrupt 0 Interface Block Diagram

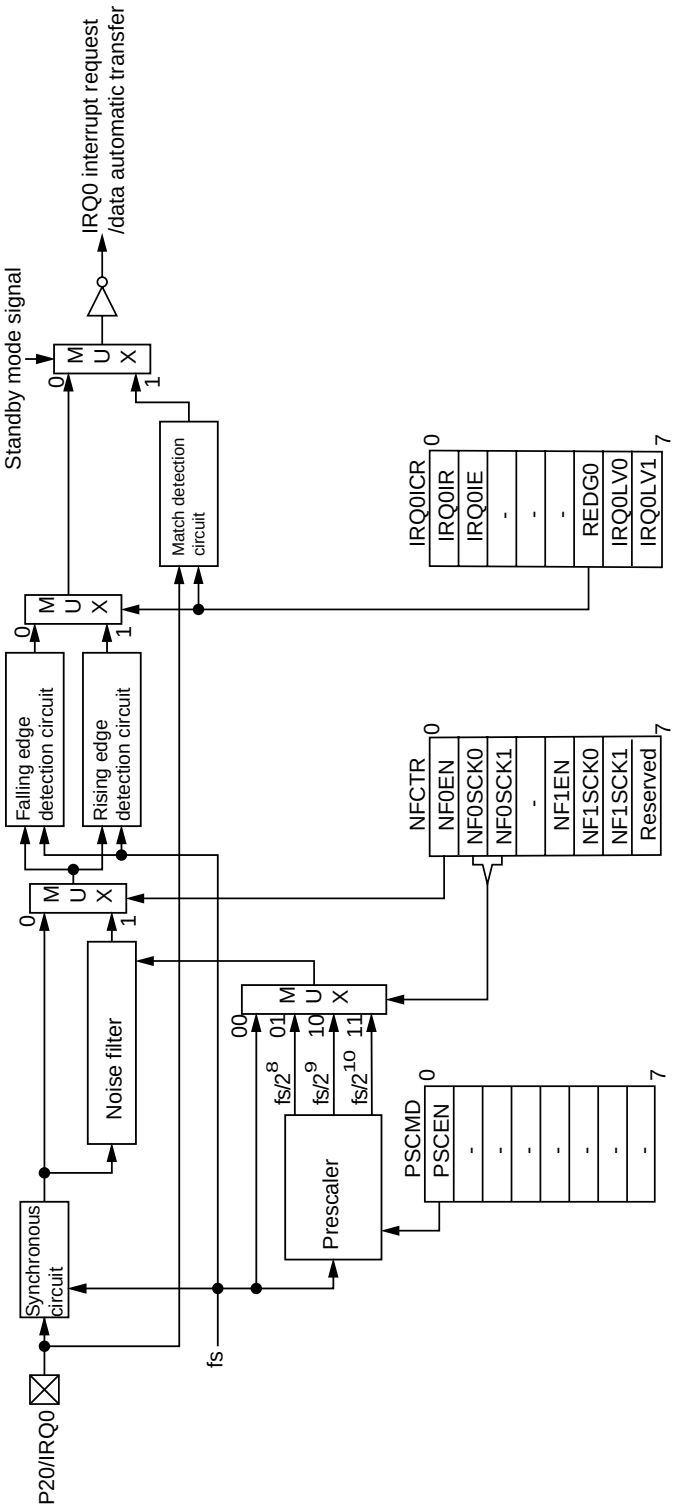


Figure:3.3.1 External Interrupt 0 Interface Block Diagram

■ External Interrupt 1 Interface Block Diagram

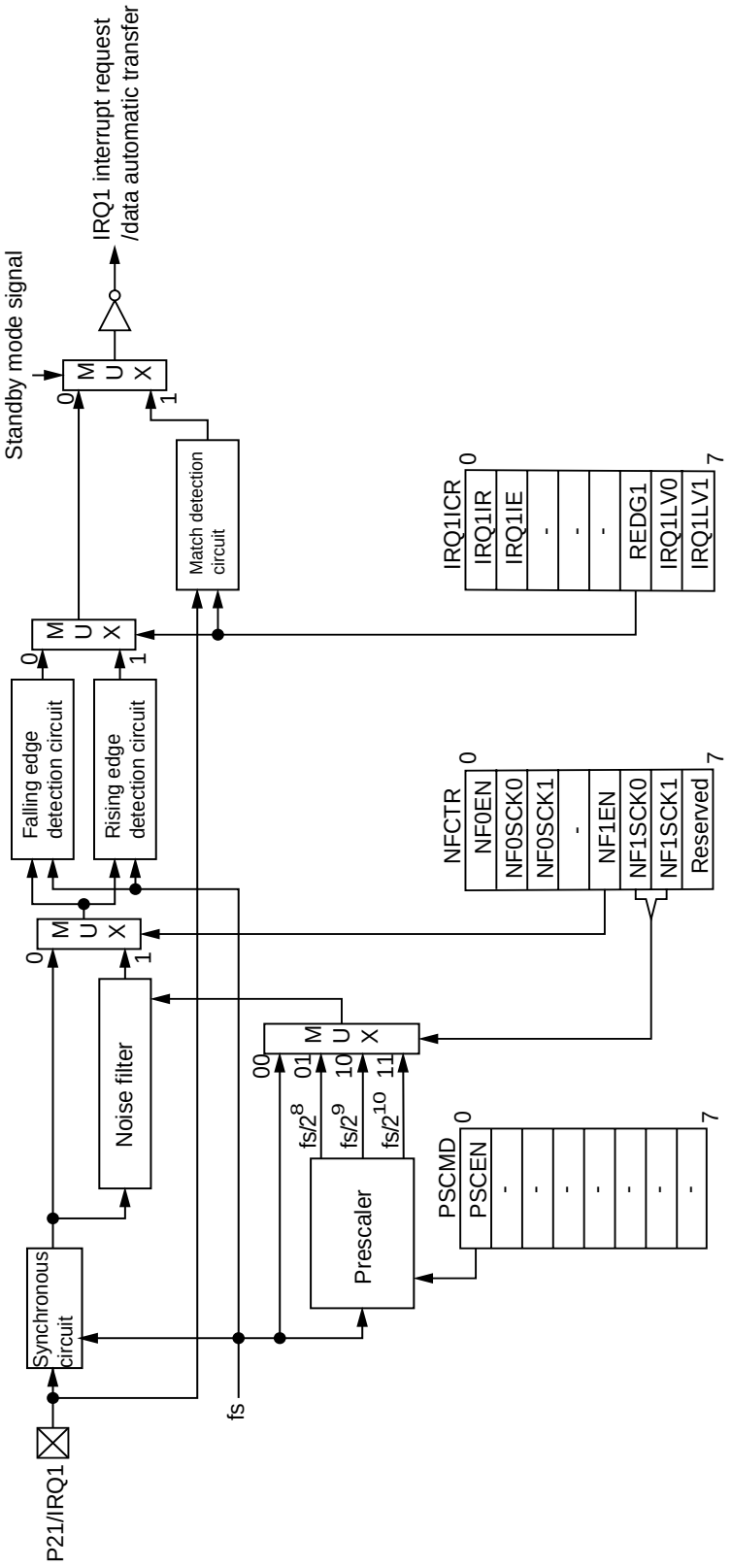


Figure:3.3.2 External Interrupt 1 Interface Block Diagram

■ External Interrupt 2 Interface Block Diagram

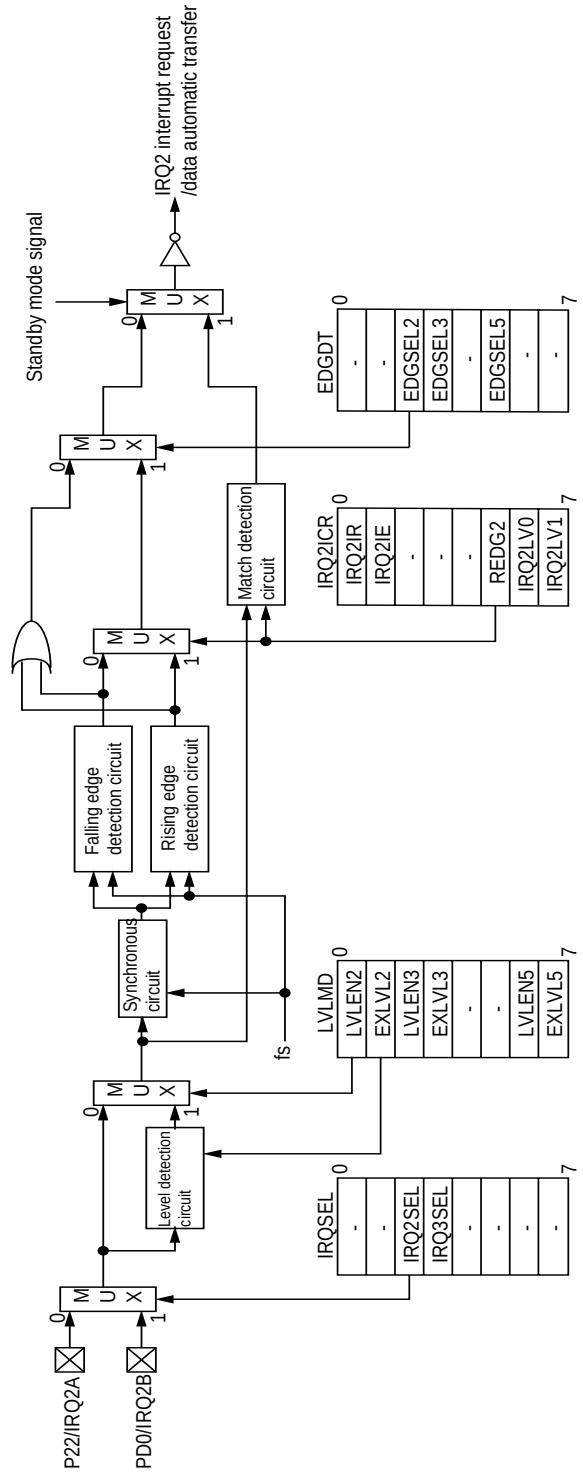


Figure:3.3.3 External Interrupt 2 Interface Block Diagram

■ External Interrupt 3 Interface Block Diagram

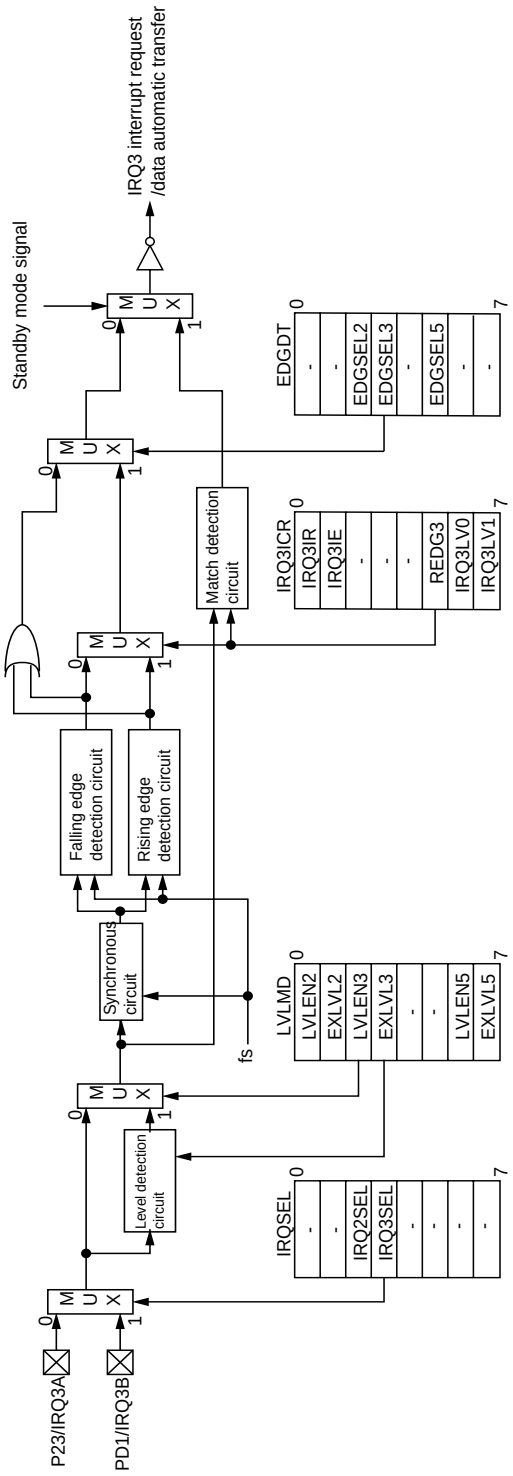


Figure:3.3.4 External Interrupt 3 Interface Block Diagram

■ External Interrupt 4 Interface Block Diagram

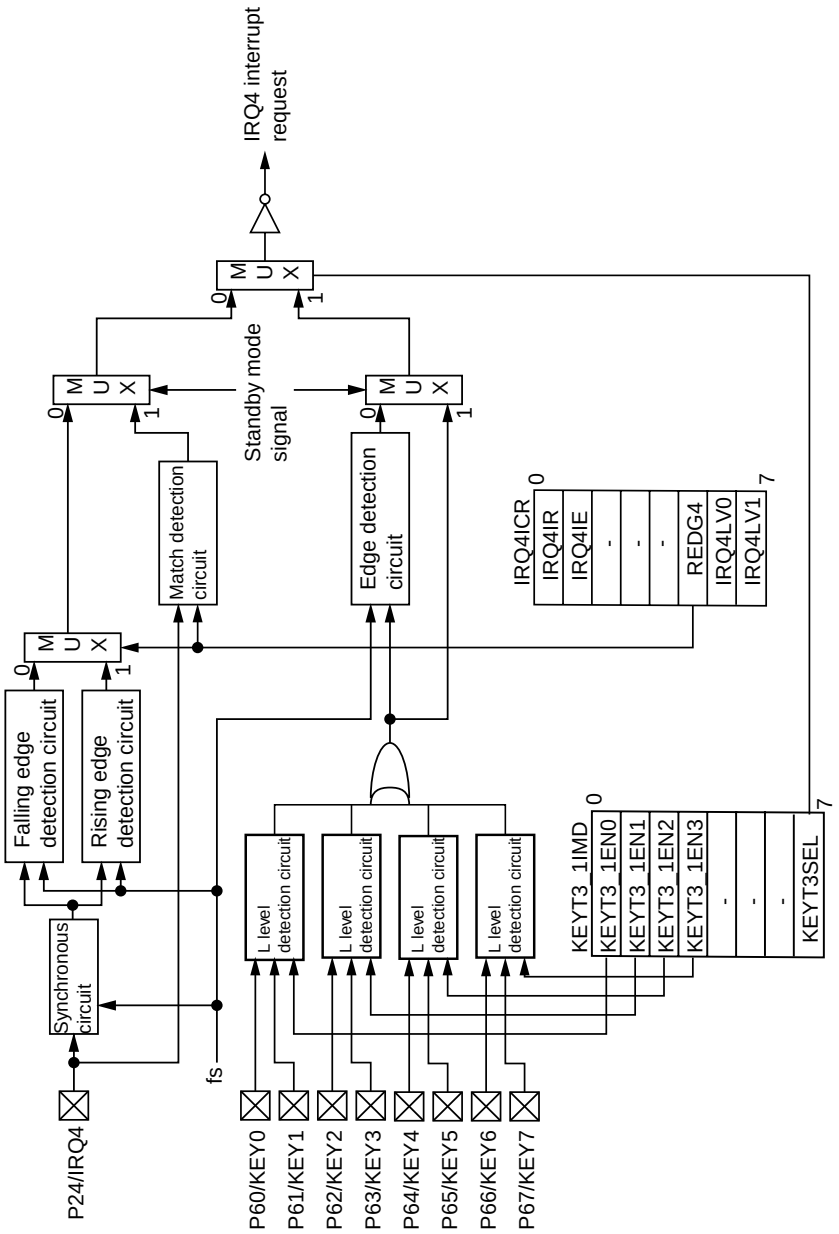


Figure:3.3.5 External Interrupt 4 Interface Block Diagram

■ External Interrupt 5 Interface Block Diagram

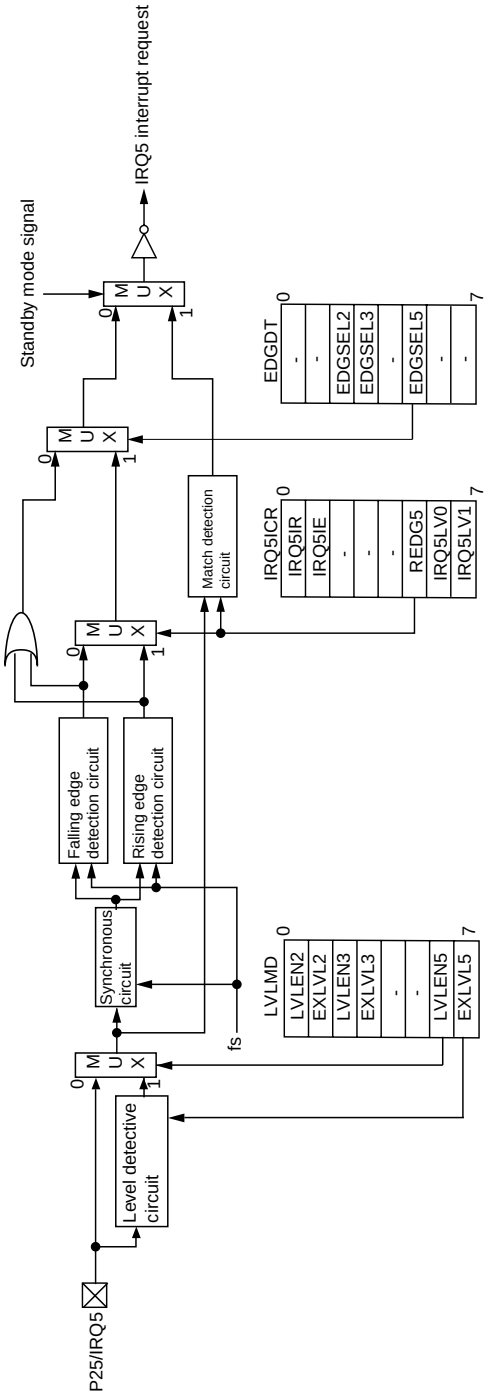


Figure:3.3.6 External Interrupt 5 Interface Block Diagram

3.3.3 Control Registers

The external interrupt input signals, which passed through each internal interrupt interface 0 to 5 generate interrupt requests.

External interrupt 0 to 5 interface are controlled by the external interrupt control register (IRQnICR). External interrupt interface 0 to 1 are controlled by the noise filter control register (NFCTR) and the prescaler control register (PSCMD), and external interrupt interface 2 to 3, 5 is controlled by the both edges interrupt control register (EDGDT), and external interrupt interface 4 is controlled by the key interrupt control register (KEYT3_1IMD), and external interrupt interface 2 to 3 are controlled by the external interrupt pin switching control register (IRQSEL), and external interrupt interface 2 to 3,5 are controlled by the external interrupt valid input switching control register (LVLMD).

Table 3-3-2 shows the list of registers, which control external interrupt 0 to 5.

Table:3.3.2 External Interrupt Control Register

External interrupt	Register	Address	R/W	Function	Page
External interrupt 0	IRQ0ICR	0x03FE2	R/W	External interrupt 0 control register	III-20
	NFCTR	0x03F2E	R/W	Noise filter control register	III-55
	PSCMD	0x03F6F	R/W	Prescaler control register	III-54
External interrupt 1	IRQ1ICR	0x03FE3	R/W	External interrupt 1 control register	III-21
	NFCTR	0x03F2E	R/W	Noise filter control register	III-55
	PSCMD	0x03F6F	R/W	Prescaler control register	III-54
External interrupt 2	IRQ2ICR	0x03FE4	R/W	External interrupt 2 control register	III-22
	EDGDT	0x03F1E	R/W	Both edges interrupt control register	III-56
	IRQSEL	0x03F4E	R/W	External interrupt pin switching control register	III-58
	LVLMD	0x03F6D	R/W	External interrupt valid input switching control register	III-59
External interrupt 3	IRQ3ICR	0x03FE5	R/W	External interrupt 3 control register	III-23
	EDGDT	0x03F1E	R/W	Both edges interrupt control register	III-56
	IRQSEL	0x03F4E	R/W	External interrupt pin switching control register	III-58
	LVLMD	0x03F6D	R/W	External interrupt valid input switching control register	III-59
External interrupt 4	IRQ4ICR	0x03FE6	R/W	External interrupt 4 control register	III-24
	KEYT3_1IMD	0x03F3E	R/W	Key interrupt control register	III-57
External interrupt 5	IRQ5ICR	0x03FE7	R/W	External interrupt 5 control register	III-31
	EDGDT	0x03F1E	R/W	Both edges interrupt control register	III-56
	LVLMD	0x03F6D	R/W	External interrupt valid input switching control register	III-59

R/W:Readable/Writable

■ Prescaler Control Register (PSCMD)

Prescaler control register enables or disables the prescaler count. Prescaler is used when the dividing clock of fs base is used at IRQ0, IRQ1.

Table:3.3.3 Prescaler Control Register (PSCMD:0x03F6F)

bp	7	6	5	4	3	2	1	0
Flag	-	-	-	-	-	-	-	PSCEN
At reset	-	-	-	-	-	-	-	0
Access	R/W							

bp	Flag	Description
7-1	-	-
0	PSCEN	Prescaler count control 0:Disable count 1:Enable count

■ Noise Filter Control Register (NFCTR)

The noise filter control register (NFCTR) sets the noise remove function to IRQ0 and IRQ1 and also selects the sampling cycle of noise remove function.

Table:3.3.4 Noise Filter Control Register (NFCTR:0x03F2E)

bp	7	6	5	4	3	2	1	0
Flag	Reserved	NF1SCK1	NF1SCK0	NF1EN	-	NF0SCK1	NF0SCK0	NF0EN
At reset	0	0	0	0	-	0	0	0
Access	R/W							

bp	Flag	Description
7	Reserved	Set always “0”
6-5	NF1SCK1 NF1SCK0	IRQ1/noise sampling period 00:fs 01:fs/2^8 10:fs/2^9 11:fs/2^{10}
4	NF1EN	IRQ1/noise filter setup 0:Noise filter OFF 1:Noise filter ON
3	-	-
2-1	NF0SCK1 NF0SCK0	IRQ0/noise sampling period 00:fs 01:fs/2^8 10:fs/2^9 11:fs/2^{10}
0	NF0EN	IRQ0/noise filter setup 0:Noise filter OFF 1:Noise filter ON

■ Both Edges Interrupt Control Register (EDGDT)

The both edges interrupt control register (EDGDT) selects interrupt edges of IRQ2 and IRQ3. Interrupts are generated at both edges, or at single edge. The external interrupt control register (IRQ2ICR, IRQ3ICR) specifies whether interrupts are generated.

Table:3.3.5 Both Edges Interrupt Control Register (EDGDT:0x03F1E)

bp	7	6	5	4	3	2	1	0
Flag	-	-	EDGSEL5	-	EDGSEL3	EDGSEL2	-	-
At reset	-	-	0	-	0	0	-	-
Access	R/W							

bp	Flag	Description
7-6	-	-
5	EDGSEL5	IRQ5 both edges interrupt selection 0:Programmable active edge interrupt selection 1:Both edges interrupt selection
4	-	-
3	EDGSEL3	IRQ3 both edges interrupt selection 0:Programmable active edge interrupt selection 1:Both edges interrupt selection
2	EDGSEL2	IRQ2 both edges interrupt selection 0:Programmable active edge interrupt selection 1:Both edges interrupt selection
1-0	-	-

■ Key Interrupt Control Register (KEYT3_1IMD)

The key interrupt control register selects if key interrupt is accepted, and external interrupt IRQ4 is accepted. Also, this register assigns KEY interrupt input pin to key interrupt in 2-bit unit.

Table:3.3.6 Key Interrupt Control Register 1 (KEYT3_1IMD:0x03F3E)

bp	7	6	5	4	3	2	1	0
Flag	KEYT3SEL	-	-	-	KEYT3_ 1EN3	KEYT3_ 1EN2	KEYT3_ 1EN1	KEYT3_ 1EN0
At reset	0	-	-	-	0	0	0	0
Access	R/W							

bp	Flag	Description
7	KEYT3SEL	IRQ4 interrupt source selection 0: External interrupt IRQ4 1:Key interrupt
6-4	-	-
3	KEYT3_1EN3	KEY7, KEY6 interrupt selection 0:Disable 1:Enable
2	KEYT3_1EN2	KEY5, KEY4 interrupt selection 0:Disable 1:Enable
1	KEYT3_1EN1	KEY3, KEY2 interrupt selection 0:Disable 1:Enable
0	KEYT3_1EN0	KEY1, KEY0 interrupt selection 0:Disable 1:Enable

■ External Interrupt Pin Switching Control Register (IRQSEL)

The external interrupt pin switching control register specifies interrupt input pin of external interrupt 2 and external interrupt 3 .

Table:3.3.7 External Interrupt Pin Switching Control Register (IRQSEL:0x03F4E)

bp	7	6	5	4	3	2	1	0
Flag	-	-	-	-	IRQ3SEL	IRQ2SEL	-	-
At reset	-	-	-	-	0	0	-	-
Access	R/W							

bp	Flag	Description
7-4	-	-
3	IRQ3SEL	External interrupt 3 input pin switching 0:P23 1:PD1
2	IRQ2SEL	External interrupt 2 input pin switching 0:P22 1:PD0
1-0	-	-

■ External Interrupt Valid Input Switching Control Register (LVLMD)

Table:3.3.8 External Interrupt Valid Input Switching Control Register (LVLMD:0x03F6D)

bp	7	6	5	4	3	2	1	0
Flag	EXLVL5	LVLEN5	-	-	EXLVL3	LVLEN3	EXLVL2	LVLEN2
At reset	0	0	-	-	0	0	0	0
Access	R/W							

bp	Flag	Description
7	EXLVL5	External interrupt 5 valid input level set 0:L level 1:H level
6	LVLEN5	External interrupt 5 valid input set 0:Hedge 1:Level
5-4	-	-
3	EXLVL3	External interrupt 3 valid input level set 0:L level 1:H level
2	LVLEN3	External interrupt 3 valid input set 0:Hedg 1:Levele
1	EXLVL2	External interrupt 2 valid input level set 0:L level 1:H level
0	LVLEN2	External interrupt 2 valid input set 0:Hedge 1:Level

3.3.4 Programmable Active Edge Interrupt

■ Programmable Active Edge Interrupts (External interrupts 0 to 5)

The programmable active edge interrupt can select the rising/falling edge about the signal which is input from the external interrupt input pin and generate the interrupt at the selected edge. Also, if the value which is set to the external interrupt valid edge specify flag and the level of the external interrupt pin are matched, it is possible from the standby mode.

■ Programmable Active Edge Interrupt Setup Example (External interrupt 0 to 5)

External interrupt 0 (IRQ0) is generated at the rising edge of the input signal from P20.
The table below shows a setup example of IRQ0.

Setup Procedure	Description
(1)Specify the interrupt active edge IRQ0ICR(0x03FE2) bp5ÅFREDG0 =1	(1)Set the REDG0 flag of the external interrupt 0 control register (IRQ0ICR) to “1” to specify the rising edge as the active edge for interrupts.
(2)Set the interrupt level IRQ0ICR (0x03FE2) bp7-6:IRQ0LV1-0 =10	(2)Set the interrupt priority level in the IRQ0LV1 to 0 flag of the IRQ0ICR register. The interrupt request flag of the IRQ0ICR register may be set, so make sure to clear the interrupt request flag (IRQ0IR). [Chapter 3. 3-1-4 Interrupt flag setup]
(3)Enable the interrupt IRQ0ICR (0x03FE2) bp1:IRQ0IE =1	(3)Set the IRQ0IE flag of the IRQ0ICR register to “1” enable the interrupt.

External interrupt 0 is generated at the rising edge of the input signal from P20.

The interrupt request flag can be set at switching the interrupt edge, so specify the interrupt valid edge before the interrupt permission.

The external interrupt pin is recommended to be pull-up in advance.

At the standby mode, if the value that is set to the external interrupt valid specified flag and the external interrupt pin level are matched, the interrupt is generated. (refer to figure 3-3-1 to 3-3-6.)
So when “flag is 0 and pin is 0” or “flag is 1 and pin is 1” before standby, interrupt is generated at the standby mode and CPU can be returned.

3.3.5 Both Edges Interrupt

■ Both Edges Interrupt (External interrupt 2, 3, and 5)

Both edges interrupt can generate interrupt at both the falling edge and the rising edge by the input signal from external input pins. CPU also can be returned from standby mode.

At the standby mode, if the value that is set to the external interrupt valid specified flag and the external interrupt pin level are matched, the interrupt is generated. (refer to figure 3-3-1 to 3-3-6.)
So when “flag is 0 and pin is 0” or “flag is 1 and pin is 1” before standby, interrupt is generated at the standby mode and CPU can be returned.

■ Both Edges Interrupt Setup Example (External interrupt 2, External interrupt 3)

External interrupt 2 (IRQ2) is generated at the both edges of the input signal from P22 pin.
The table below shows a setup example of IRQ2.

Setup Procedure	Description
(1)Select the both edges interrupt EDGDT (0x03F1E) bp2:EDGSEL1 =1	(1)Set the EDGSEL2 flag of the both edges interrupt control register (EDGDT) to “1” to select the both edges interrupt.
(2)Set the interrupt level IRQ2ICR (0x03FE4) bp7-6:IRQ2LV1-0 =10	(2)Set the interrupt level by the IRQ2LV1 to 0 flag of the IRQ2ICR register. The interrupt request flag of the IRQ2ICR register may be set, so make sure to clear the interrupt request flag (IRQ2IR). [Chapter 3. 3-1-4 Interrupt flag setup]
(3)Enable the interrupt IRQ2ICR (0x03FE4) bp1:IRQ2IE =1	(3)Set the IRQ2IE flag of the IRQ2ICR register to “1” to enable the interrupt.

At the both edges of the input signal from P22 pin, an external interrupt 2 is generated.

When the both edges interrupt is selected, the interrupt request is generated at the both edge, regardless of the REDGn flag of the external interrupt control register (IRQnICR).

The interrupt request flag may be set at switching the interrupt edge. So, clear the interrupt request flag before the interrupt acceptance. Also, select the both edges interrupt before the interrupt acceptance.

The external interrupt pis is recommended to be pull-up, in advance.

3.3.6 Level Interrupt

■ Level Interrupt (External interrupts 2, 3, and 5)

The level interrupt can select the input level H or input level L about the signal which is input from the external interrupt input pin and generate the interrupt at the selected edge. It is possible from the standby mode.

■ Level Interrupt Example (External interrupts 2, 3, and 5)

External interrupt 2 (IRQ2) is generated at the H level of the input signal from P20.
The table below shows a setup example of IRQ2.

Setup Procedure	Description
(1)Specify the interrupt valid edge IRQ2ICR (0x03FE4) bp5:REDG2 =1	(1)Set theREDG2 flag of the external interrupt 0 control register(IRQ2ICR) to “0” and specify the rising edge as the valid edge.
(2)Specify the interrupt valid input LVLMD(0x03F6D) bp1 :EXLVL2 =1	(2)Set the EXLVL flag of the external interrupt valid input switching control register(LVLMD) to “1” to specify the interrupt valid input level as the level interrupt(H level).
(3)Enable the level interrupt LVLMD (0x03F6D) bp7-6:IRQ2LV1-0 =10	(3)Set the EXLVL flag of the external interrupt valid input switching control register(LVLMD) to “1” to specify the interrupt valid input level as the level interrupt(H level)
(4)Set the interrupt level IRQ2ICR (0x03FE4) bp7-6:IRQ2LV1-0 =10	(4)Set the interrupt priority level in the IRQ2LV1 to 0 flag of the IRQ2ICR register. The interrupt request flag of the IRQ2ICR register may be set, so make sure to clear the interrupt request flag (IRQ2IR).
(5)Enable the interrupt IRQ2ICR (0x03FE4) bp1:IRQ2IE =1	(5)Set the IRQ2IE flag of the IRQ2ICR register to “1” enable the interrupt.

External interrupt 2 is generated at the H level of the input signal from P22.

Set the external interrupt valid input level equal to the polarity of the interrupt valid edge.

External interrupt valid input level = H level Interrupt valid edge=rising edge
External interrupt valid input level = L level Interrupt valid edge=falling edge

The interrupt request flag can be set at switching the interrupt edge, so specify the interrupt valid edge before the interrupt permission.

The external interrupt pin is recommended to be pull-up in advance.

At the standby mode, if the value that is set to the external interrupt valid specified flag and the external interrupt pin level are matched, the interrupt is generated. (refer to figure 3-3-1 to 3-3-6.)
So when “flag is 0 and pin is 0” or “flag is 1 and pin is 1” before standby, interrupt is generated at the standby mode and CPU can be returned.

3.3.7 Key Input Interrupt

■ Key Input Interrupt (External interrupt 4)

This LSI can set port 6 (P60 to P67) pin by 2 bit to key input pin. An interrupt can be generated at the falling edge, if at least 1 key input pin outputs low level. (Standby mode can be recovered by the key interrupt.)

Key input pin should be pull-up in advance.

■ Key Input Interrupt Setup Example (External interrupt 4)

After P60 to P63 of port 6 are set to key input pins and key is input (“L” level), the external interrupt 4 (IRQ4) is generated.
An example setup procedure, with a description of each step is shown below.

Setup Procedure	Description
(1)Set the key input to input P6DIR (0x03F36) bp3-0:P4DIR3-0 =0000	(1)Set the P6DIR3 to 0 flag of the port 6 direction control register (P6DIR) to “0000” to set P40 to P43 pins to input pins.
(2)Set the pull-up resistor P6PLU (0x03F46) bp3-0:P6PLU3-0 =1111	(2)Set the P6PLU3 to 0 flag of the port 6 pull-up resistor control register (P4PLU) to “1111” to add the pull-up resistors to P60 to P63 pins.
(3)Select the key input interrupt KEYT3_1IMD (0x03F3E) bp7:KEYT3_1SEL =1	(3)Set the KEYT3SEL flag of the key interrupt control register (KEYT3_1IMD) to “1” to enable the port 6 key interrupt at the external interrupt 4. .
(4)Select the key input pin KEYT3_1IMD (0x03F3E) bp1-0:KEYT3_1EN1-0 =11	(4)Set the KEYT3_1EN1 to 0 of the key interrupt control register (KEYT3_1IMD) to “11” to set P60 to P63 pins to key input pins.
(5)Set the interrupt level IRQ4ICR (0x03FE6) bp7-6:IRQ4LV1-0 =10	(5)Set the interrupt level by the IRQ4LV1 to 0 flag of the IRQ4ICR register. If the interrupt request flag has been already set, clear the request flag(IRQ4IR). [Chapter 3 3-1-4. Interrupt Flag Setup]
(6)Enable the interrupt IRQ4ICR (0x03FE6) bp1:IRQ4IE =1	(6)Set the IRQ4IE flag of the IRQ4ICR register to “1” to enable the interrupt.

*Above (3) and (4) can be set at the same time.

If there is at least one input signal, from the P60 to P63 pins, shows low level, the external interrupt 4 is generated at the falling edge.

The key input should be setup before the interrupt is accepted.

3.3.8 Noise Filter

■ Noise Filter (External interrupts 0 and 1)

Noise filter reduce noise by sampling the input waveform from the external interrupt pins (IRQ0, IRQ1). Its sampling cycle can be selected from 4 types(fs, $fs/2^8$, $fs/2^9$, $fs/2^{10}$)

■ Noise Remove Selection (External interrupts 0 and 1)

Noise remove function can be selected by setting the NFnEN flag of the noise filter control register (NFCTR) to "1".

Table:3.3.9 Addition of Noise Remove Function

NFnEN	IRQ input (P20)	IRQ input (P21)
0	IRQ0 noise filter OFF	IRQ1 noise filter OFF
1	IRQ0 noise filter ON	IRQ1 noise filter ON

■ Sampling Cycle Setup (External interrupts 0 and 1)

The sampling cycle of noise remove function can be set by the NFnSCK2 to 0 flag of the NFCTR register.

Table:3.3.10 Sampling Cycle / Time of Noise Remove Function

NFnCKS1	NFnCKS0	Sampling cycle	fs=10 MHz	
0	0	fs	10 MHz	100 ns
	1	$fs/2^8$	39.06 kHz	25.6 μs
1	0	$fs/2^9$	19.53 kHz	51.20 μs
	1	$fs/2^{10}$	9.76 kHz	102.40 μs

■ Noise Remove Function Operation (External interrupts 0 and 1)

After sampling the input signal to the external interrupt pins (IRQ0, IRQ1) with the set sampling time, if the same level comes continuously three times, that level is sent to the inside of LSI. If the same level does not come continuously three times, the previous level is sent. It means that only the signal with the amplitude of longer than "Sampling time × 3 sampling clock" can pass through the noise filter, and other signals with amplitude shorter than this are removed, because those are regarded as noise.

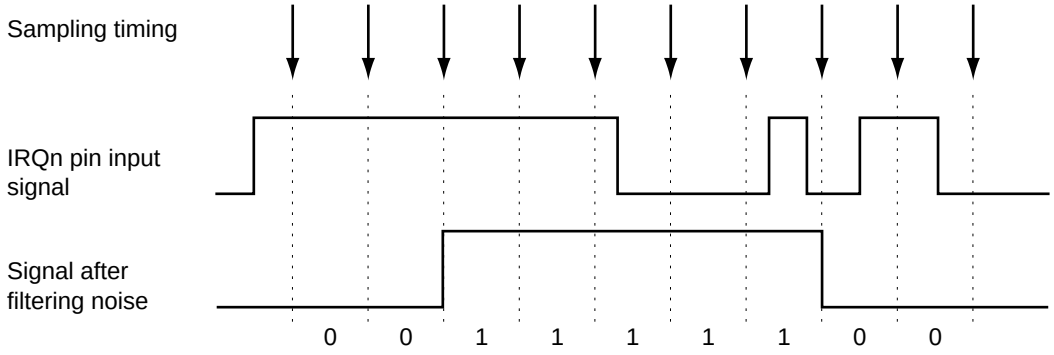


Figure:3.3.7 Noise Remove Function Operation

Noise filter cannot be used at STOP mode and HALT mode.

Noise filter can be uses at the SLOW mode. However, sampling timing gets slow extremely.

■ Noise Filter Setup Example (External interrupt 0 and 1)

Noise remove function is added to the input signal from P20 pin to generate the external interrupt 0 (IRQ0) at the rising edge. The sampling clock is set to fs, and the operation state is fs = 10 MHz. An example setup procedure, with a description of each step is shown below.

Setup procedure	Description
(1)Specify the interrupt valid edge IRQ0ICR (0x03FE2) bp5:REDG0 =1	(1)Set the REDG0 flag of the external interrupt 0 control register (IRQ0ICR) to “1” to specify the interrupt valid edge to the rising edge.
(2)Select the sampling clock NFCTR (0x03F2E) bp2-1:NF0SCK1-0 =00	(2)Select the sampling clock to fosc by the NF0SCK1 to 0 flag of the noise filter control register (NFCTR).
(3)Set the noise filter operation NFCTR (0x03F2E) bp0:NF0EN =1	(3)Set the NF0EN flag of the NFCTR register to “1” to add the noise filter operation.
(4)Set the interrupt level IRQ0ICR (0x03FE2) bp7-6:IRQ0LV1-0 =10	(4)Set the interrupt level by the IRQ0LV1 to 0 flag of the IRQ0ICR register. If the interrupt request flag has been already set, clear the request flag. [Chapter 3 3-1-4. Interrupt Flag Setup]
(5)Enable the interrupt IRQ0ICR (0x03FE2) bp1:IRQ0IE =1	(5)Set the IRQ0IE flag of the IRQ0ICR register to “1” to enable the interrupt.

*Above (3) and (2) can be set at the same time.

The input signal from P20 pin outputs the interrupt factor at the edge that is followed to the programmable active edge after passing through the noise filter.

The noise filter should be setup before the interrupt is enabled.

The external interrupt pins are recommended to be pull-up in advance.

3.3.9 External Interrupt At The Standby Mode

■ External Interrupt at the Standby Mode (External interrupt 0 to 5)

It is possible from the standby mode by the external interrupt.

At the standby mode, when the value which is set to the external interrupt valid edge specify flag and the external interrupt pin level are matched, the interrupt is generated. Therefore, be aware of the value of the external interrupt valid edge specify flag and the external interrupt pin level at the transition to the standby mode. If the value which is set to the external interrupt valid edge specify flag and the external interrupt pin level are matched at the transition to the standby mode, it recovers from the standby mode right away.

■ Setup Examples of the External Interrupt at the Standby Mode

The generation of the external interrupt 0 (IRQ0) can recover from STOP mode by the low level signal which is input from the external interrupt.

Setup procedure	Description
(1)Specify the interrupt valid edge IRQ0ICR (0x03FE2) bp5:REDG0 =0	(1)Set the REDG0 of the external interrupt 0 control register (IRQ0ICR) to “0” to specify the interrupt valid edge to the rising edge.
(2)Set the external interrupt pin The external interrupt 0 pin is pulled-up in advance.	(2)The value of the REDG0 flag of the IRQ0ICR register and the external interrupt pin level is different.
(3)Set the interrupt level IRQ0ICR (0x03FE2) bp7-6:IRQ0LV1-0 =10	(3)Set the interrupt level by the IRQ0LV1 to 0 flag of the IRQ0ICR register. If the interrupt request has been already set, clear the interrupt request flag (IRQ0IR).
(4)Enable the interrupt IRQ0ICR (0x03FE2) bp1:IRQ0IE =1	(4)Set the IRQ0IE flag of the IRQ0ICR register to “1” to enable the interrupt.
(5)Set the STOP mode CPUM (0x03F00) bp3:STOP =1	(5)Transfer to the STOP mode by setting STOP flag of the CPU mode control register (CPUM) to “1”. [Chapter 2 2-4-4. Transfer to Standby Mode]

If the low level of the signal is input to the external interrupt 0 pin, then, the value of the external interrupt valid edge specify flag and the external interrupt 0 pin are matched, the external interrupt 0 is accepted and recover from the STOP mode.

Recovering from the STOP mode is done when the oscillation stabilization wait time which is set at the oscillation stabilization wait control register (DLYCTR) is passed after the acceptance of the external interrupt. [Chapter 2 2-8-4. Oscillation Stabilization Wait Time]

Chapter 4 I/O Ports

4

4.1 Overview

4.1.1 I/O Port Overview

A total of 85pins on this LSI, including those shared with special function pins, are allocated for the I/O ports of port 0, port 1, port 2, port 3, port 4, port 5, port 6, port 7, port 8, port 9, port A, and port D

4.1.2 I/O Port Status at Reset

Table:4.1.1 I/O port status at reset (single chip mode)

Port	I/O mode	Pull-up/Pull-down resistor	I/O port, special functions
Port 0	Input mode	No pull-up resistor	I/O port
Port 1	Input mode	No pull-up resistor	I/O port
Port 2	Input mode	P27:Pull-up resistor Others:No pull-up resistor	I/O port
Port 3	Input mode	No pull-up resistor	I/O port
Port 4	Input mode	No pull-up/pull-down resistor	I/O port
Port 5	Input mode	No pull-up resistor	I/O port
Port 6	Input mode	No pull-up resistor	I/O port
Port 7	Input mode	No pull-up/pull-down resistor	I/O port
Port 8	Input mode	No pull-up resistor	I/O port
Port 9	Input mode	No pull-up resistor	I/O port
Port A	Input mode	No pull-up/pull-down resistor	I/O port
Port D	Input mode	No pull-up resistor	I/O port

Table:4.1.2 I/O port status at reset (processor mode)

Port	I/O mode	Pull-up/Pull-down resistor	I/O port, special functions
Port 0	Input mode	No pull-up resistor	I/O port
Port 1	Input mode	No pull-up resistor	I/O port
Port 2	Input mode	P27:Pull-up resistor Others:No pull-up resistor	I/O port
Port 3	Input mode	No pull-up resistor	I/O port
Port 4	Input mode	No pull-up/pull-down resistor	I/O port
Port 5	A7,A6,A5,A4,A3,A2,A1, A0 : Output mode	No pull-up resistor	A7,A6,A5,A4,A3,A2,A1,A0
Port 6	A15,A14,A13,A12,A11,A 10,A9,A8 : Output mode	No pull-up resistor	A15,A14,A13,A12,A11,A10,A9,A8
Port 7	,NEW,NRE,NCS: Output mode Others : Input mode	No pull-up/pull-down resistor	,NEW,NRE,NCS,I/O port
Port 8	Input mode	No pull-up resistor	D7,D6,D5,D4,D3,D2,D1,D0
Port 9	Input mode	No pull-up resistor	I/O port
Port A	Input mode	No pull-up/pull-down resistor	I/O port
Port D	Input mode	No pull-up resistor	I/O port

4.1.3 Control Registers

port 0,port 1,port 2,port 3,port 4,port 5,port 6,port 7,port 8,port 9,port A,port Dare controlled by the data output register (PnOUT), the data input register (PnIN), the I/O direction control register (PnDIR), the pull-up resistor control register (PnPLU) or the pull-up/pull-down resistor control register (PnPLUD) and registers that control special function pin (P10MD, PnIMD, PnSYO, PnSEV, PnCNT, EXADV, PnODC).

port 0,port 1,port 2,port 3,port 4,port 5,port 6,port 7,port 8,port 9,port A,port DThe following Table shows the registers to control

Table:4.1.3 I/O Port Control Registers List

Register	Address	R/W	Function	Page
P0OUT	0x03F10	R/W	Port 0 Output Register	IV-7
P0IN	0x03F20	R	Port 0 Input Register	IV-8
P0DIR	0x03F30	R/W	Port 0 Direction Control Register	IV-8
P0PLU	0x03F40	R/W	Port 0 Pull-up Resistor Control Register	IV-9
P0ODC	0x03F1C	R/W	Port 0 Nch Open-drain Control Register	IV-9
P1OUT	0x03F11	R/W	Port 1 Output Register	IV-15
P1IN	0x03F21	R	Port 1 Input Register	IV-16
P1DIR	0x03F31	R/W	Port 1 Direction Control Register	IV-16
P1PLU	0x03F41	R/W	Port 1 Pull-up Resistor Control Register	IV-17
P1OMD	0x03F2B	R/W	Port 1 Output Mode Register	IV-18
P1CNT0	0x03F7E	R/W	Port 1 Output Control Register 0	IV-19
P2OUT	0x03F12	R/W	Port 2 Output Register	IV-27
P2IN	0x03F22	R	Port 2 Input Register	IV-28
P2DIR	0x03F32	R/W	Port 2 Direction Control Register	IV-28
P2PLU	0x03F42	R/W	Port 2 Pull-up Resistor Control Register	IV-29
P3OUT	0x03F13	R/W	Port 3 Output Register	IV-35
P3IN	0x03F23	R	Port 3 Input Register	IV-36
P3DIR	0x03F33	R/W	Port 3 Direction Control Register	IV-36
P3PLU	0x03F43	R/W	Port 3 Pull-up Resistor Control Register	IV-37
P3ODC	0x03F2C	R/W	Port 3 Nch Open-drain Control Register	IV-37
P4OUT	0x03F14	R/W	Port 4 Output Register	IV-42
P4IN	0x03F24	R	Port 4 Input Register	IV-43
P4DIR	0x03F34	R/W	Port 4 Direction Control Register	IV-43
P4PLU	0x03F44	R/W	Port 4 Pull-up/Pull-down Resistor Control Register	IV-44
P4ODC	0x03F3C	R/W	Port 4 Nch Open-drain Control Register	IV-44
SELUD	0x03F4B	R/W	Pull-up/Pull-down Resistor Selection Register	IV-45
P5OUT	0x03F15	R/W	Port 5 Output Register	IV-49

Register	Address	R/W	Function	Page
P5IN	0x03F25	R	Port 5 Input Register	IV-50
P5DIR	0x03F35	R/W	Port 5 Direction Control Register	IV-50
P5PLU	0x03F45	R/W	Port 5 Pull-up Resistor Control Register	IV-51
P6OUT	0x03F16	R/W	Port 6 Output Register	IV-58
P6IN	0x03F26	R	Port 6 Input Register	IV-59
P6DIR	0x03F36	R/W	Port 6 Direction Control Register	IV-59
P6PLU	0x03F46	R/W	Port 6 Pull-up Resistor Control Register	IV-60
EXADV	0x03F0E	R/W	Address Output Control Register	IV-60
P7OUT	0x03F17	R/W	Port 7 Output Register	IV-67
P7IN	0x03F27	R	Port 7 Input Register	IV-68
P7DIR	0x03F37	R/W	Port 7 Direction Control Register	IV-68
P7PLU	0x03F47	R/W	Port 7 Pull-up/Pull-down Resistor Control Register	IV-69
P7SYO	0x03F1F	R/W	Port 7 Synchronous Output Control Register	IV-69
P7SEV	0x03F2F	R/W	Port 7 Synchronous Output Event Selection Register	IV-70
SELUD	0x03F4B	R/W	Pull-up/Pull-down Resistor Selection Register	IV-70
EXADV	0x03F0E	R/W	Address Output Control Register	IV-71
P8OUT	0x03F18	R/W	Port 8 Output Register	IV-81
P8IN	0x03F28	R	Port 8 Input Register	IV-82
P8DIR	0x03F38	R/W	Port 8 Direction Control Register	IV-82
P8PLU	0x03F48	R/W	Port 8 Pull-up Resistor Control Register	IV-83
P9OUT	0x03F19	R/W	Port 9 Output Register	IV-90
P9IN	0x03F29	R	Port 9 Input Register	IV-91
P9DIR	0x03F39	R/W	Port 9 Direction Control Register	IV-91
P9PLU	0x03F49	R/W	Port 9 Pull-up Resistor Control Register	IV-92
P9ODC	0x03F4C	R/W	Port 9 Nch Open-drain Control Register	IV-92
PAOUT	0x03F1A	R/W	Port A Output Register	IV-97
PAIN	0x03F2A	R	Port A Input Register	IV-98
PADIR	0x03F3A	R/W	Port A Direction Control Register	IV-98
PAPLU	0x03F4A	R/W	Port A Pull-up/Pull-down Resistor Control Register	IV-99
PAIMD	0x03F4A	R/W	Port A Input Mode Register	IV-99
PDOUT	0x03F1D	R/W	Port D Output Register	IV-107
PDIN	0x03F2D	R	Port D Input Register	IV-108
PDDIR	0x03F3D	R/W	Port D Direction Control Register	IV-108
PDPLU	0x03F4D	R/W	Port D Pull-up Resistor Control Register	IV-109
PDOMD	0x03F1B	R/W	Port D Output Mode Register	IV-109

4.2 Port 0

4.2.1 Description

■ General Port Setup

To output the data to pins, set the control flag of the port 0 direction control register (P0DIR) to "1" to write the value of the port 0 output register (P0OUT).

To read input data of pins, set the control flag of the port 0 direction control register (P0DIR) to "0" to read the value of the port 0 input register (P0IN).

Each bit can be set individually as either an input or output by the port 0 I/O direction control register (P0DIR). The control flag of the port 0 direction control register (P0DIR) is set to "1" for output mode, and "0" for input mode.

Each bit can be set individually if pull-up resistor is added or not, by the port 0 pull-up resistor control register (P0PLU). Set the control flag of the port 0 pull-up resistor control register (P0PLU) to "1" to add pull-up resistor.

P00, P02, P03, and P5 can select the Nch open-drain output by each bit by the port 0 Nch open-drain control register (P0ODC). The port 0 Nch open-drain control register (P0ODC) is set to "1" for the Nch open-drain output and "0" for the push-pull output.

■ Special Function Pin Setup

P00 is used as output pin of the serial 0 transmission data or the UART 0 transmission data, as well. When the SC0SBOS flag of the serial interface 0 mode register 1 (P0ODC) is set to "1", it is output pin of the serial data. Also, the push-pull output or the Nch open-drain output can be selected by the setup of the port 0 Nch open-drain control register (P0ODC).

P01 is used as input pin of the serial 0 reception data or the UART 0 reception data, as well.

P02 is used as I/O pin of the serial 0 clock, as well. When the SC0SBTS flag of the serial interface 0 mode register 1 (SC0MD1) is set to "1", it is output pin of the serial clock. Also, the push-pull output or the Nch open-drain output can be selected by the setup of the port 0 Nch open-drain control register (P0ODC).

P03 is used as output pin of the serial 2 transmission data or the IIC2 transmission data, as well. When the SC2SBOS flag of the serial interface 2 mode register 1 (SC2MD1) is set to "1", it is output pin of the serial data. Also, the push-pull output or the Nch open-drain output can be selected by the setup of the port 0 Nch open-drain control register (P0ODC).

P04 is used as input pin of the serial 2 reception data or the IIC 2 reception data.

P05 is used as I/O pin of the serial 2 clock, as well. When the SC2SBTS flag of the serial interface 2 mode register 1 (SC2MD1) is set to "1", it is output pin of the serial clock. Also, the push-pull output or the Nch open-drain output can be selected by the setup of the port 0 Nch open-drain control register (P0ODC).

P06 is used as the D/A output pin of the DA0, as well. With the D/A control register (DACTR), P06 is used as the D/A output pin of the DA0 during D/A conversion, it is used as a general-purpose port for other times. When the pin is used as the D/A conversion, "1" is read out from the port 0 input register (P0IN).

4.2.2 Registers

The following Table shows registers that control the Port 0

Table:4.2.1 Port 0control register

Registers	Address	R/W	Function	Page
P0OUT	0x03F10	R/W	Port 0 Output Register	IV-7
P0IN	0x03F20	R	Port 0 Input Register	IV-8
P0DIR	0x03F30	R/W	Port 0 Direction Control Register	IV-8
P0PLU	0x03F40	R/W	Port 0 Pull-up Resistor Control Register	IV-9
P0ODC	0x03F1C	R/W	Port 0 Nch Open-drain Control Register	IV-9

R/W:Readable/Writable

■ Port 0 Output Register(P0OUT:0x03F10)

bp	7	6	5	4	3	2	1	0
Flag	-	P0OUT6	P0OUT5	P0OUT4	P0OUT3	P0OUT2	P0OUT1	P0OUT0
At reset	-	x	x	x	x	x	x	x
Access	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bp	Flag	Description
7 6 5 4 3 2 1 0	- P0OUT6 P0OUT5 P0OUT4 P0OUT3 P0OUT2 P0OUT1 P0OUT0	Output data 0:Output L(VSS level) 1:Output H(VDD level)

■ Port 0 Input Register(P0IN:0x03F20)

bp	7	6	5	4	3	2	1	0
Flag	-	P0IN6	P0IN5	P0IN4	P0IN3	P0IN2	P0IN1	P0IN0
At reset	-	x	x	x	x	x	x	x
Access	-	R	R	R	R	R	R	R

bp	Flag	Description
7 6 5 4 3 2 1 0	- P0IN6 P0IN5 P0IN4 P0IN3 P0IN2 P0IN1 P0IN0	Input data 0:Pin is L(VSS level) 1:Pin is H(VDD level)

■ Port 0 Direction Control Register(P0DIR:0x03F30)

bp	7	6	5	4	3	2	1	0
Flag	-	P0DIR6	P0DIR5	P0DIR4	P0DIR3	P0DIR2	P0DIR1	P0DIR0
At reset	-	0	0	0	0	0	0	0
Access	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bp	Flag	Description
7 6 5 4 3 2 1 0	- P0DIR6 P0DIR5 P0DIR4 P0DIR3 P0DIR2 P0DIR1 P0DIR0	I/O mode selection 0:Input mode 1:Output mode

■ Port 0 Pull-up Resistor Control Register(P0PLU:0x03F40)

bp	7	6	5	4	3	2	1	0
Flag	-	P0PLU6	P0PLU5	P0PLU4	P0PLU3	P0PLU2	P0PLU1	P0PLU0
At reset	-	0	0	0	0	0	0	0
Access	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bp	Flag	Description
7 6 5 4 3 2 1 0	- P0PLU6 P0PLU5 P0PLU4 P0PLU3 P0PLU2 P0PLU1 P0PLU0	Pull-up resistor selection 0:Not added 1:Added

■ Port 0 Nch Open-drain Control Register(P0ODC:0x03F1C)

bp	7	6	5	4	3	2	1	0
Flag	-	-	P0ODC5	-	P0ODC3	P0ODC2	-	P0ODC0
At reset	-	-	0	-	0	0	-	0
Access	-	-	R/W	-	R/W	R/W	-	R/W

bp	Flag	Description
7 6 5 4 3 2 1 0	- - P0ODC5 - P0ODC3 P0ODC2 - P0ODC0	Nch open-drain output selection 0:Push/pull output 1:Nch open-drain output

4.2.3 Block Diagram

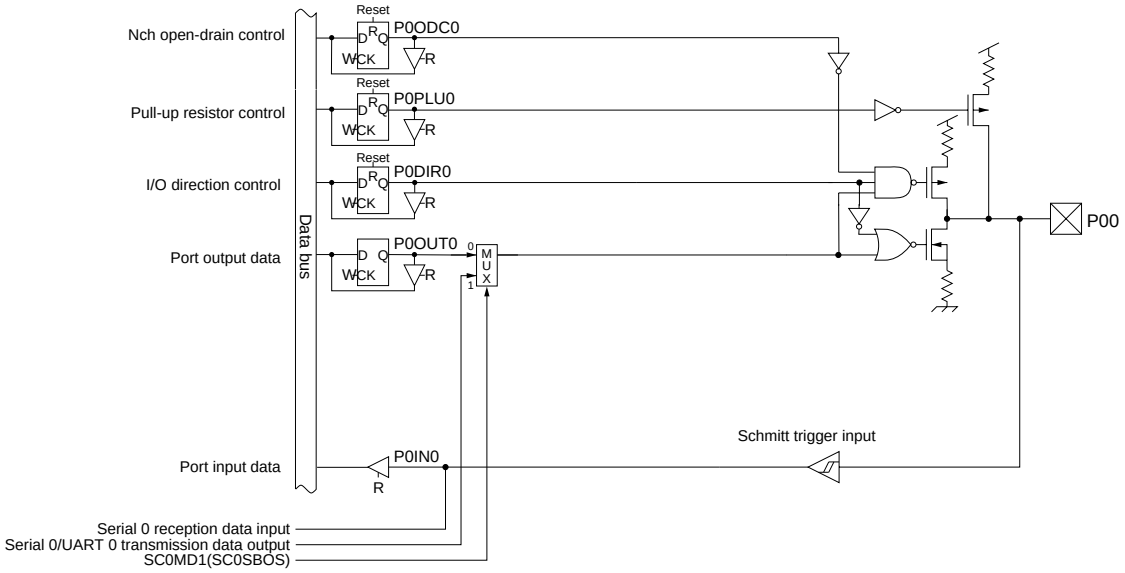


Figure:4.2.1 P00 Block Diagram

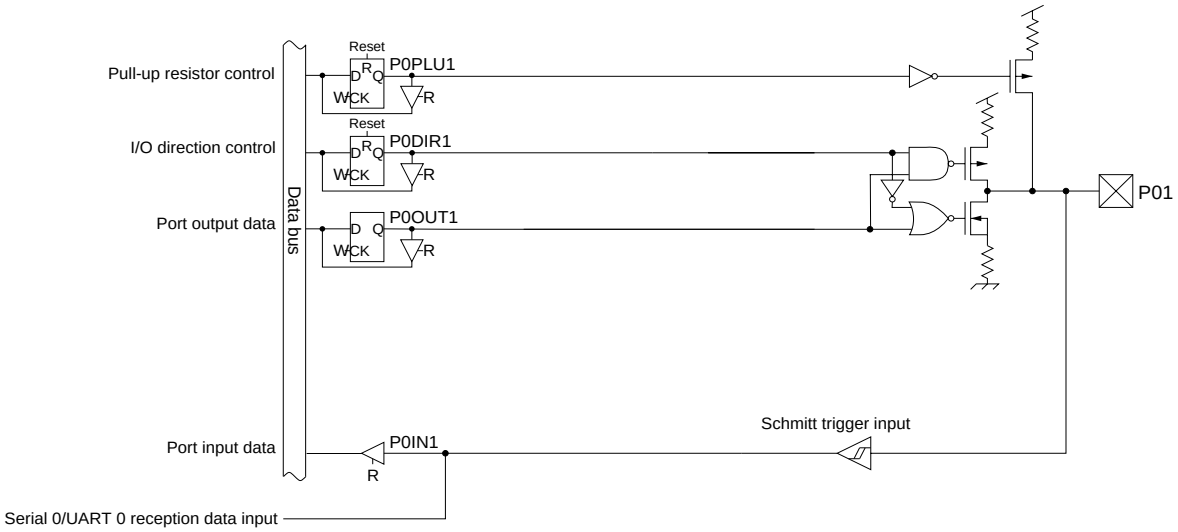


Figure:4.2.2 P01 Block Diagram

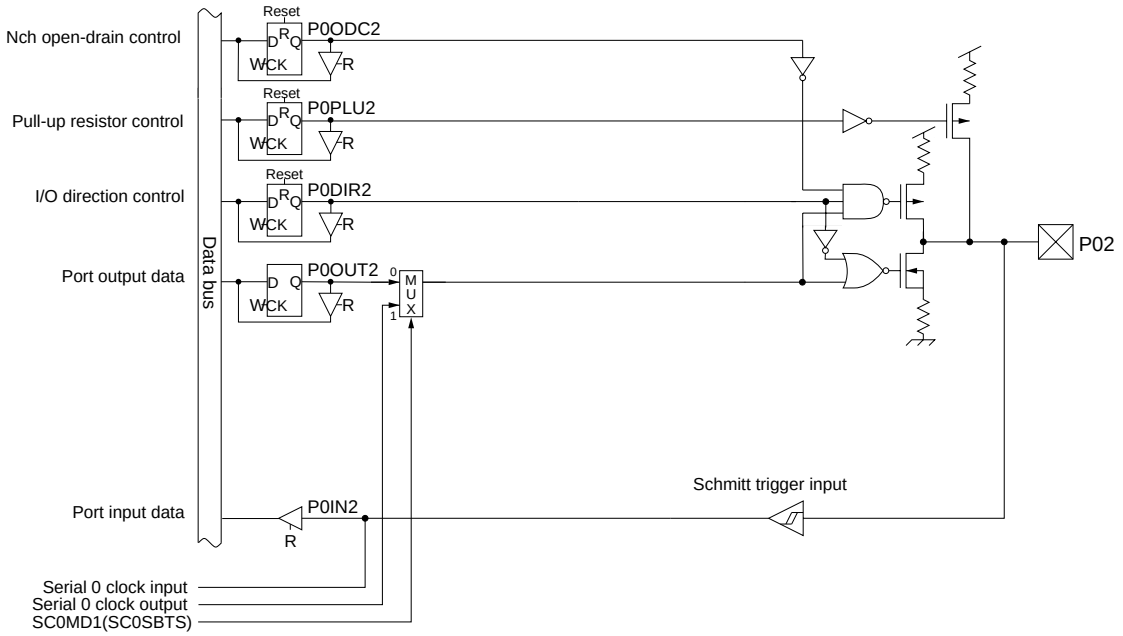


Figure:4.2.3 P02 Block Diagram

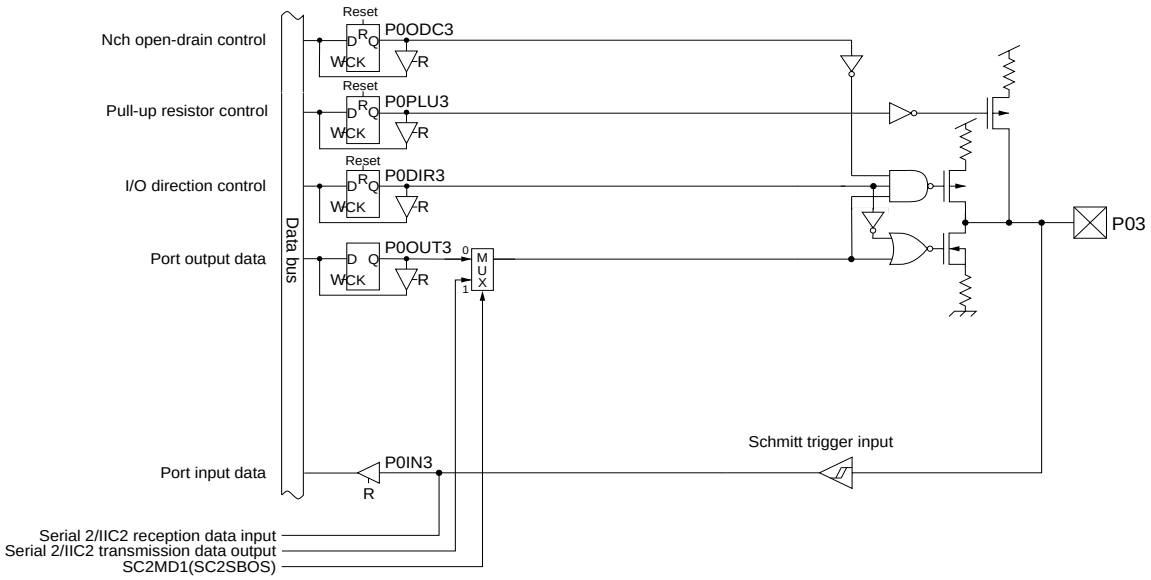


Figure:4.2.4 P03 Block Diagram

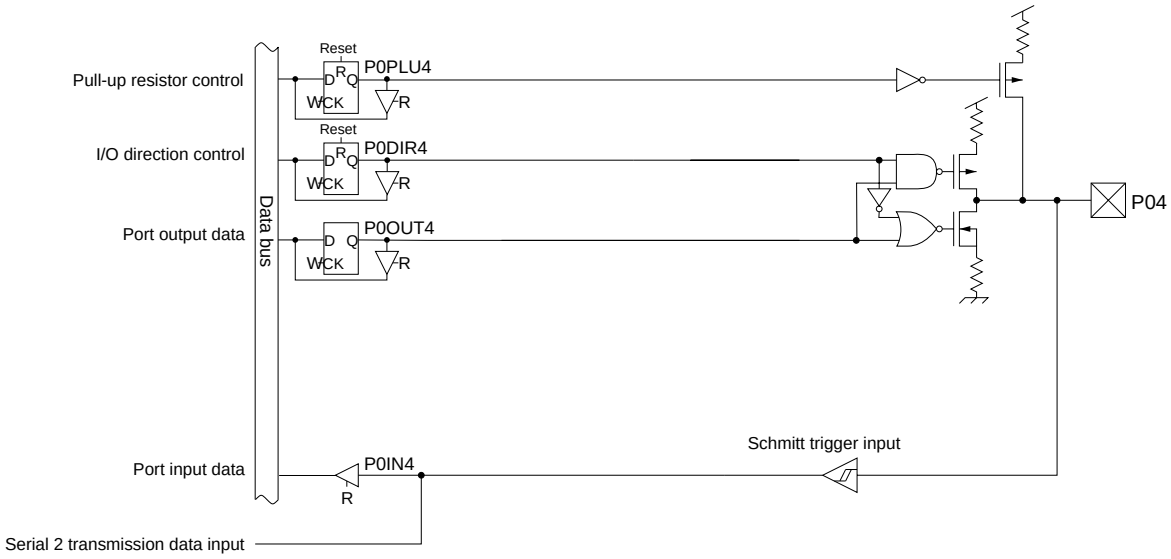


Figure:4.2.5 P04 Block Diagram

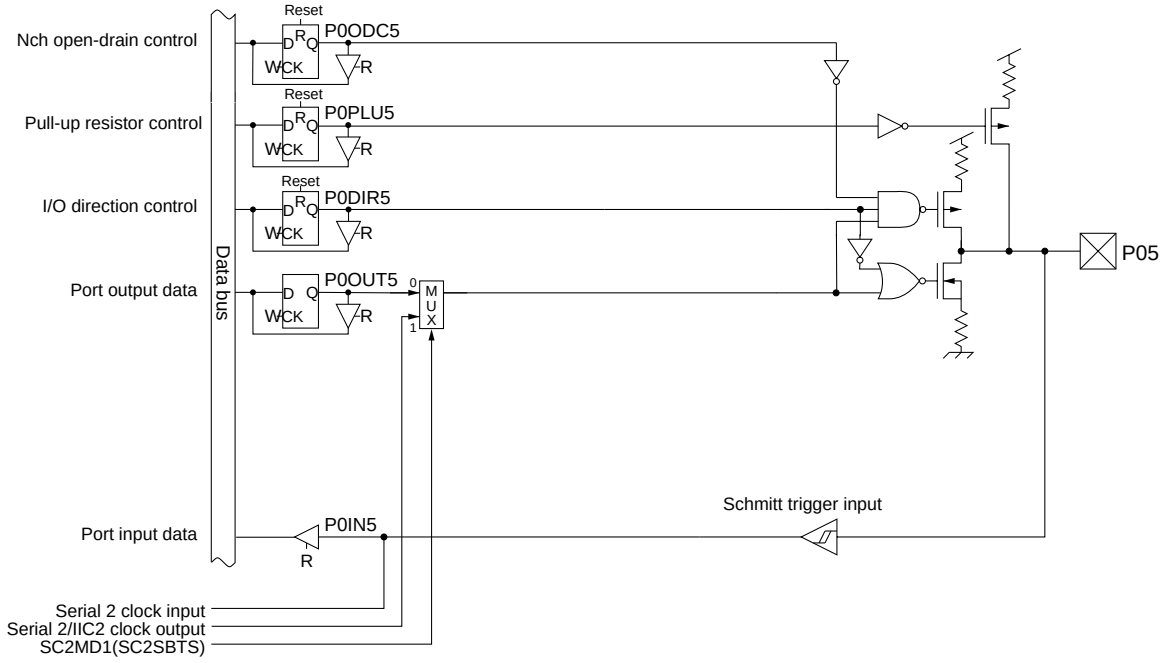


Figure:4.2.6 P05 Block Diagram

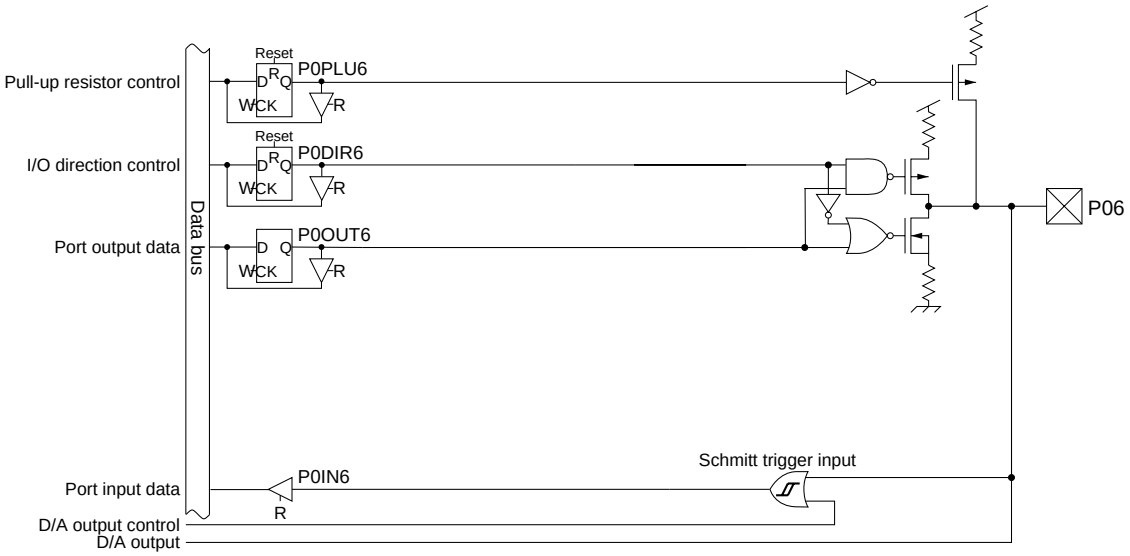


Figure:4.2.7 P06 Block Diagram

4.3 Port 1

4.3.1 Description

■ General Port Setup

To output the data to pins, set the control flag of the port 1 direction control register (P1DIR) to "1" to write the value of the port 1 output register (P1OUT).

To read input data of pins, set the control flag of the port 1 direction control register (P1DIR) to "0" to read the value of the port 1 input register (P1IN).

Each bit can be set individually as either an input or output by the port 1 I/O direction control register (P1DIR). The control flag of the port 1 direction control register (P1DIR) is set to "1" for output mode, and "0" for input mode.

Each bit can be set individually if pull-up resistor is added or not, by the port 1 pull-up resistor control register (P1PLU). Set the control flag of the port 1 pull-up resistor control register (P1PLU) to "1" to add pull-up resistor.

Each bit can be selected individually as output mode by the port 1 output mode register (P1OMD). The port 1 output mode register (P1OMD) is set to "1" to output the special function data, and "0" to use as the general port.

■ Special Function Pin Setup

P10 is used as I/O pin of the timer 0 and output pin of the remote control career, as well. The output mode can be selected by bpm of the port 1 output mode register (P1OMD) by each bit. The port 1 output mode register (P1OMD) is set to "1" to output the special function data, and "0" to use as the general port.

P11 is used as I/O pin of the timer 1, as well. The output mode can be selected by bpm of the port 1 output mode register (P1OMD) by each bit. The port 1 output mode register (P1OMD) is set to "1" to output the special function data, and "0" to use as the general port.

P12 is used as I/O pin of the timer 2, as well. The output mode can be selected by bpm of the port 1 output mode register (P1OMD) by each bit. The port 1 output mode register (P1OMD) is set to "1" to output the special function data, and "0" to use as the general port.

P13 is used as I/O pin of the timer 3, as well. The output mode can be selected by bpm of the port 1 output mode register (P1OMD) by each bit. The port 1 output mode register (P1OMD) is set to "1" to output the special function data, and "0" to use as the general port.

P14 is used as I/O pin of the timer 4, as well. The output mode can be selected by bpm of the port 1 output mode register (P1OMD) by each bit. The port 1 output mode register (P1OMD) is set to "1" to output the special function data, and "0" to use as the general port.

P15 is used as I/O pin of the timer 5, as well. The output mode can be selected by bpm of the port 1 output mode register (P1OMD) by each bit. The port 1 output mode register (P1OMD) is set to "1" to output the special function data, and "0" to use as the general port.

P16 is used as I/O pin of the timer 7, as well. The output mode can be selected by bpm of the port 1 output mode register (P1OMD) by each bit. The port 1 output mode register (P1OMD) is set to "1" to output the special function data, and "0" to use as the general port.

P10, P12, and P14 have the functions of the real time output control and can switch pin output to "0", "1", "Hi-impedance" at the event generation timing of the falling edge of the interrupt X. The real time control is the function which can change the output signal without the interposition with synchronized to the interrupt event.

4.3.2 Registers

The following Table shows registers that control the Port 1

Table:4.3.1 Port 1control register

Registers	Address	R/W	Function	Page
P1OUT	0x03F11	R/W	Port 1 Output Register	IV-15
P1IN	0x03F21	R	Port 1 Input Register	IV-16
P1DIR	0x03F31	R/W	Port 1 Direction Control Register	IV-16
P1PLU	0x03F41	R/W	Port 1 Pull-up Resistor Control Register	IV-17
P1OMD	0x03F2B	R/W	Port 1 Output Mode Register	IV-18
P1CNT0	0x03F7E	R/W	Port 1 Real Time Output Control Register 0	IV-19

R/W:Readable/Writable

■ Port 1 Output Register(P1OUT:0x03F11)

bp	7	6	5	4	3	2	1	0
Flag	-	P1OUT6	P1OUT5	P1OUT4	P1OUT3	P1OUT2	P1OUT1	P1OUT0
At reset	-	x	x	x	x	x	x	x
Access	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bp	Flag	Description
7 6 5 4 3 2 1 0	- P1OUT6 P1OUT5 P1OUT4 P1OUT3 P1OUT2 P1OUT1 P1OUT0	Output data 0:Output L(VSS level) 1:Output H(VDD level)

■ Port 1 Input Register(P1IN:0x03F21)

bp	7	6	5	4	3	2	1	0
Flag	-	P1IN6	P1IN5	P1IN4	P1IN3	P1IN2	P1IN1	P1IN0
At reset	-	x	x	x	x	x	x	x
Access	-	R	R	R	R	R	R	R

bp	Flag	Description
7 6 5 4 3 2 1 0	- P1IN6 P1IN5 P1IN4 P1IN3 P1IN2 P1IN1 P1IN0	Input data 0:Pin is L(VSS level) 1:Pin is H(VDD level)

■ Port 1 Direction Control Register(P1DIR:0x03F31)

bp	7	6	5	4	3	2	1	0
Flag	-	P1DIR6	P1DIR5	P1DIR4	P1DIR3	P1DIR2	P1DIR1	P1DIR0
At reset	-	0	0	0	0	0	0	0
Access	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bp	Flag	Description
7 6 5 4 3 2 1 0	- P1DIR6 P1DIR5 P1DIR4 P1DIR3 P1DIR2 P1DIR1 P1DIR0	I/O mode selection 0:Input mode 1:Output mode

■ Port 1 Pull-up Resistor Control Register(P1PLU:0x03F41)

bp	7	6	5	4	3	2	1	0
Flag	-	P1PLU6	P1PLU5	P1PLU4	P1PLU3	P1PLU2	P1PLU1	P1PLU0
At reset	-	0	0	0	0	0	0	0
Access	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bp	Flag	Description
7 6 5 4 3 2 1 0	- P1PLU6 P1PLU5 P1PLU4 P1PLU3 P1PLU2 P1PLU1 P1PLU0	Pull-up resistor selection 0:Not added 1:Added

■ Port 1 Output Mode Register(P1OMD:0x03F2B)

bp	7	6	5	4	3	2	1	0
Flag	-	P1OMD6	P1OMD5	P1OMD4	P1OMD3	P1OMD2	P1OMD1	P1OMD0
At reset	-	0	0	0	0	0	0	0
Access	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bp	Flag	Description
7	-	-
6	P1OMD6	I/O port, TM7IO selection 0:I/O port 1:TM7IO
5	P1OMD5	I/O port, TM5IO selection 0:I/O port 1:TM5IO
4	P1OMD4	I/O port, TM4IO selection 0:I/O port 1:TM4IO
3	P1OMD3	I/O port, TM3IO selection 0:I/O port 1:TM3IO
2	P1OMD2	I/O port, TM2IO selection 0:I/O port 1:TM2IO
1	P1OMD1	I/O port, TM1IO selection 0:I/O port 1:TM1IO
0	P1OMD0	I/O port, TM0IO/RMOUT selection 0:I/O port 1:TM0IO/RMOUT

■ Port 1 Real Time Output Control Register 0 (P1CNT0:0x03F7E)

bp	7	6	5	4	3	2	1	0
Flag	-	-	P1CNT05	P1CNT04	P1CNT03	P1CNT02	P1CNT01	P1CNT00
At reset	-	-	0	0	0	0	0	0
Access	-	-	R/W	R/W	R/W	R/W	R/W	R/W

bp	Flag	Description
7 6	- -	- -
5 4	P1CNT05 P1CNT04	P14 Real time control 00:I/O port (real time control disabled) 01:"1"(High) output 10:"0"(Low) output 11:"Hi-z" output
3 2	P1CNT03 P1CNT02	P12 Real time control 00:I/O port (real time control disabled) 01:"1"(High) output 10:"0"(Low) output 11:"Hi-z" output
1 0	P1CNT01 P1CNT00	P10 Real time control 00:I/O port (real time control disabled) 01:"1"(High) output 10:"0"(Low) output 11:"Hi-z" output

4.3.3 Block Diagram

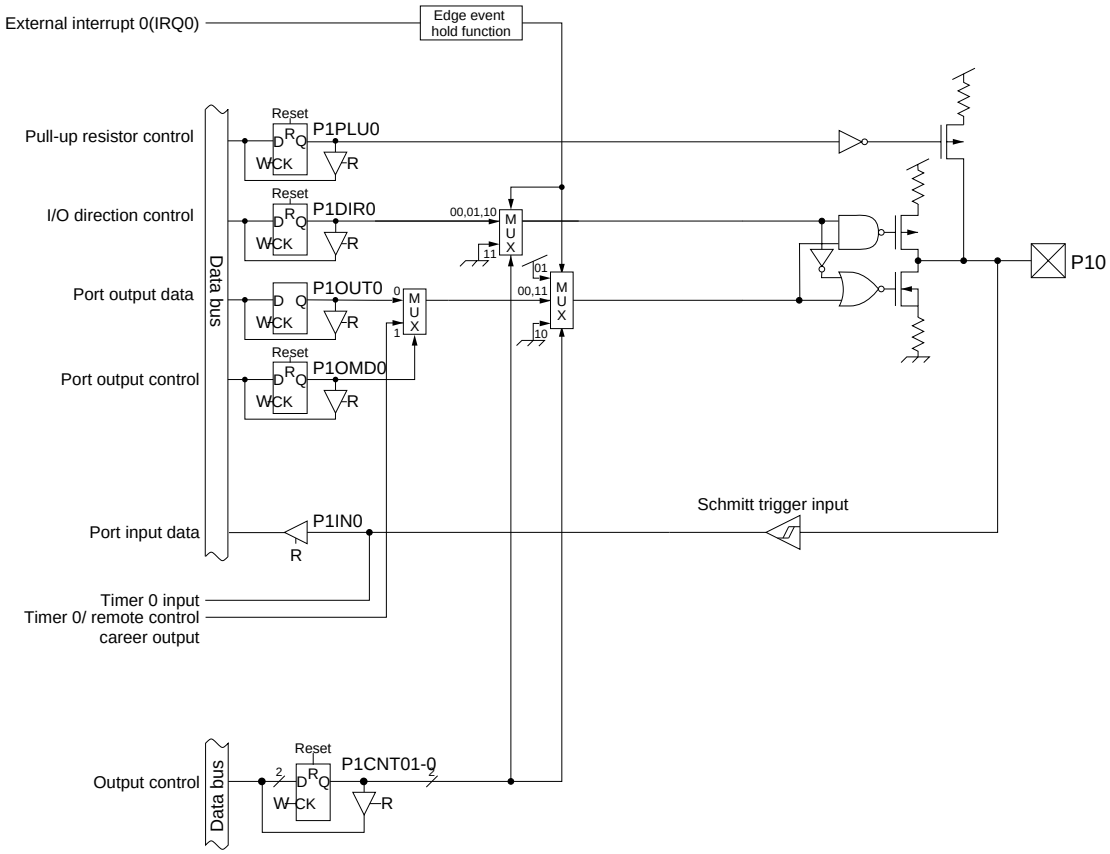


Figure:4.3.1 P10 Block Diagram

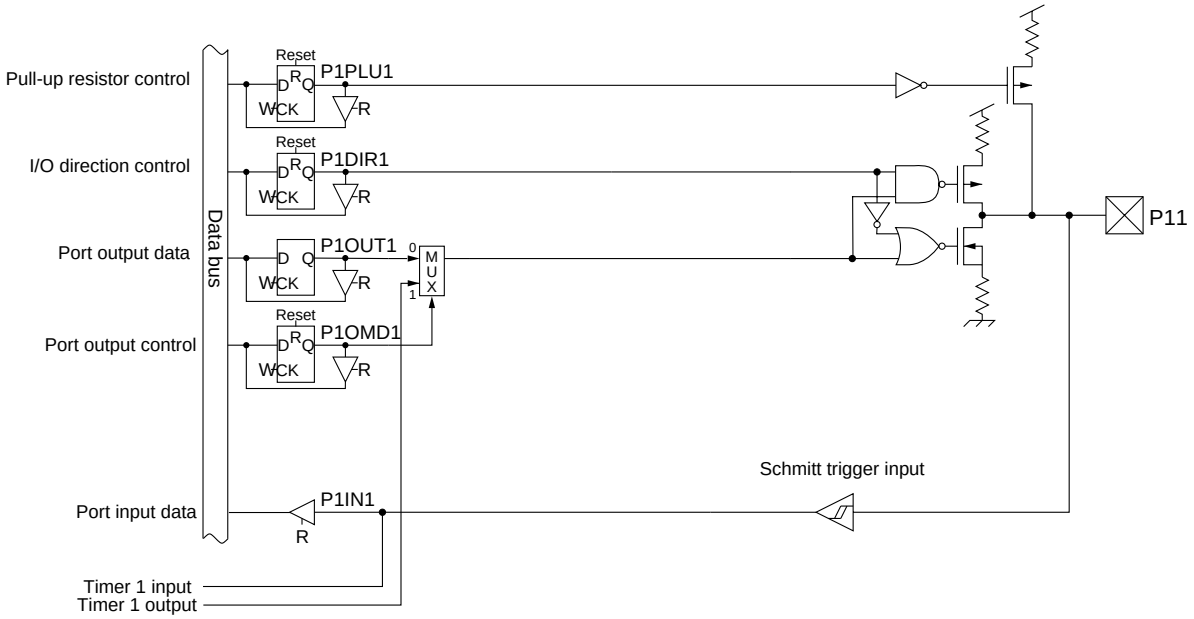


Figure:4.3.2 P11 Block Diagram

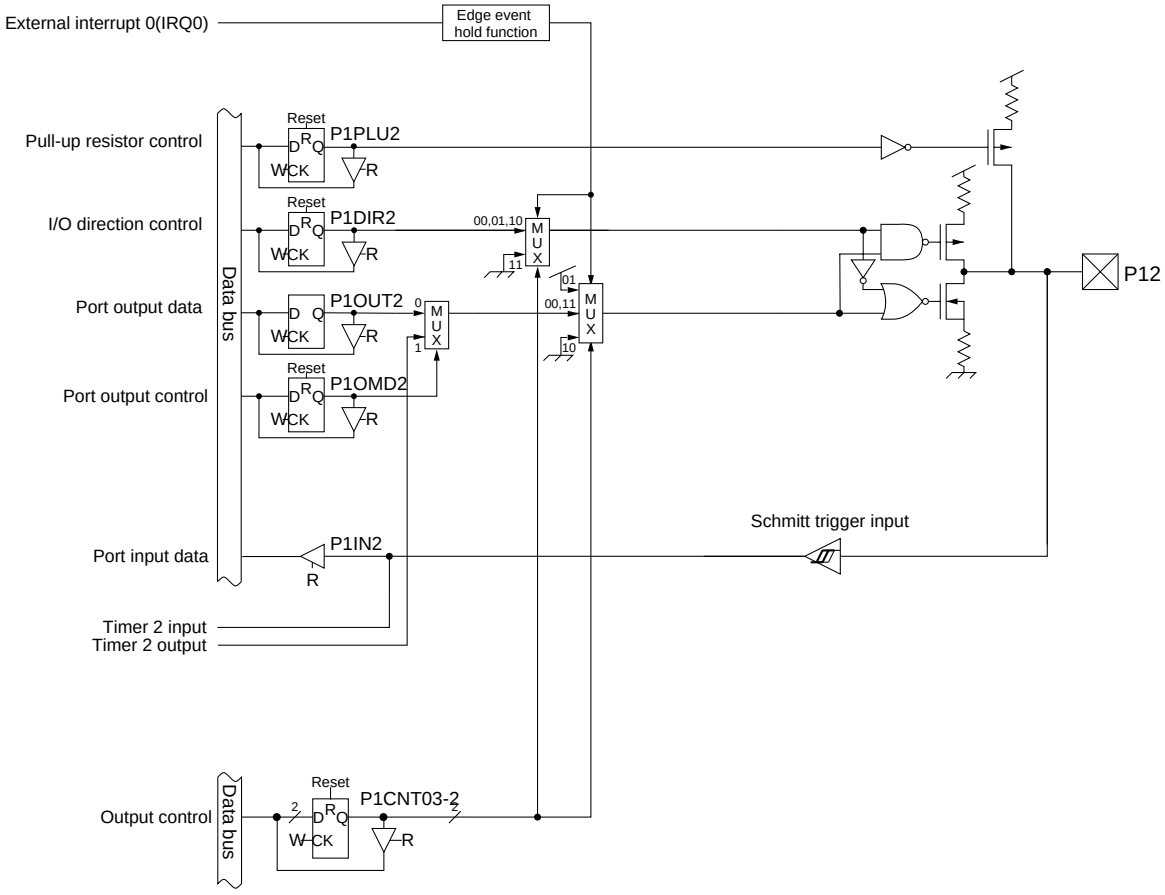


Figure:4.3.3 P12 Block Diagram

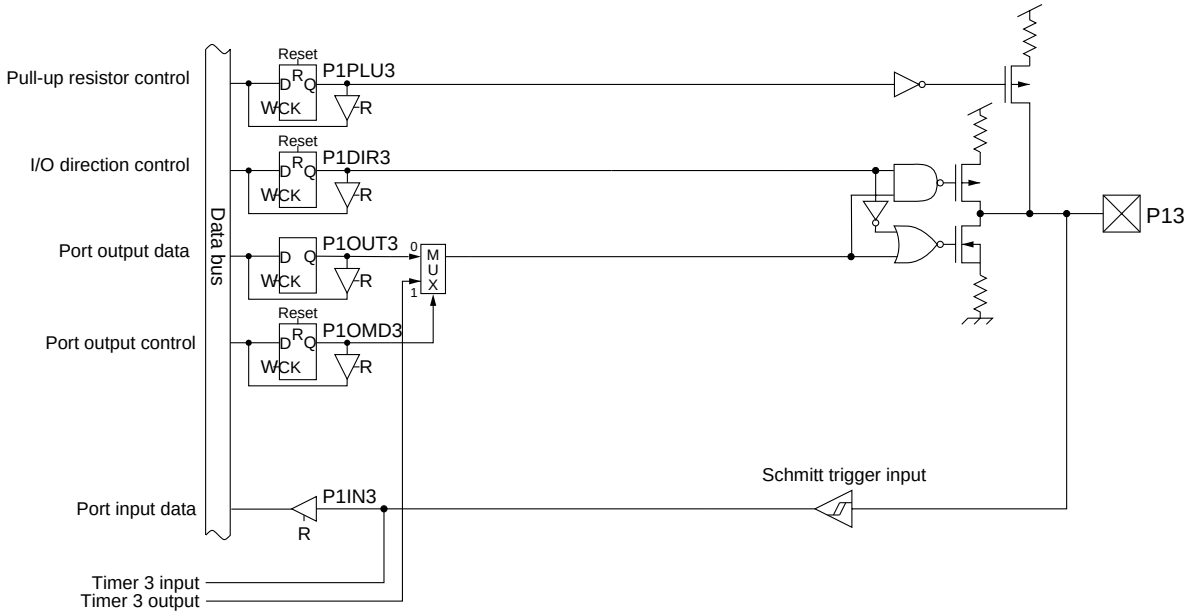


Figure:4.3.4 P13 Block Diagram

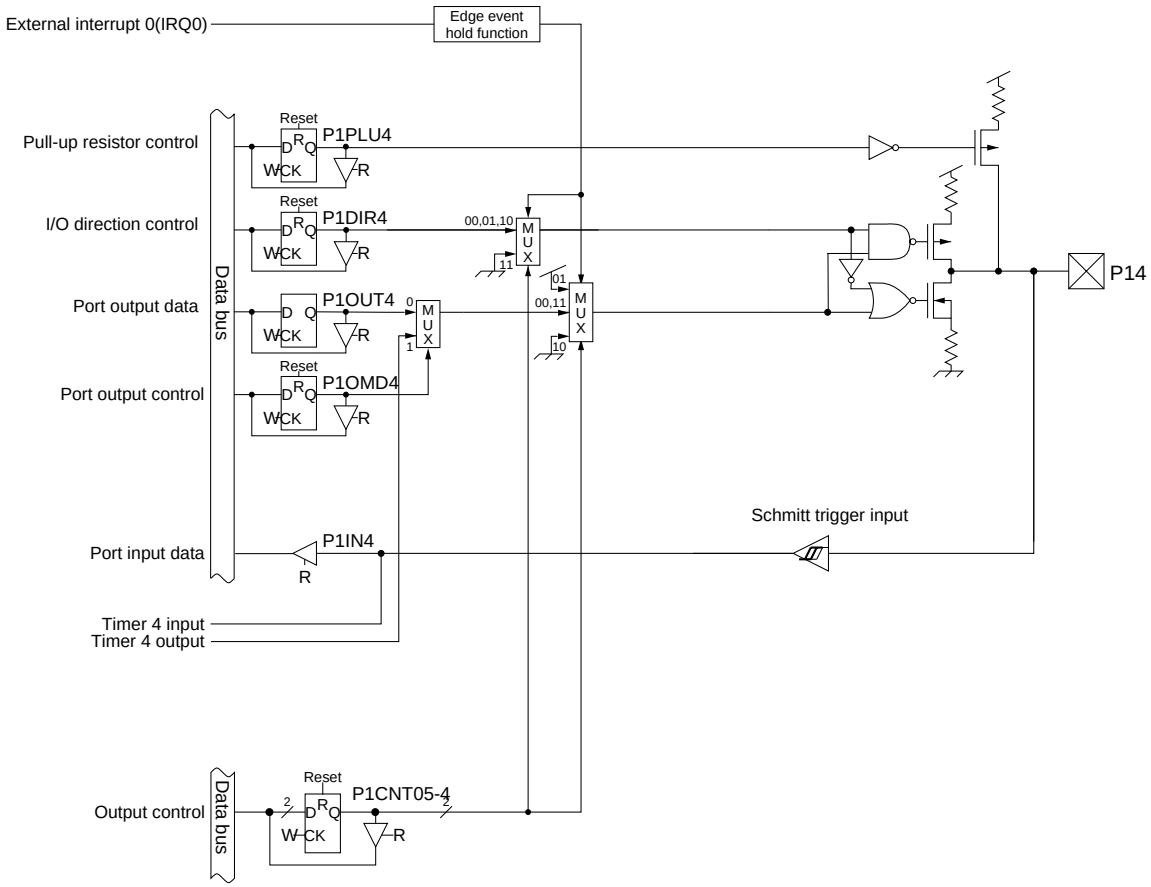


Figure:4.3.5 P14 Block Diagram

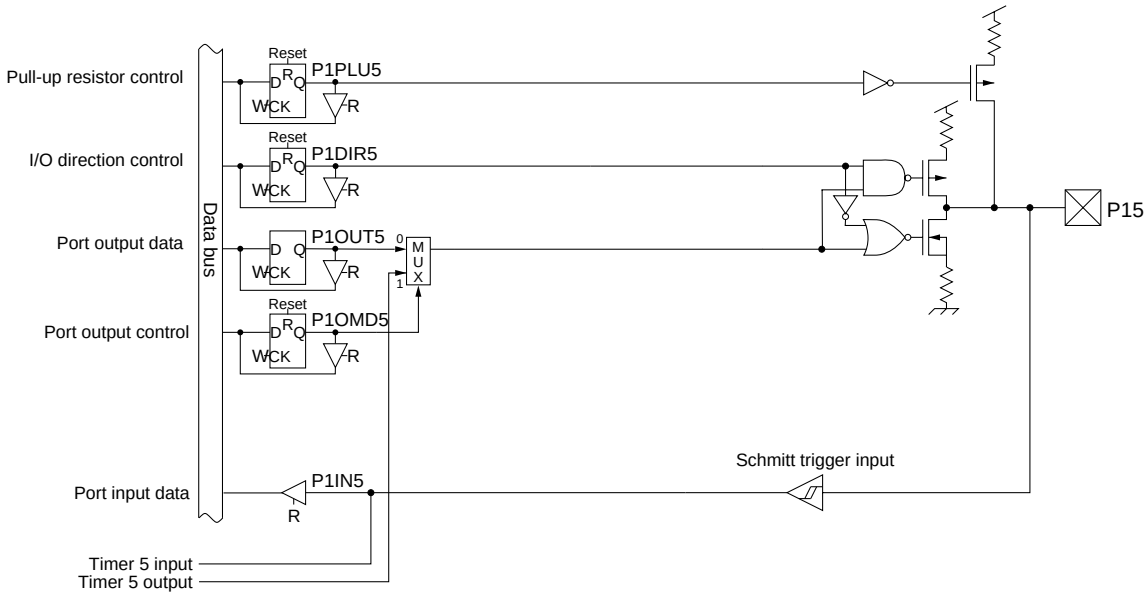


Figure:4.3.6 P15 Block Diagram

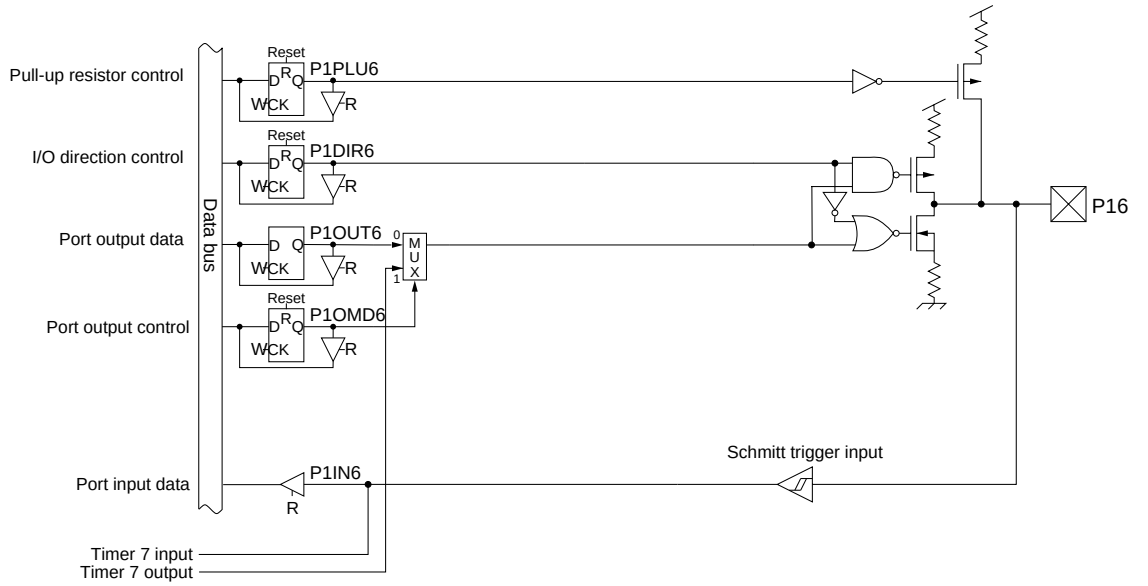


Figure:4.3.7 P16 Block Diagram

4.4 Port 2

4.4.1 Description

■ General Port Setup

To output the data to pins, set the control flag of the port 2 direction control register (P2DIR) to "1" to write the value of the port 2 output register (P2OUT).

To read input data of pins, set the control flag of the port 2 direction control register (P2DIR) to "0" to read the value of the port 2 input register (P2IN).

Each bit can be set individually as either an input or output by the port 2 I/O direction control register (P2DIR). The control flag of the port 2 direction control register (P2DIR) is set to "1" for output mode, and "0" for input mode.

Each bit can be set individually if pull-up resistor is added or not, by the port 2 pull-up resistor control register (P2PLU). Set the control flag of the port 2 pull-up resistor control register (P2PLU) to "1" to add pull-up resistor.

P27 is reset pin. When the software is reset, write "0" to the bp7 of the port 2 output register (P2OUT). Also, P27 is always added pull-up resistor.

■ Special Function Pin Setup

P20 is used as external interrupt 0 pin, as well.

P21 is used as external interrupt 1 pin, as well.

P22 is used as external interrupt 2 pin, as well.

External interrupt 2 can select either P22 or PD0 by setting of the external interrupt pin switching control register (IRQSEL). When IRQ2SEL flag of the external interrupt pin switching control register (IRQSEL) is 0, P22 is selected and 1, PD0 is selected.

P23 is used as external interrupt 3 pin, as well.

External interrupt 3 can select either P23 or PD1 by setting of the external interrupt pin switching control register (IRQSEL). When IRQ3SEL flag of the external interrupt pin switching control register (IRQSEL) is 0, P23 is selected and 1, PD1 is selected.

P24 is used as external interrupt 4 pin, as well.

P25 is used as external interrupt 5 pin, as well.

4.4.2 Registers

The following Table shows registers that control the Port 2

Table:4.4.1 Port 2 Control register

Registers	Address	R/W	Function	Page
P2OUT	0x03F12	R/W	Port 2 Output Register	IV-27
P2IN	0x03F22	R	Port 2 Input Register	IV-28
P2DIR	0x03F32	R/W	Port 2 Direction Control Register	IV-28
P2PLU	0x03F42	R/W	Port 2 Pull-up Resistor Control Register	IV-29

R/W:Readable/Writable

■ Port 2 Output Register(P2OUT:0x03F12)

bp	7	6	5	4	3	2	1	0
Flag	P2OUT7	-	P2OUT5	P2OUT4	P2OUT3	P2OUT2	P2OUT1	P2OUT0
At reset	x	-	x	x	x	x	x	x
Access	R/W	-	R/W	R/W	R/W	R/W	R/W	R/W

bp	Flag	Description
7 6 5 4 3 2 1 0	P2OUT7 - P2OUT5 P2OUT4 P2OUT3 P2OUT2 P2OUT1 P2OUT0	Output data 0:Output L(VSS level) 1:Output H(VDD level)

■ Port 2 Input Register(P2IN:0x03F22)

bp	7	6	5	4	3	2	1	0
Flag	P2IN7	-	P2IN5	P2IN4	P2IN3	P2IN2	P2IN1	P2IN0
At reset	x	-	x	x	x	x	x	x
Access	R	-	R	R	R	R	R	R

bp	Flag	Description
7 6 5 4 3 2 1 0	P2IN7 - P2IN5 P2IN4 P2IN3 P2IN2 P2IN1 P2IN0	Input data 0:Pin is L(VSS level) 1:Pin is H(VDD level)

■ Port 2 Direction Control Register(P2DIR:0x03F32)

bp	7	6	5	4	3	2	1	0
Flag	-	-	P2DIR5	P2DIR4	P2DIR3	P2DIR2	P2DIR1	P2DIR0
At reset	-	-	0	0	0	0	0	0
Access	-	-	R/W	R/W	R/W	R/W	R/W	R/W

bp	Flag	Description
7 6 5 4 3 2 1 0	- - P2DIR5 P2DIR4 P2DIR3 P2DIR2 P2DIR1 P2DIR0	I/O mode selection 0:Input mode 1:Output mode

■ Port 2 Pull-up Resistor Control Register(P2PLU:0x03F42)

bp	7	6	5	4	3	2	1	0
Flag	-	-	P2PLU5	P2PLU4	P2PLU3	P2PLU2	P2PLU1	P2PLU0
At reset	-	-	0	0	0	0	0	0
Access	-	-	R/W	R/W	R/W	R/W	R/W	R/W

bp	Flag	Description
7 6 5 4 3 2 1 0	- - P2PLU5 P2PLU4 P2PLU3 P2PLU2 P2PLU1 P2PLU0	Pull-up resistor selection 0:Not added 1:Added

4.4.3 Block Diagram

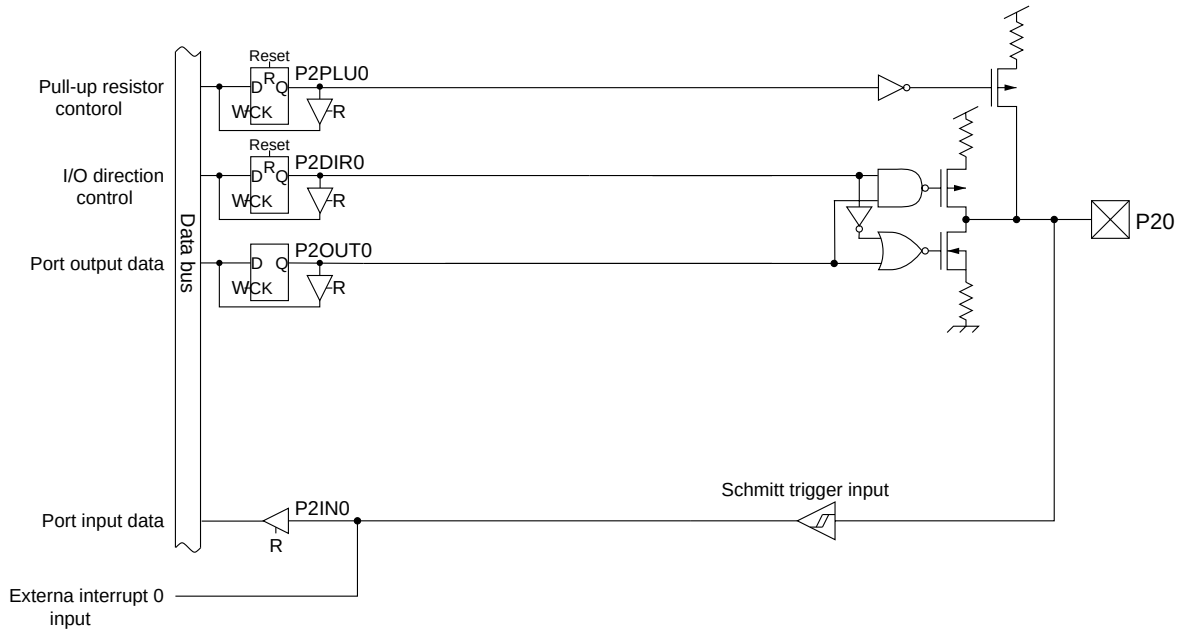


Figure:4.4.1 P20 Block Diagram

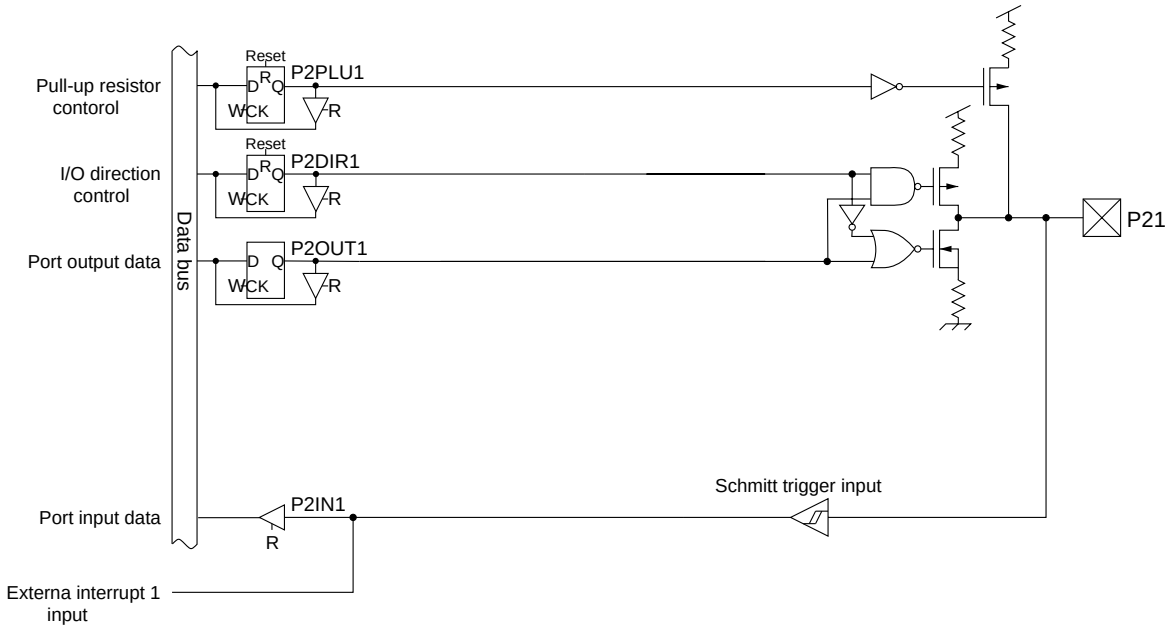


Figure:4.4.2 P21 Block Diagram

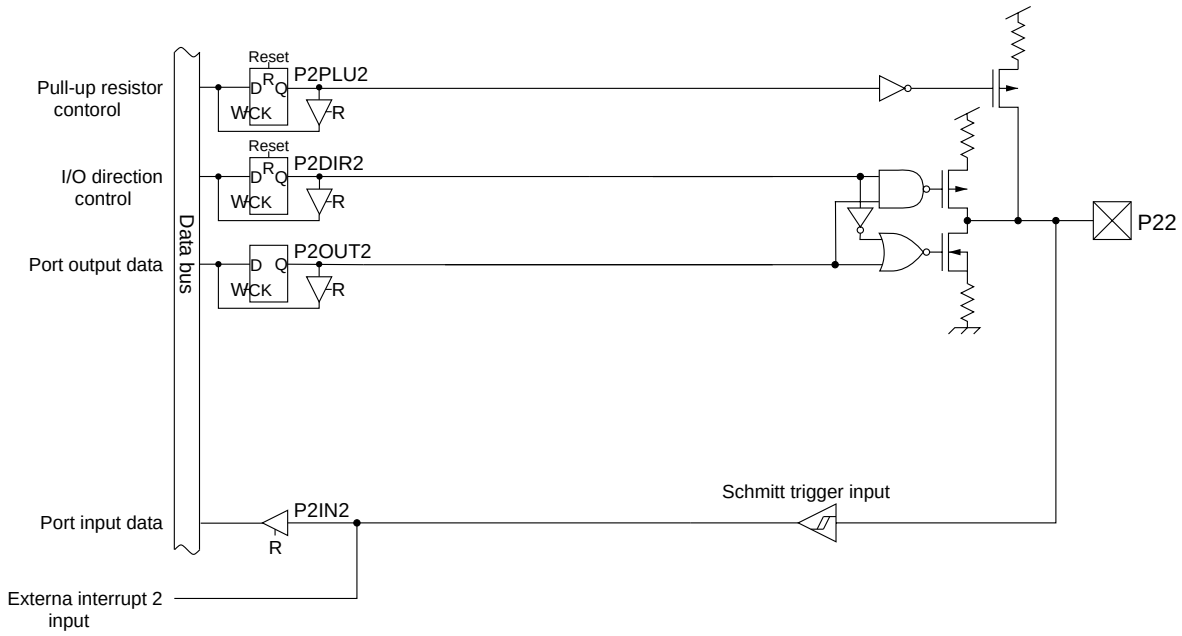


Figure:4.4.3 P22 Block Diagram

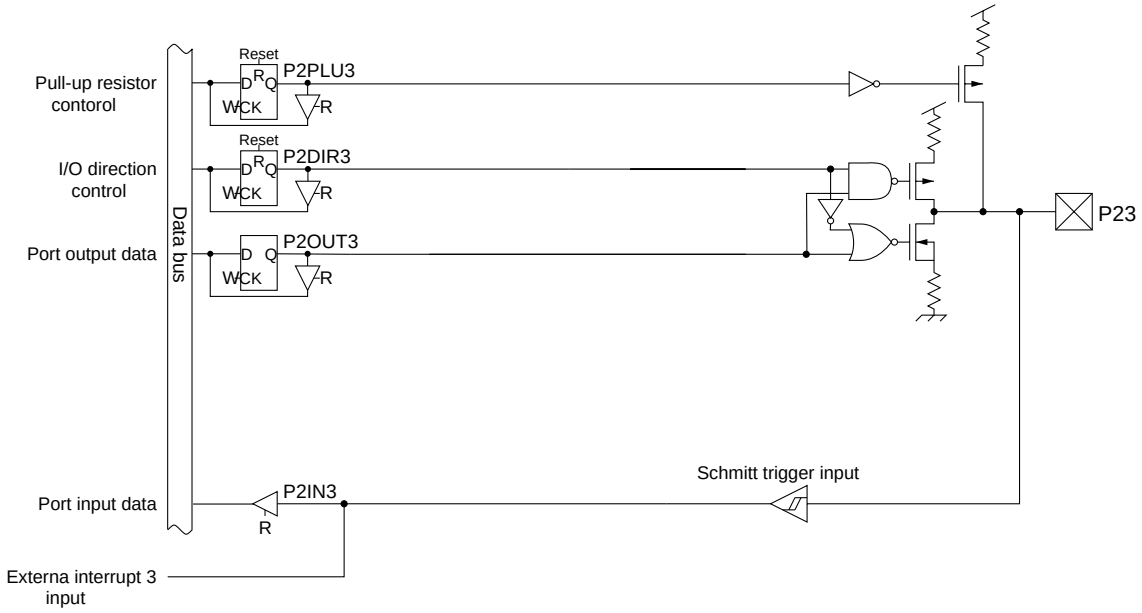


Figure:4.4.4 P23 Block Diagram

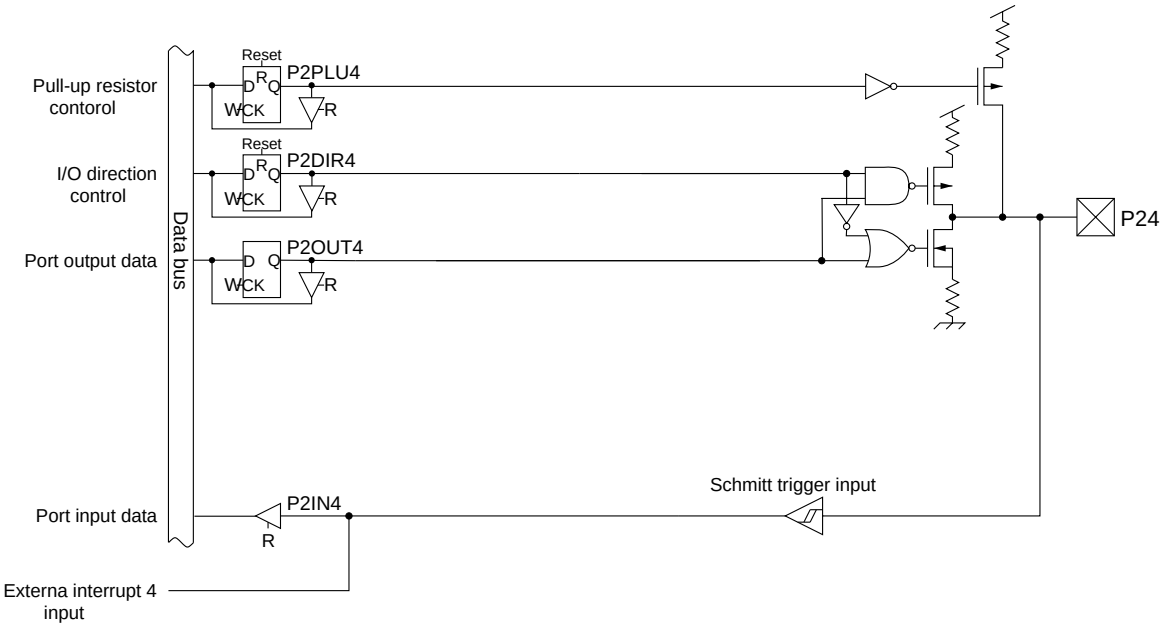


Figure:4.4.5 P24 Block Diagram

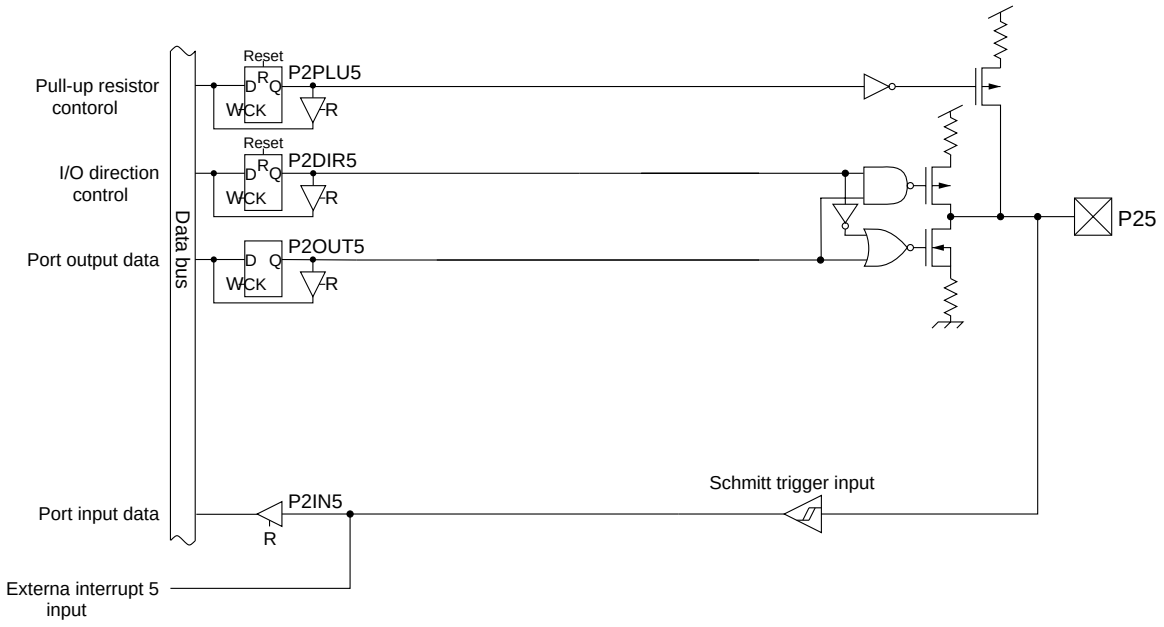


Figure:4.4.6 P25 Block Diagram

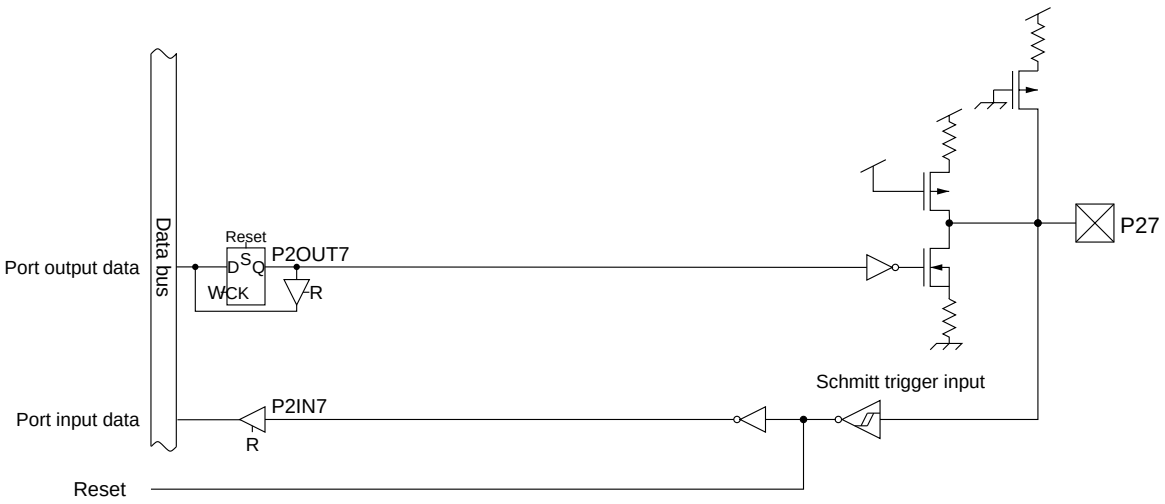


Figure:4.4.7 P27 Block Diagram

4.5 Port 3

4.5.1 Description

■ General Port Setup

To output the data to pins, set the control flag of the port 3 direction control register (P3DIR) to "1" to write the value of the port 3 output register (P3OUT).

To read input data of pins, set the control flag of the port 3 direction control register (P3DIR) to "0" to read the value of the port 3 input register (P3IN).

Each bit can be set individually as either an input or output by the port 3 I/O direction control register (P3DIR). The control flag of the port 3 direction control register (P3DIR) is set to "1" for output mode, and "0" for input mode.

Each bit can be set individually if pull-up resistor is added or not, by the port 3 pull-up resistor control register (P3PLU). Set the control flag of the port 3 pull-up resistor control register (P3PLU) to "1" to add pull-up resistor.

P30, P32, P33, and P35 can select the Nch open-drain output by each bit by the port 3 Nch open-drain control register (P3ODC). The port 3 output mode register (P3OMD) is set to "1" for the Nch open-drain output and "0" for the push-pull output.

■ Special Function Pin Setup

P30 is used as output pin of the serial 1 transmission data or the UART 1 transmission data, as well. When the SC1SBOS flag of the serial interface 1 mode register 1 (SC1MD1) is set to "1", it is output pin of the serial data. Also, the push-pull output or the Nch open-drain output can be selected by the setup of the port 3 Nch open-drain control register (P3ODC).

P31 is used as input pin of the serial 1 reception data or the UART 1 reception data, as well.

P32 is used as I/O pin of the serial 1 clock, as well. When the SC1SBTS flag of the serial interface 1 mode register 1 (SC1MD1) is set to "1", it is output pin of the serial clock. Also, the push-pull output or the Nch open-drain output can be selected by the setup of the port 3 Nch open-drain control register (P3ODC).

P33 is used as output pin of the serial 3 transmission data or the IIC3 transmission data, as well. When the SC3SBOS flag of the serial interface 3 mode register 1 (SC3MD1) is set to "1", it is output pin of the serial data. Also, the push-pull output or the Nch open-drain output can be selected by the setup of the port 3 Nch open-drain control register (P3ODC).

P34 is used as input pin of the serial 3 reception data.

P35 is used as I/O pin of the serial 3 clock, as well. When the SC3SBTS flag of the serial interface 3 mode register 1 (SC3MD1) is set to "1", it is output pin of the serial clock. Also, the push-pull output or the Nch open-drain output can be selected by the setup of the port 3 Nch open-drain control register (P3ODC).

4.5.2 Registers

The following Table shows registers that control the Port 3

Table:4.5.1 Port 3control register

Registers	Address	R/W	Function	Page
P3OUT	0x03F13	R/W	Port 3 Output Register	IV-35
P3IN	0x03F23	R	Port 3 Input Register	IV-36
P3DIR	0x03F33	R/W	Port 3 Direction Control Register	IV-36
P3PLU	0x03F43	R/W	Port 3 Pull-up Resistor Control Register	IV-37
P3ODC	0x03F2C	R/W	Port 3 Nch Open-drain Control Register	IV-37

R/W:Readable/Writable

■ Port 3 Output Register(P3OUT:0x03F13)

bp	7	6	5	4	3	2	1	0
Flag	-	-	P3OUT5	P3OUT4	P3OUT3	P3OUT2	P3OUT1	P3OUT0
At reset	-	-	x	x	x	x	x	x
Access	-	-	R/W	R/W	R/W	R/W	R/W	R/W

bp	Flag	Description
7 6 5 4 3 2 1 0	- - P3OUT5 P3OUT4 P3OUT3 P3OUT2 P3OUT1 P3OUT0	Output data 0:Output L(VSS level) 1:Output H(VDD level)

■ Port 3 Input Register(P3IN:0x03F23)

bp	7	6	5	4	3	2	1	0
Flag	-	-	P3IN5	P3IN4	P3IN3	P3IN2	P3IN1	P3IN0
At reset	-	-	x	x	x	x	x	x
Access	-	-	R	R	R	R	R	R

bp	Flag	Description
7 6 5 4 3 2 1 0	- - P3IN5 P3IN4 P3IN3 P3IN2 P3IN1 P3IN0	Input data 0:Pin is L(VSS level) 1:Pin is H(VDD level)

■ Port 3 Direction Control Register(P3DIR:0x03F33)

bp	7	6	5	4	3	2	1	0
Flag	-	-	P3DIR5	P3DIR4	P3DIR3	P3DIR2	P3DIR1	P3DIR0
At reset	-	-	0	0	0	0	0	0
Access	-	-	R/W	R/W	R/W	R/W	R/W	R/W

bp	Flag	Description
7 6 5 4 3 2 1 0	- - P3DIR5 P3DIR4 P3DIR3 P3DIR2 P3DIR1 P3DIR0	I/O mode selection 0:Input mode 1:Output mode

■ Port 3 Pull-up Resistor Control Register(P3PLU:0x03F43)

bp	7	6	5	4	3	2	1	0
Flag	-	-	P3PLU5	P3PLU4	P3PLU3	P3PLU2	P3PLU1	P3PLU0
At reset	-	-	0	0	0	0	0	0
Access	-	-	R/W	R/W	R/W	R/W	R/W	R/W

bp	Flag	Description
7 6 5 4 3 2 1 0	- - P3PLU5 P3PLU4 P3PLU3 P3PLU2 P3PLU1 P3PLU0	Pull-up resistor selection 0:Not added 1:Added

■ Port 3 Nch Open-drain Control Register(P3ODC:0x03F2C)

bp	7	6	5	4	3	2	1	0
Flag	-	-	P3ODC5	-	P3ODC3	P3ODC2	-	P3ODC0
At reset	-	-	0	-	0	0	-	0
Access	-	-	R/W	-	R/W	R/W	-	R/W

bp	Flag	Description
7 6 5 4 3 2 1 0	- - P3ODC5 - P3ODC3 P3ODC2 - P3ODC0	Nch open-drain output selection 0:Push/pull output 1:Nch open-drain output

4.5.3 Block Diagram

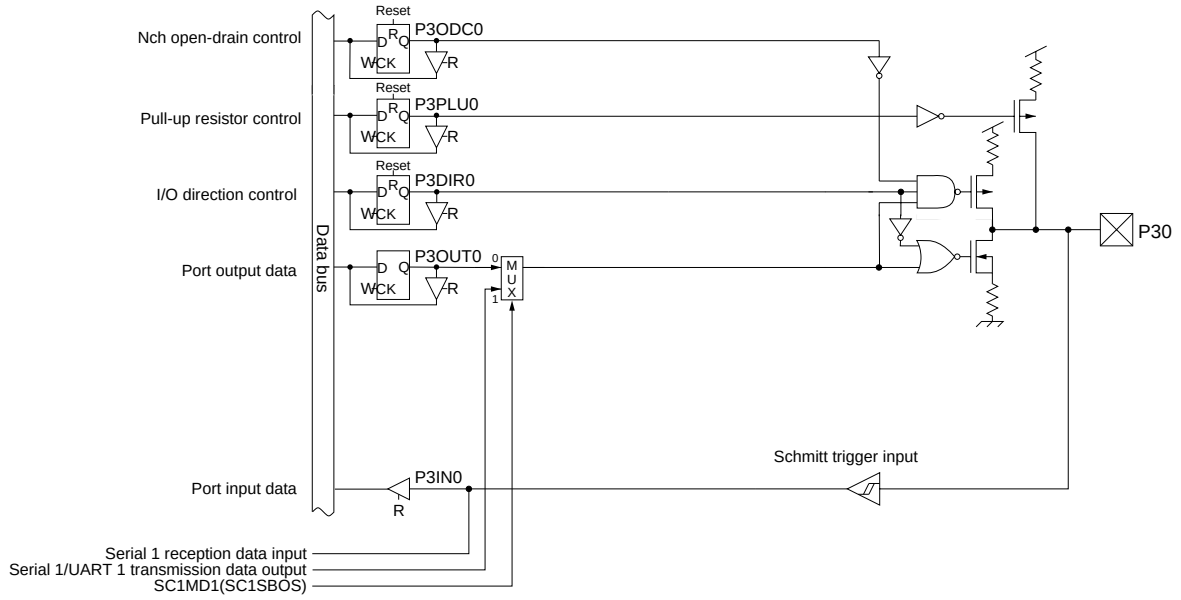


Figure:4.5.1 P30 Block Diagram

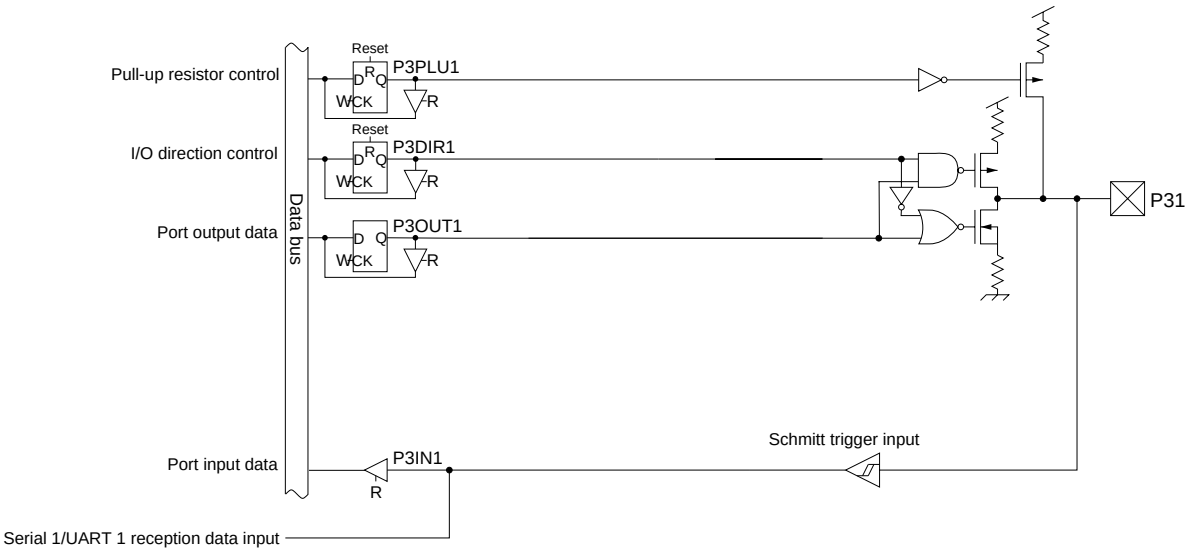


Figure:4.5.2 P31 Block Diagram

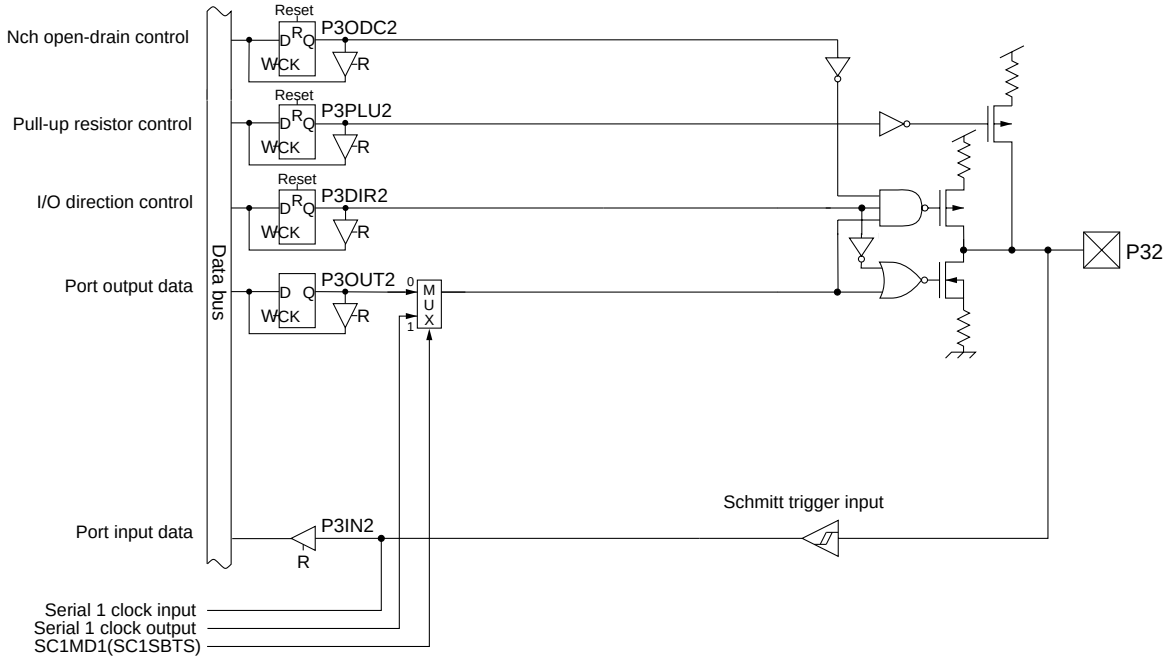


Figure:4.5.3 P32 Block Diagram

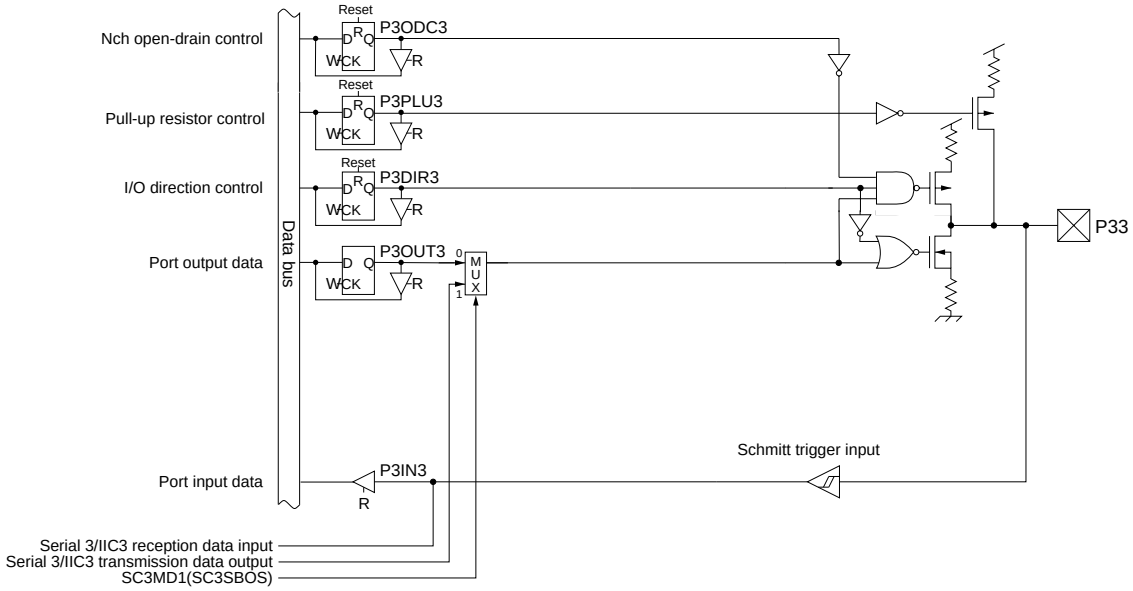


Figure:4.5.4 P33 Block Diagram

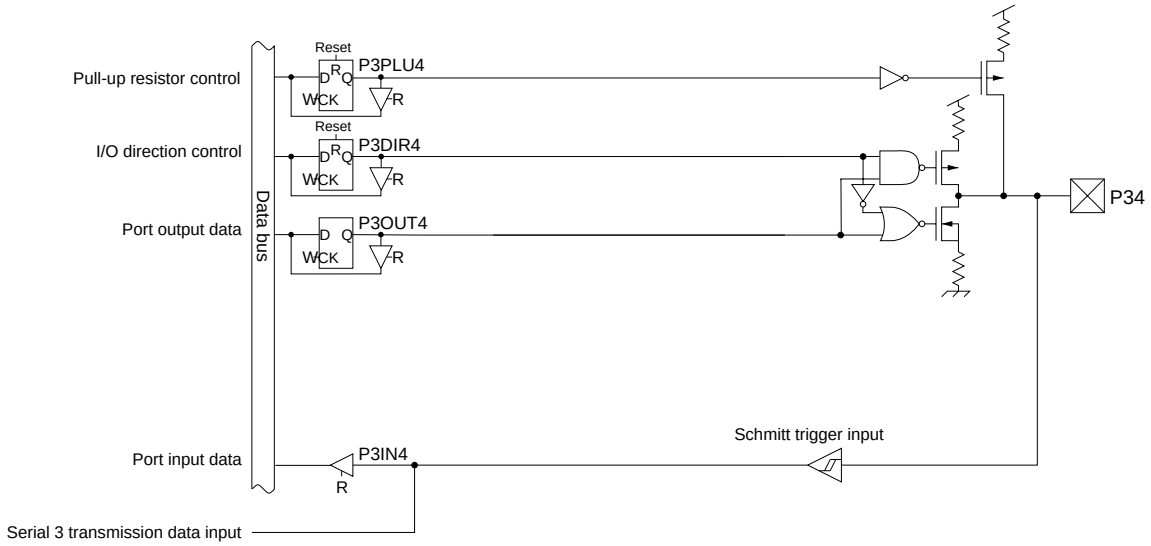


Figure:4.5.5 P34 Block Diagram

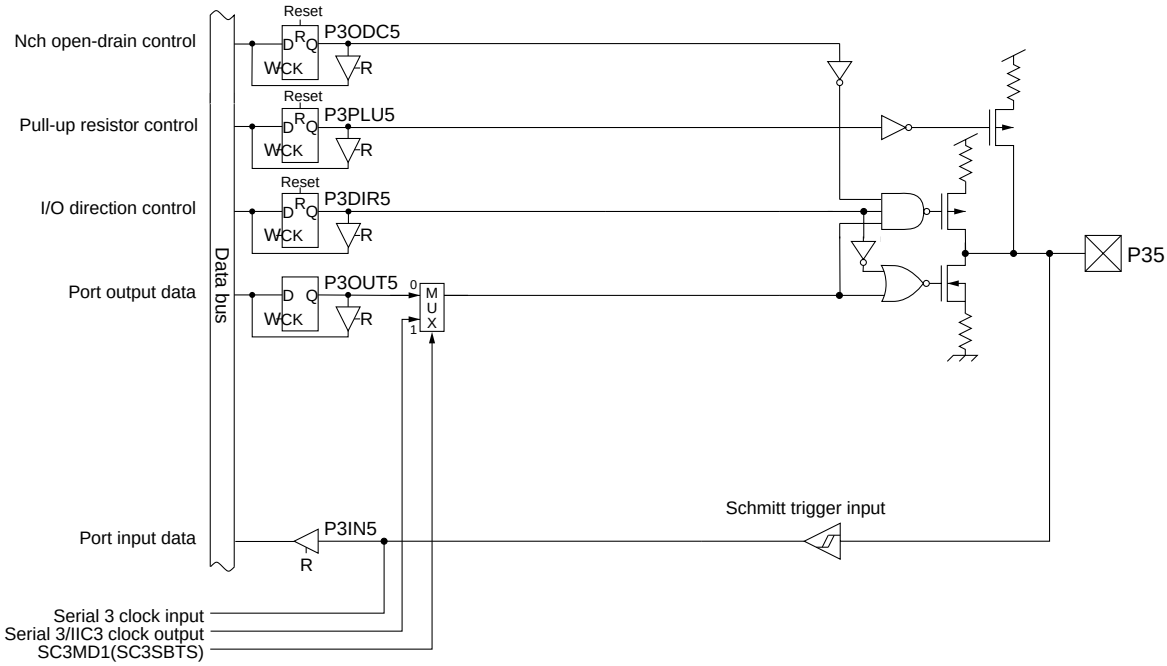


Figure:4.5.6 P35 Block Diagram

4.6 Port 4

4.6.1 Description

■ General Port Setup

To output the data to pins, set the control flag of the port 4 direction control register (P4DIR) to "1" to write the value of the port 4 output register (P4OUT).

To read input data of pins, set the control flag of the port 4 direction control register (P4DIR) to "0" to read the value of the port 4 input register (P4IN).

Each bit can be set individually as either an input or output by the port 4 I/O direction control register (P4DIR). The control flag of the port 4 direction control register (P4DIR) is set to "1" for output mode, and "0" for input mode.

Each bit can be set individually if pull-up or pull-down resistor is added or not, by the port 4 pull-up/pull-down resistor control register (P4PLU). Set the control flag of the port 4 pull-up/pull-down resistor control register (P4PLU) to "1" to add pull-up/pull-down resistor.

Port 4 can be selected to add pull-up resistor or pull-down resistor by bp0 of the pull-up/pull-down resistor selection register (SELUD).

P40, P42 can select the Nch open-drain output by each bit by the port 4 Nch open-drain control register (P4ODC). The port 4 output mode register (P4OMD) is set to "1" for the Nch open-drain output and "0" for the push-pull output.

■ Special Function Pin Setup

P40 is used as output pin of the serial 4 transmission data or the UART 4 transmission data, as well. When the SC4SBOS flag of the serial interface 4 mode register 1 (SC4MD1) is set to "1", it is output pin of the serial data. Also, the push-pull output or the Nch open-drain output can be selected by the setup of the port 4 Nch open-drain control register (P4ODC).

P41 is used as input pin of the serial 4 reception data or the UART 4 reception data, as well.

P42 is used as I/O pin of the serial 4 clock, as well. When the SC4SBTS flag of the serial interface 4 mode register 1 (SC4MD1) is set to "1", it is output pin of the serial clock. Also, the push-pull output or the Nch open-drain output can be selected by the setup of the port 4 Nch open-drain control register (P4ODC).

4.6.2 Registers

The following Table shows registers that control the Port 4

Table:4.6.1 Port 4control register

Registers	Address	R/W	Function	Page
P4OUT	0x03F14	R/W	Port 4 Output Register	IV-42
P4IN	0x03F24	R	Port 4 Input Register	IV-43
P4DIR	0x03F34	R/W	Port 4 Direction Control Register	IV-43
P4PLU	0x03F44	R/W	Port 4 Pull-up/Pull-down Resistor Control Register	IV-44
P4ODC	0x03F3C	R/W	Port 4 Nch Open-drain Control Register	IV-44
SELUD	0x03F4B	R/W	Pull-up/Pull-down Resistor Selection Register	IV-45

R/W:Readable/Writable

■ Port 4 Output Register(P4OUT:0x03F14)

bp	7	6	5	4	3	2	1	0
Flag	-	-	-	-	P4OUT3	P4OUT2	P4OUT1	P4OUT0
At reset	-	-	-	-	x	x	x	x
Access	-	-	-	-	R/W	R/W	R/W	R/W

bp	Flag	Description
7 6 5 4 3 2 1 0	- - - - P4OUT3 P4OUT2 P4OUT1 P4OUT0	Output data 0:Output L(VSS level) 1:Output H(VDD level)

■ Port 4 Input Register(P4IN:0x03F24)

bp	7	6	5	4	3	2	1	0
Flag	-	-	-	-	P4IN3	P4IN2	P4IN1	P4IN0
At reset	-	-	-	-	x	x	x	x
Access	-	-	-	-	R	R	R	R

bp	Flag	Description
7 6 5 4 3 2 1 0	- - - - P4IN3 P4IN2 P4IN1 P4IN0	Input data 0:Pin is L(VSS level) 1:Pin is H(VDD level)

■ Port 4 Direction Control Register(P4DIR:0x03F34)

bp	7	6	5	4	3	2	1	0
Flag	-	-	-	-	P4DIR3	P4DIR2	P4DIR1	P4DIR0
At reset	-	-	-	-	0	0	0	0
Access	-	-	-	-	R/W	R/W	R/W	R/W

bp	Flag	Description
7 6 5 4 3 2 1 0	- - - - P4DIR3 P4DIR2 P4DIR1 P4DIR0	I/O mode selection 0:Input mode 1:Output mode

■ Port 4 Pull-up/Pull-down Resistor Control Register(P4PLU:0x03F44)

bp	7	6	5	4	3	2	1	0
Flag	-	-	-	-	P4PLU3	P4PLU2	P4PLU1	P4PLU0
At reset	-	-	-	-	0	0	0	0
Access	-	-	-	-	R/W	R/W	R/W	R/W

bp	Flag	Description
7 6 5 4 3 2 1 0	- - - - P4PLU3 P4PLU2 P4PLU1 P4PLU0	Pull-up/pull-down resistor selection 0:Not added 1:Added

■ Port 4 Nch Open-drain Control Register(P4ODC:0x03F3C)

bp	7	6	5	4	3	2	1	0
Flag	-	-	-	-	-	P4ODC2	-	P4ODC0
At reset	-	-	-	-	-	0	-	0
Access	-	-	-	-	-	R/W	-	R/W

bp	Flag	Description
7 6 5 4 3 2 1 0	- - - - - P4ODC2 - P4ODC0	Nch open-drain output selection 0:Push/pull output 1:Nch open-drain output

■ Pull-up/Pull-down Resistor Selection Register(SELUD:0x03F4B)

bp	7	6	5	4	3	2	1	0
Flag	-	-	-	-	-	PADWN	P7DWN	P4DWN
At reset	-	-	-	-	-	0	0	0
Access	-	-	-	-	-	R/W	R/W	R/W

bp	Flag	Description
7	-	-
6	-	-
5	-	-
4	-	-
3	-	-
2	PADWN	Port A pull-up/pull-down selection 0:Pull-up 1:Pull-down
1	P7DWN	Port 7 pull-up/pull-down selection 0:Pull-up 1:Pull-down
0	P4DWN	Port 4 pull-up/pull-down selection 0:Pull-up 1:Pull-down

4.6.3 Block Diagram

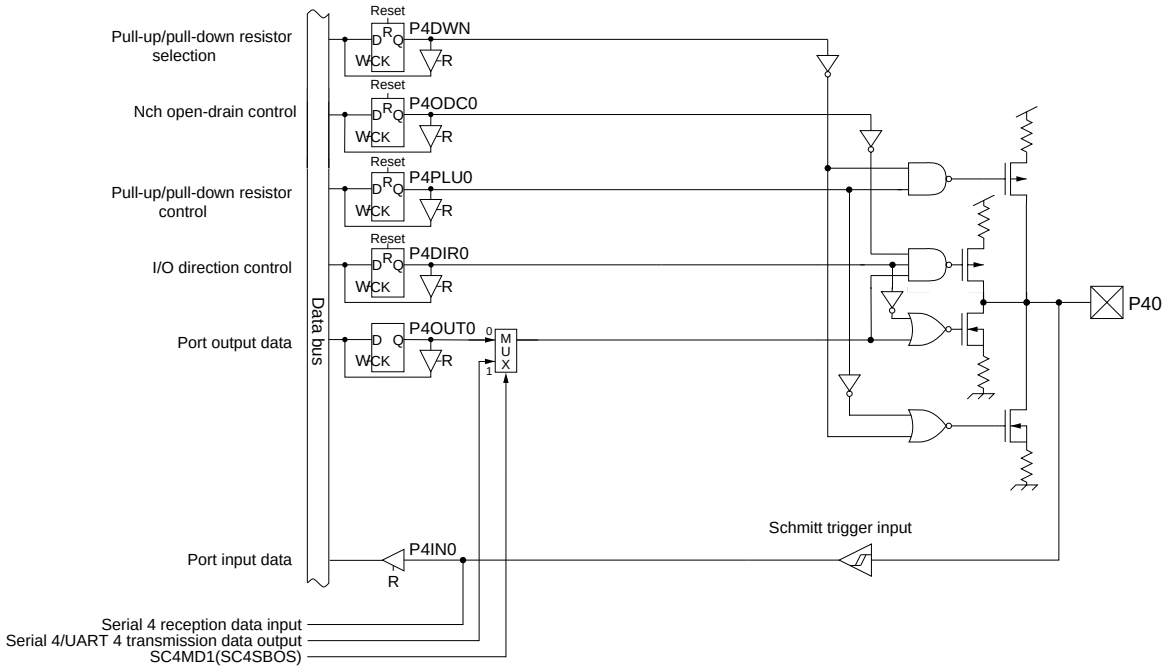


Figure:4.6.1 P40 Block Diagram

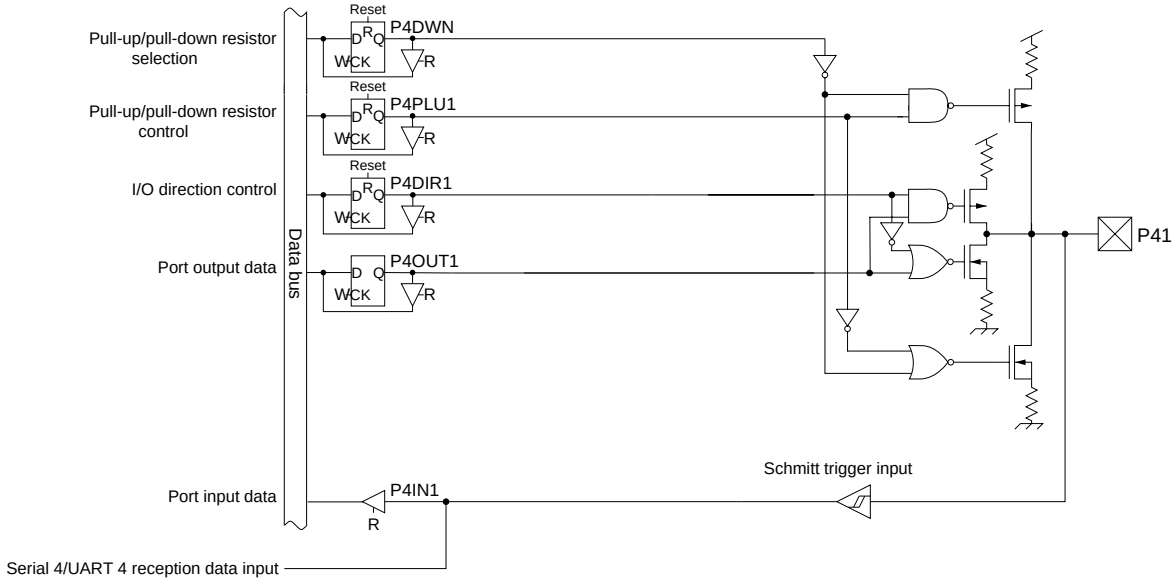


Figure:4.6.2 P41 Block Diagram

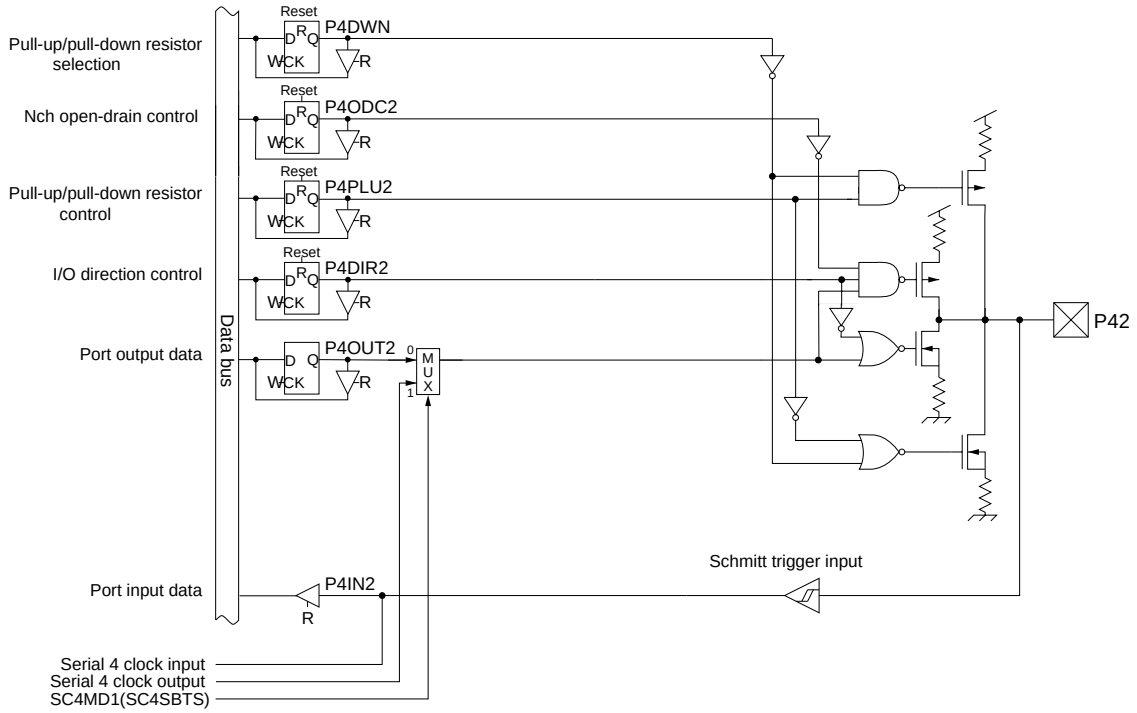


Figure:4.6.3 P42 Block Diagram

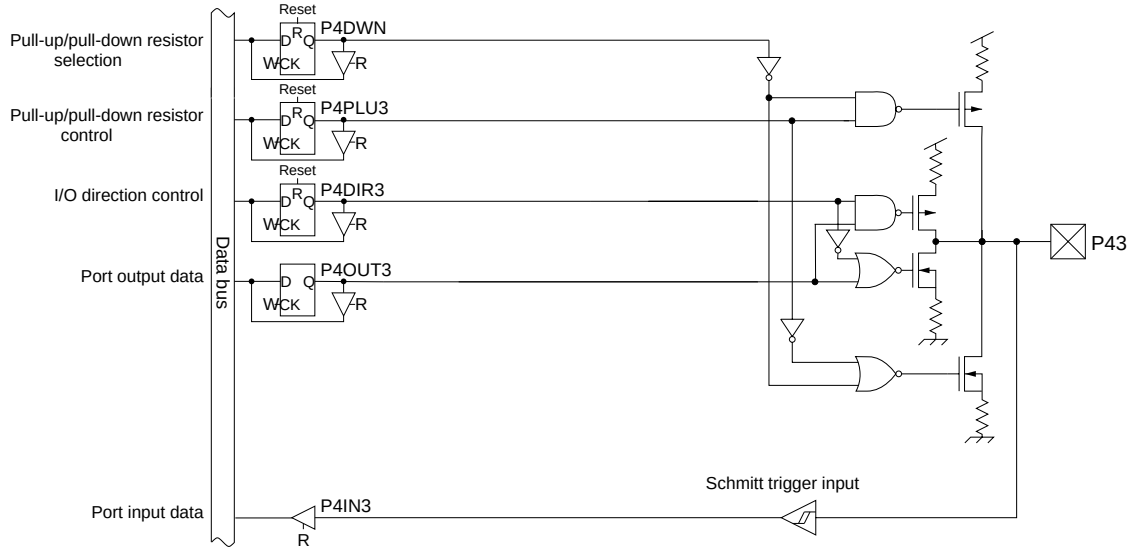


Figure:4.6.4 P43 Block Diagram

4.7 Port 5

4.7.1 Description

■ General Port Setup

To output the data to pins, set the control flag of the port 5 direction control register (P5DIR) to "1" to write the value of the port 5 output register (P5OUT).

To read input data of pins, set the control flag of the port 5 direction control register (P5DIR) to "0" to read the value of the port 5 input register (P5IN).

Each bit can be set individually as either an input or output by the port 5 I/O direction control register (P5DIR). The control flag of the port 5 direction control register (P5DIR) is set to "1" for output mode, and "0" for input mode.

Each bit can be set individually if pull-up resistor is added or not, by the port 5 pull-up resistor control register (P5PLU). Set the control flag of the port 5 pull-up resistor control register (P5PLU) to "1" to add pull-up resistor.

■ Special Function Pin Setup

P50 is address output pin to the external extension memory at the processor mode or the memory extension mode. These modes are set to the output modes automatically.

P51 is address output pin to the external extension memory at the processor mode or the memory extension mode. These modes are set to the output modes automatically.

P52 is address output pin to the external extension memory at the processor mode or the memory extension mode. These modes are set to the output modes automatically.

P53 is address output pin to the external extension memory at the processor mode or the memory extension mode. These modes are set to the output modes automatically.

P54 is address output pin to the external extension memory at the processor mode or the memory extension mode. These modes are set to the output modes automatically.

P55 is address output pin to the external extension memory at the processor mode or the memory extension mode. These modes are set to the output modes automatically.

P56 is address output pin to the external extension memory at the processor mode or the memory extension mode. These modes are set to the output modes automatically.

P57 is address output pin to the external extension memory at the processor mode or the memory extension mode. These modes are set to the output modes automatically.

4.7.2 Registers

The following Table shows registers that control the Port 5

Table:4.7.1 Port 5control register

Registers	Address	R/W	Function	Page
P5OUT	0x03F15	R/W	Port 5 Output Register	IV-49
P5IN	0x03F25	R	Port 5 Input Register	IV-50
P5DIR	0x03F35	R/W	Port 5 Direction Control Register	IV-50
P5PLU	0x03F45	R/W	Port 5 Pull-up Resistor Control Register	IV-51

R/W:Readable/Writable

■ Port 5 Output Register(P5OUT:0x03F15)

bp	7	6	5	4	3	2	1	0
Flag	P5OUT7	P5OUT6	P5OUT5	P5OUT4	P5OUT3	P5OUT2	P5OUT1	P5OUT0
At reset	x	x	x	x	x	x	x	x
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bp	Flag	Description
7 6 5 4 3 2 1 0	P5OUT7 P5OUT6 P5OUT5 P5OUT4 P5OUT3 P5OUT2 P5OUT1 P5OUT0	Output data 0:Output L(VSS level) 1:Output H(VDD level)

■ Port 5 Input Register(P5IN:0x03F25)

bp	7	6	5	4	3	2	1	0
Flag	P5IN7	P5IN6	P5IN5	P5IN4	P5IN3	P5IN2	P5IN1	P5IN0
At reset	x	x	x	x	x	x	x	x
Access	R	R	R	R	R	R	R	R

bp	Flag	Description
7 6 5 4 3 2 1 0	P5IN7 P5IN6 P5IN5 P5IN4 P5IN3 P5IN2 P5IN1 P5IN0	Input data 0:Pin is L(VSS level) 1:Pin is H(VDD level)

■ Port 5 Direction Control Register(P5DIR:0x03F35)

bp	7	6	5	4	3	2	1	0
Flag	P5DIR7	P5DIR6	P5DIR5	P5DIR4	P5DIR3	P5DIR2	P5DIR1	P5DIR0
At reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bp	Flag	Description
7 6 5 4 3 2 1 0	P5DIR7 P5DIR6 P5DIR5 P5DIR4 P5DIR3 P5DIR2 P5DIR1 P5DIR0	I/O mode selection 0:Input mode 1:Output mode

■ Port 5 Pull-up Resistor Control Register(P5PLU:0x03F45)

bp	7	6	5	4	3	2	1	0
Flag	P5PLU7	P5PLU6	P5PLU5	P5PLU4	P5PLU3	P5PLU2	P5PLU1	P5PLU0
At reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bp	Flag	Description
7 6 5 4 3 2 1 0	P5PLU7 P5PLU6 P5PLU5 P5PLU4 P5PLU3 P5PLU2 P5PLU1 P5PLU0	Pull-up resistor selection 0:Not added 1:Added

4.7.3 Block Diagram

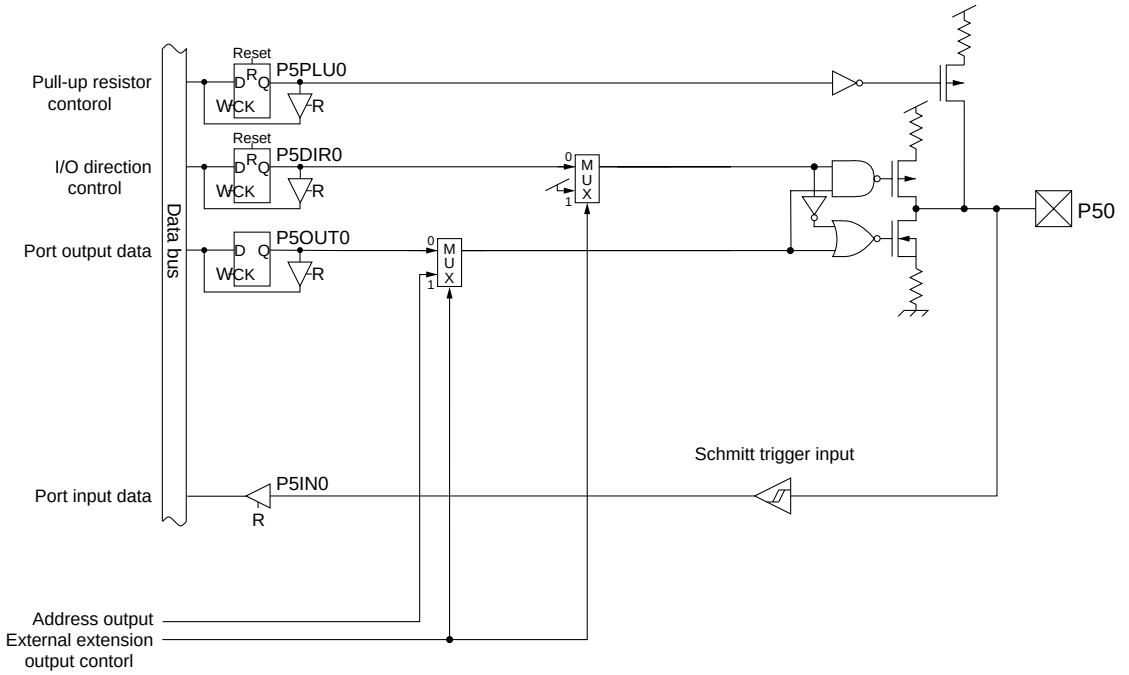


Figure:4.7.1 P50 Block Diagram

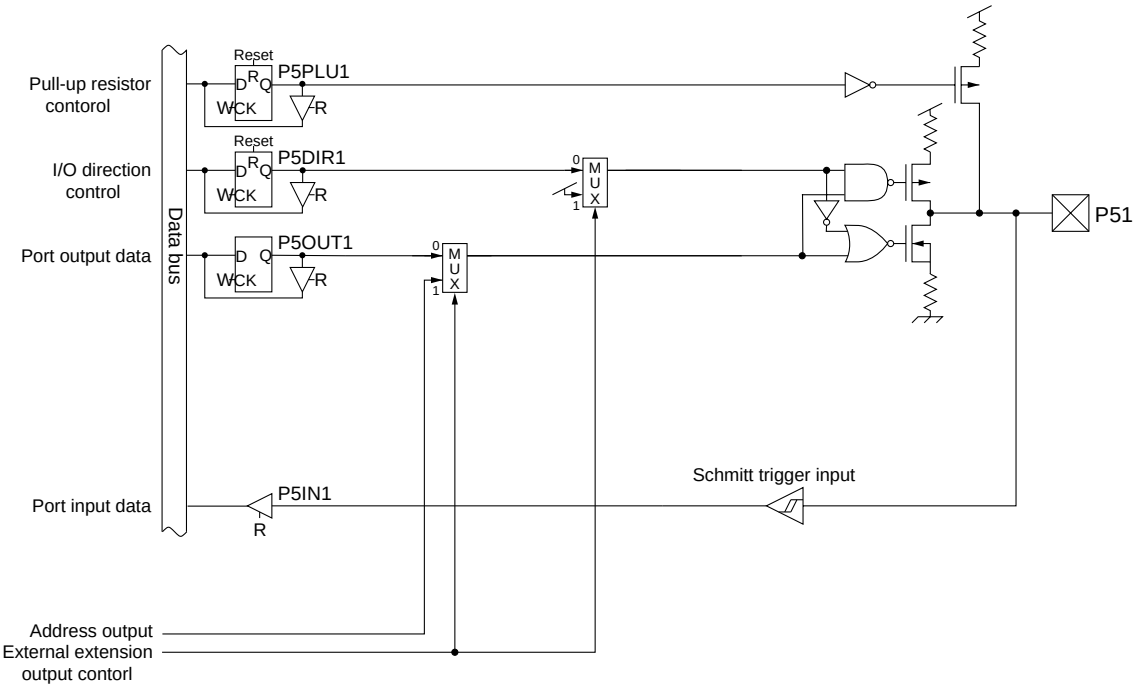


Figure:4.7.2 P51 Block Diagram

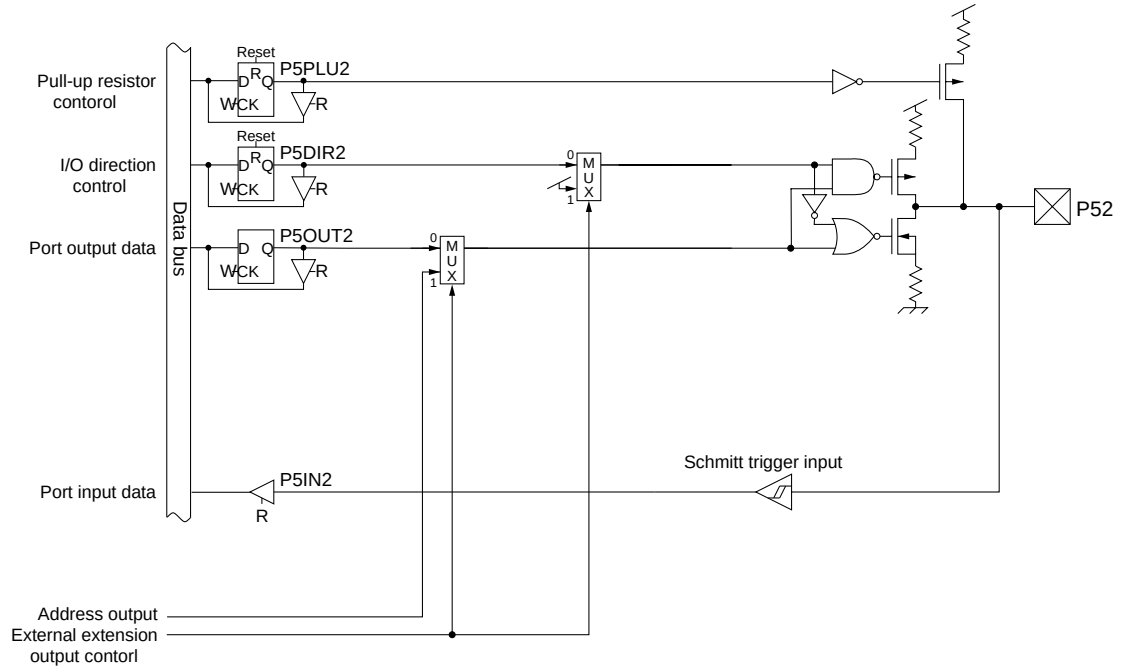


Figure:4.7.3 P52 Block Diagram

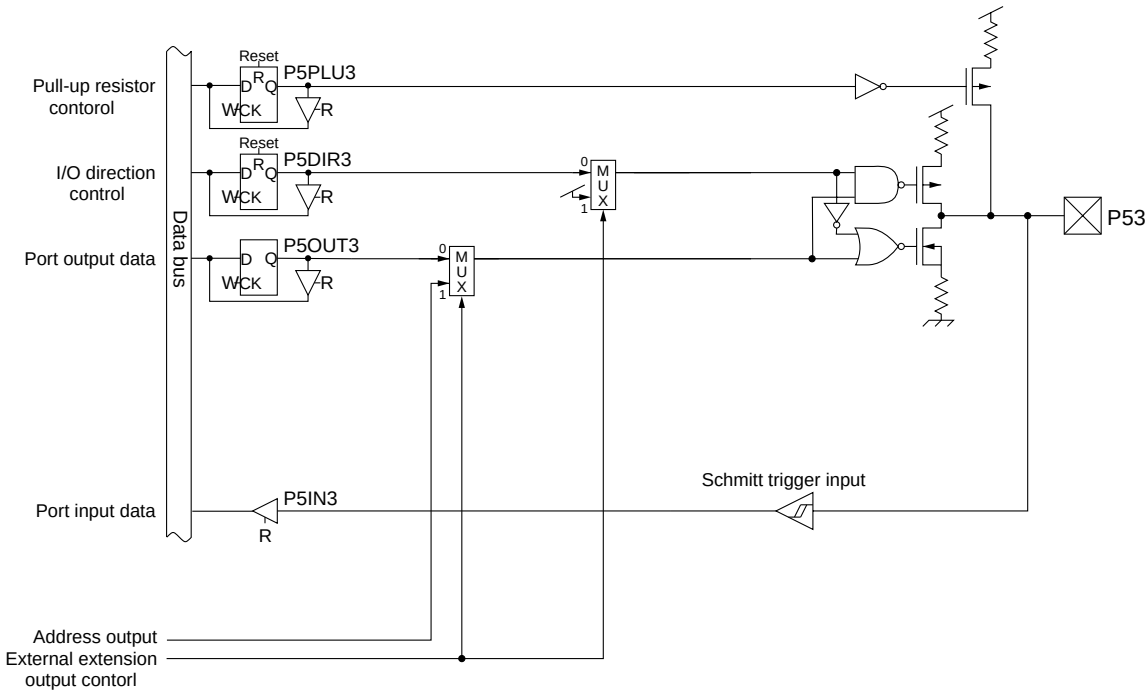


Figure:4.7.4 P53 Block Diagram

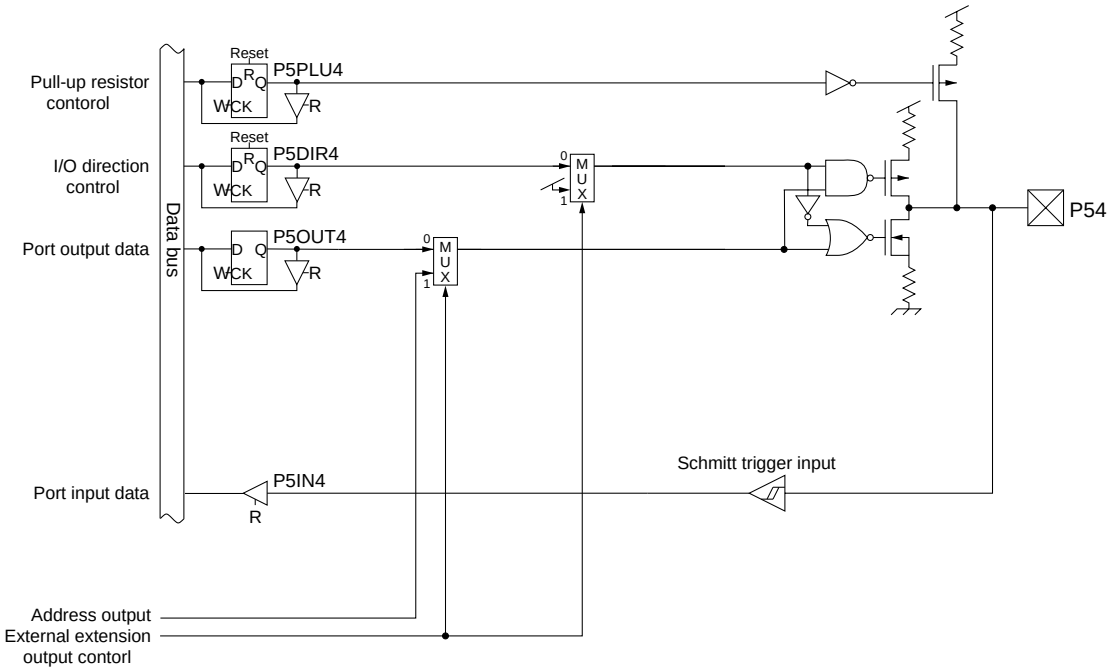


Figure:4.7.5 P54 Block Diagram

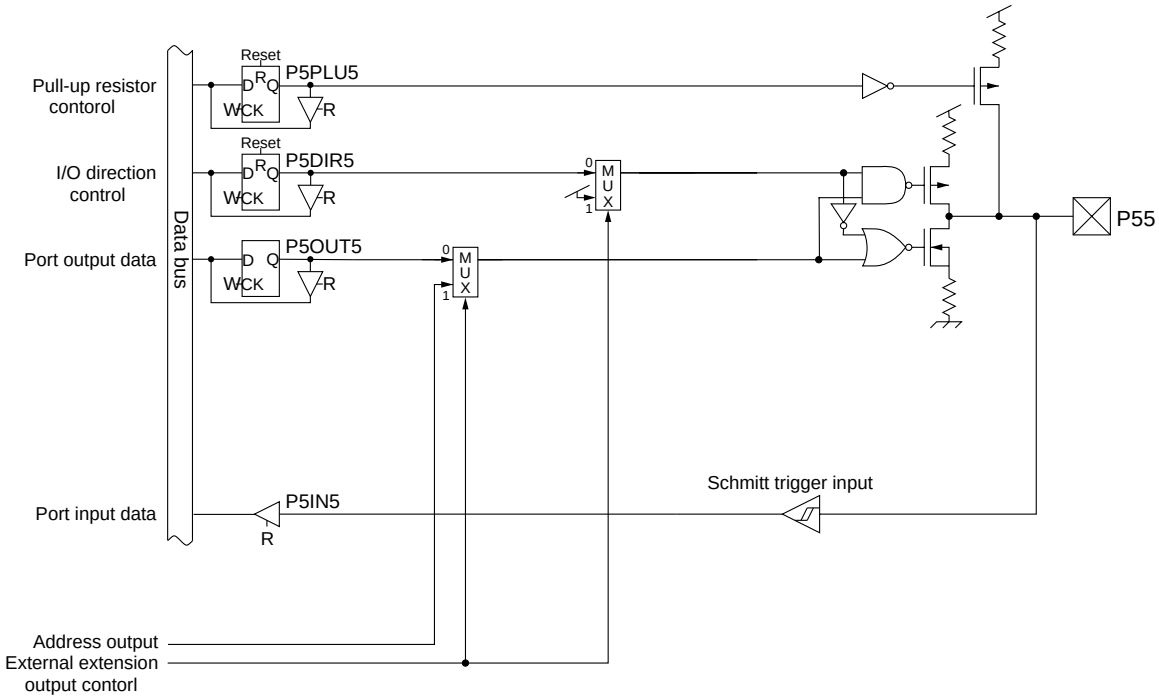


Figure:4.7.6 P55 Block Diagram

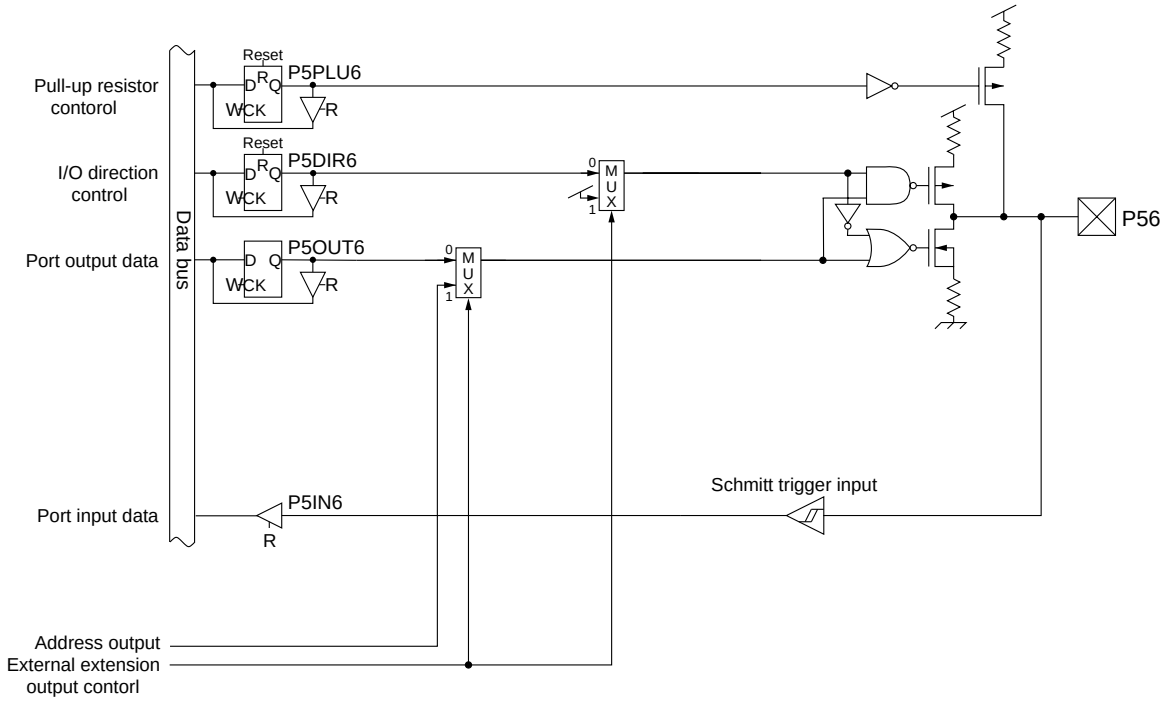


Figure:4.7.7 P56 Block Diagram

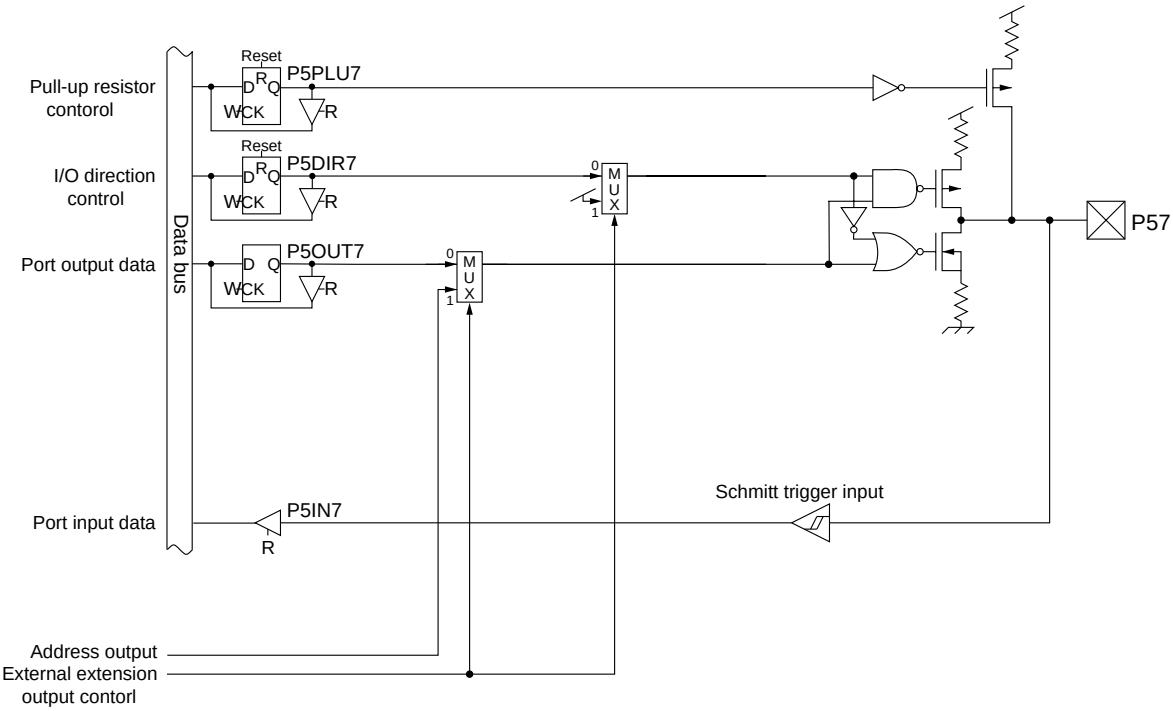


Figure:4.7.8 P57 Block Diagram

4.8 Port 6

4.8.1 Description

■ General Port Setup

To output the data to pins, set the control flag of the port 6 direction control register (P6DIR) to "1" to write the value of the port 6 output register (P6OUT).

To read input data of pins, set the control flag of the port 6 direction control register (P6DIR) to "0" to read the value of the port 6 input register (P6IN).

Each bit can be set individually as either an input or output by the port 6 I/O direction control register (P6DIR). The control flag of the port 6 direction control register (P6DIR) is set to "1" for output mode, and "0" for input mode.

Each bit can be set individually if pull-up resistor is added or not, by the port 6 pull-up resistor control register (P6PLU). Set the control flag of the port 6 pull-up resistor control register (P6PLU) to "1" to add pull-up resistor.

Port 6 can be selected to address output pin to the external extension memory or the general port pin at the memory extension mode by the address output control register (EXADV).

■ Special Function Pin Setup

P60 is used as input pin of KEY interrupt, as well.

P61 is used as input pin of KEY interrupt, as well.

P62 is used as input pin of KEY interrupt, as well.

P63 is used as input pin of KEY interrupt, as well.

P64 is used as input pin of KEY interrupt, as well.

P65 is used as input pin of KEY interrupt, as well.

P66 is used as input pin of KEY interrupt, as well.

P67 is used as input pin of KEY interrupt, as well.

P60 is address output pin to the external extension memory at the processor mode or the memory extension mode. However, bp5 of the address output control register (EXADV) should be set to use as the address output pin or the general port pin at the memory extension mode. When bp5 of the address output control register (EXADV) is "1" at the memory extension mode, or at the processor mode, it is output mode automatically.

P61 is address output pin to the external extension memory at the processor mode or the memory extension mode. However, bp5 of the address output control register (EXADV) should be set to use as the address output pin or the general port pin at the memory extension mode. When bp5 of the address output control register (EXADV) is "1" at the memory extension mode, or at the processor mode, it is output mode automatically.

P62 is address output pin to the external extension memory at the processor mode or the memory extension mode. However, bp5 of the address output control register (EXADV) should be set to use as the address output pin or the general port pin at the memory extension mode. When bp5 of the address output control register (EXADV) is "1" at the memory extension mode, or at the processor mode, it is output mode automatically.

P63 is address output pin to the external extension memory at the processor mode or the memory extension mode. However, bp5 of the address output control register (EXADV) should be set to use as the address output pin or the

general port pin at the memory extension mode. When bp5 of the address output control register (EXADV) is "1" at the memory extension mode, or at the processor mode, it is output mode automatically.

P64 is address output pin to the external extension memory at the processor mode or the memory extension mode. However, bp6 of the address output control register (EXADV) should be set to use as the address output pin or the general port pin at the memory extension mode. When bp6 of the address output control register (EXADV) is "1" at the memory extension mode, or at the processor mode, it is output mode automatically.

P65 is address output pin to the external extension memory at the processor mode or the memory extension mode. However, bp6 of the address output control register (EXADV) should be set to use as the address output pin or the general port pin at the memory extension mode. When bp6 of the address output control register (EXADV) is "1" at the memory extension mode, or at the processor mode, it is output mode automatically.

P66 is address output pin to the external extension memory at the processor mode or the memory extension mode. However, bp6 of the address output control register (EXADV) should be set to use as the address output pin or the general port pin at the memory extension mode. When bp6 of the address output control register (EXADV) is "1" at the memory extension mode, or at the processor mode, it is output mode automatically.

P67 is address output pin to the external extension memory at the processor mode or the memory extension mode. However, bp6 of the address output control register (EXADV) should be set to use as the address output pin or the general port pin at the memory extension mode. When bp6 of the address output control register (EXADV) is "1" at the memory extension mode, or at the processor mode, it is output mode automatically.

4.8.2 Registers

The following Table shows registers that control the Port 6

Table:4.8.1 Port 6control register

Registers	Address	R/W	Function	Page
P6OUT	0x03F16	R/W	Port 6 Output Register	IV-58
P6IN	0x03F26	R	Port 6 Input Register	IV-59
P6DIR	0x03F36	R/W	Port 6 Direction Control Register	IV-59
P6PLU	0x03F46	R/W	Port 6 Pull-up Resistor Control Register	IV-60
EXADV	0x03F0E	R/W	Address Output Control Register	IV-60

R/W:Readable/Writable

■ Port 6 Output Register(P6OUT:0x03F16)

bp	7	6	5	4	3	2	1	0
Flag	P6OUT7	P6OUT6	P6OUT5	P6OUT4	P6OUT3	P6OUT2	P6OUT1	P6OUT0
At reset	x	x	x	x	x	x	x	x
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bp	Flag	Description
7 6 5 4 3 2 1 0	P6OUT7 P6OUT6 P6OUT5 P6OUT4 P6OUT3 P6OUT2 P6OUT1 P6OUT0	Output data 0:Output L(VSS level) 1:Output H(VDD level)

■ Port 6 Input Register(P6IN:0x03F26)

bp	7	6	5	4	3	2	1	0
Flag	P6IN7	P6IN6	P6IN5	P6IN4	P6IN3	P6IN2	P6IN1	P6IN0
At reset	x	x	x	x	x	x	x	x
Access	R	R	R	R	R	R	R	R

bp	Flag	Description
7 6 5 4 3 2 1 0	P6IN7 P6IN6 P6IN5 P6IN4 P6IN3 P6IN2 P6IN1 P6IN0	Input data 0:Pin is L(VSS level) 1:Pin is H(VDD level)

■ Port 6 Direction Control Register(P6DIR:0x03F36)

bp	7	6	5	4	3	2	1	0
Flag	P6DIR7	P6DIR6	P6DIR5	P6DIR4	P6DIR3	P6DIR2	P6DIR1	P6DIR0
At reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bp	Flag	Description
7 6 5 4 3 2 1 0	P6DIR7 P6DIR6 P6DIR5 P6DIR4 P6DIR3 P6DIR2 P6DIR1 P6DIR0	I/O mode selection 0:Input mode 1:Output mode

■ Port 6 Pull-up Resistor Control Register(P6PLU:0x03F46)

bp	7	6	5	4	3	2	1	0
Flag	P6PLU7	P6PLU6	P6PLU5	P6PLU4	P6PLU3	P6PLU2	P6PLU1	P6PLU0
At reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bp	Flag	Description
7 6 5 4 3 2 1 0	P6PLU7 P6PLU6 P6PLU5 P6PLU4 P6PLU3 P6PLU2 P6PLU1 P6PLU0	Pull-up resistor selection 0:Not added 1:Added

■ Address Output Control Register(EXADV:0x03F0E)

bp	7	6	5	4	3	2	1	0
Flag	EXADV3	EXADV2	EXADV1	-	-	-	-	-
At reset	0	0	0	-	-	-	-	-
Access	R/W	R/W	R/W	-	-	-	-	-

bp	Flag	Description
7	EXADV3	P70,P71,P72,P73,Address output control 0:I/O port 1:address output
6	EXADV2	P64,P65,P66,P67,Address output control 0:I/O port 1:address output
5	EXADV1	P60,P61,P62,P63,Address output control 0:I/O port 1:address output
4-0	-	-

4.8.3 Block Diagram

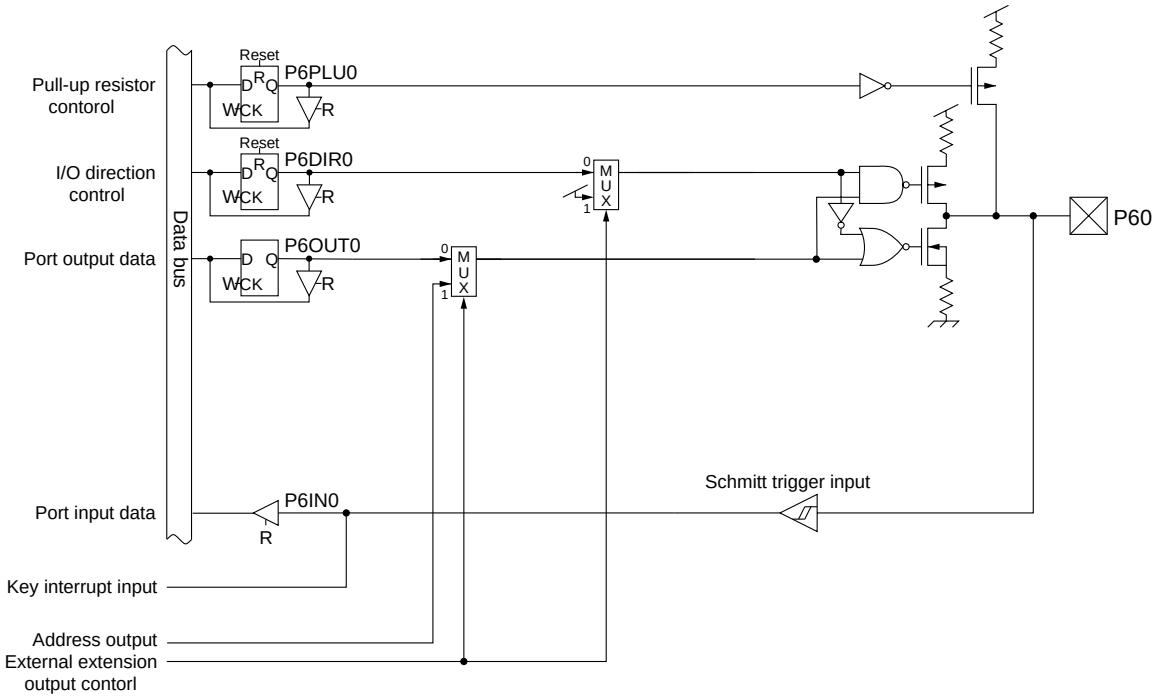


Figure:4.8.1 P60 Block Diagram

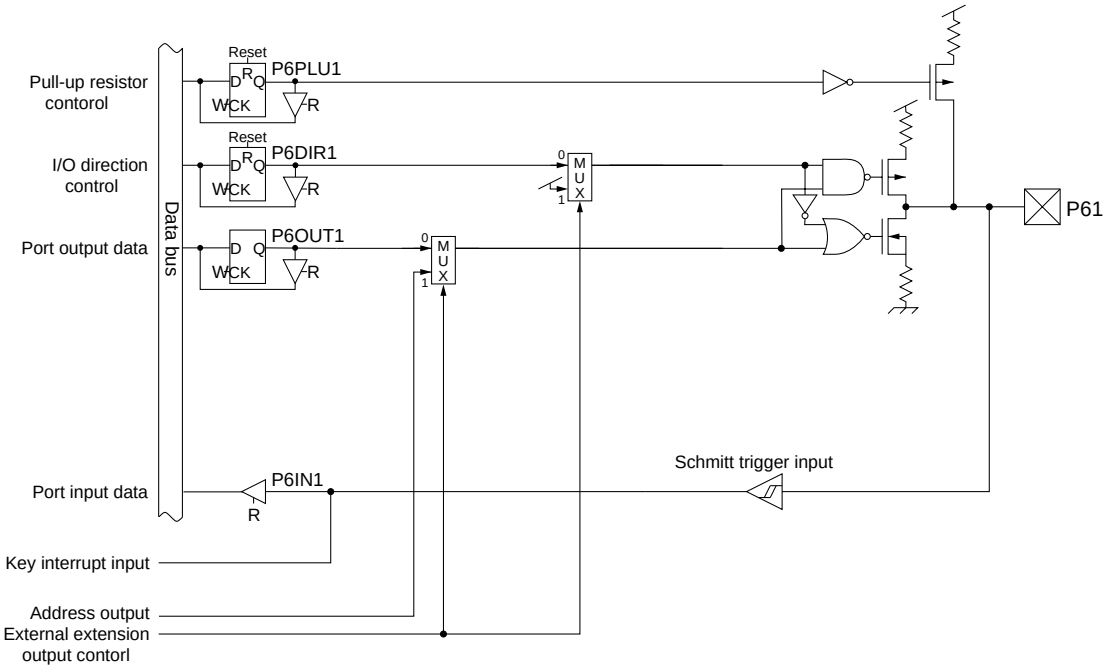


Figure:4.8.2 P61 Block Diagram

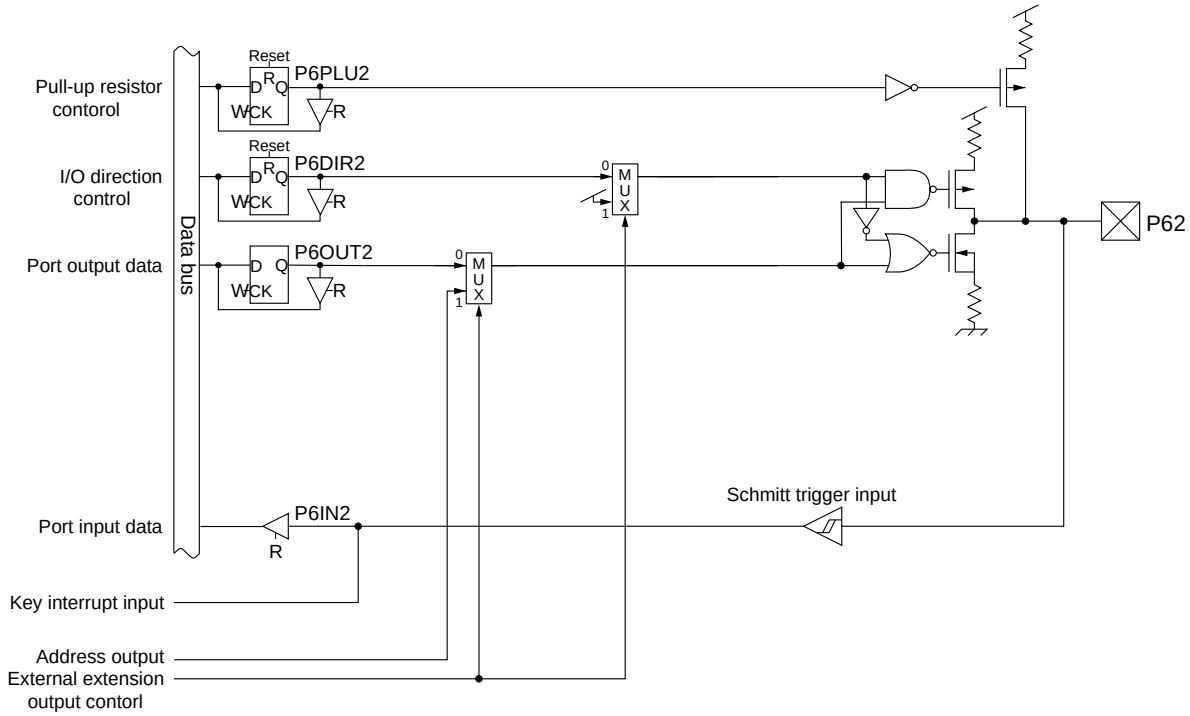


Figure:4.8.3 P62 Block Diagram

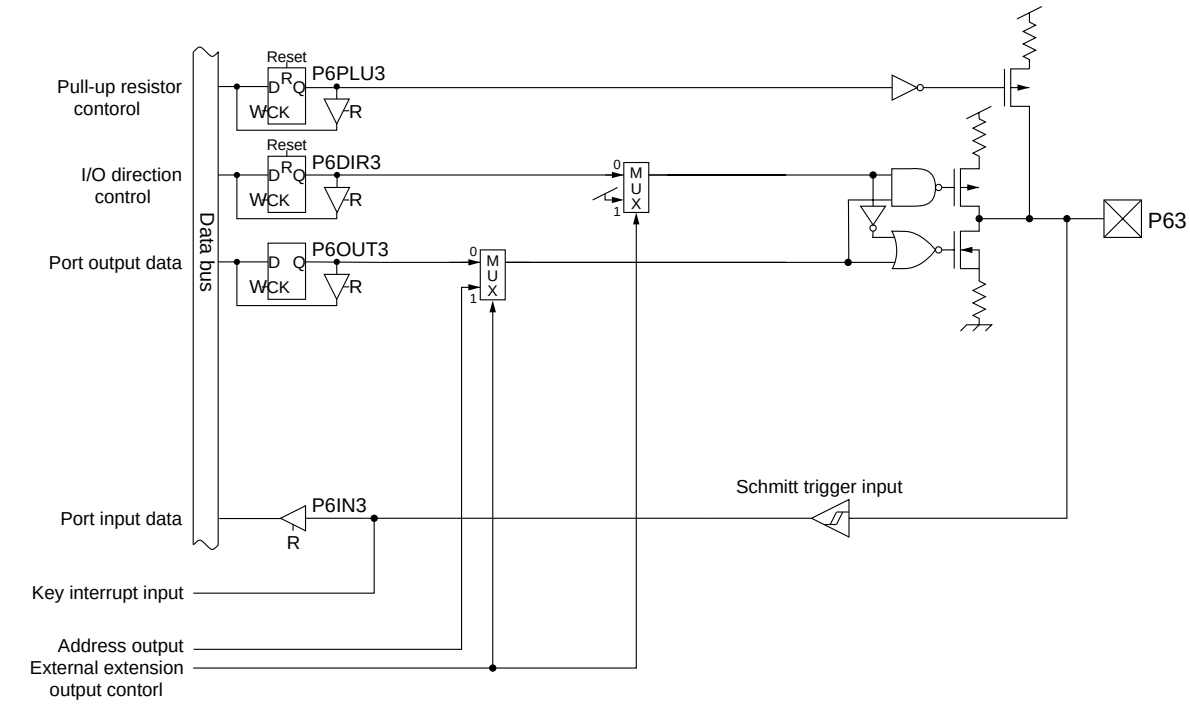


Figure:4.8.4 P63 Block Diagram

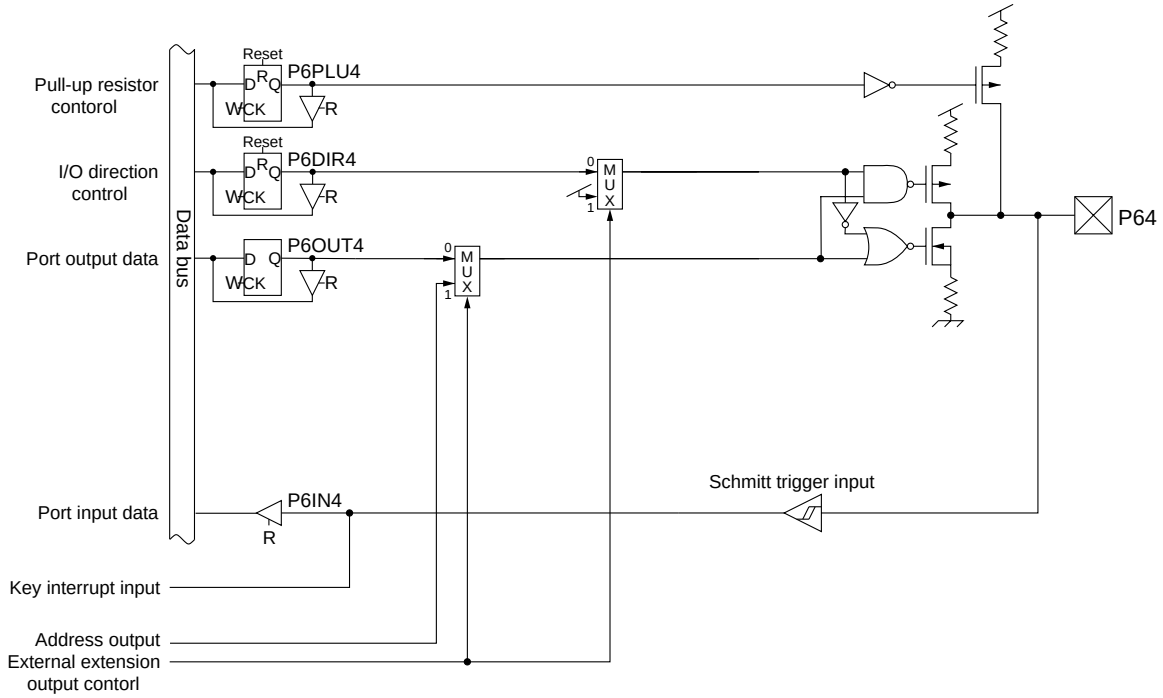


Figure:4.8.5 P64 Block Diagram

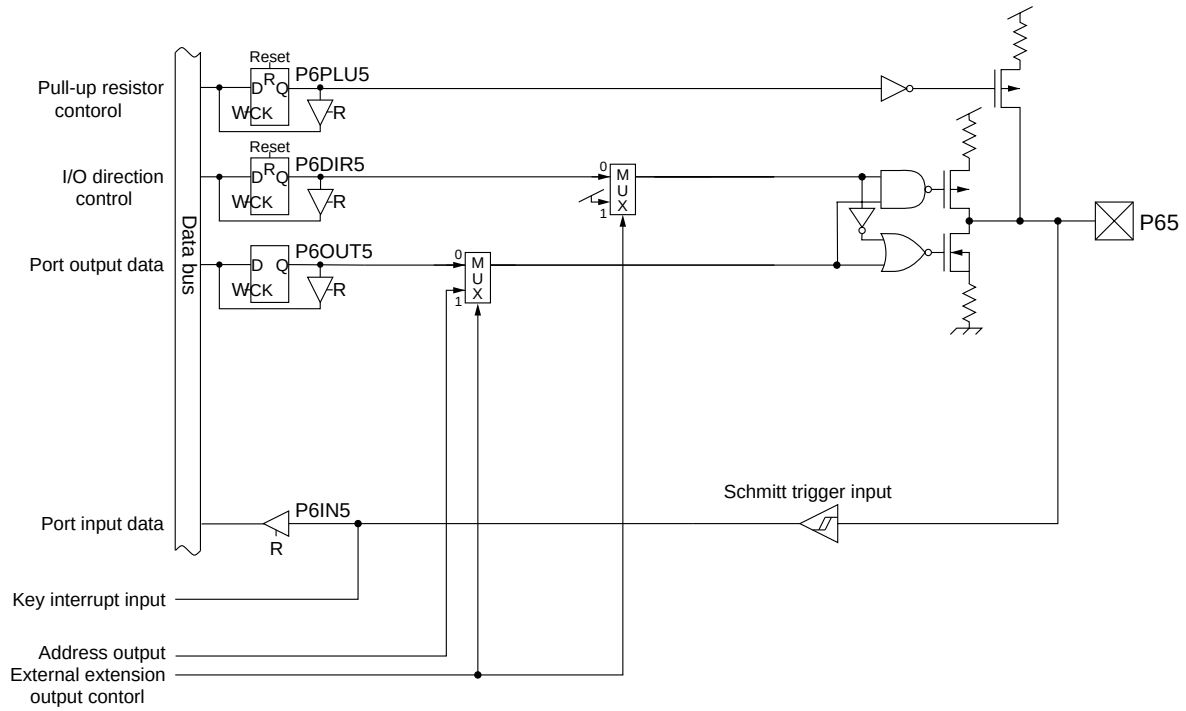


Figure:4.8.6 P65 Block Diagram

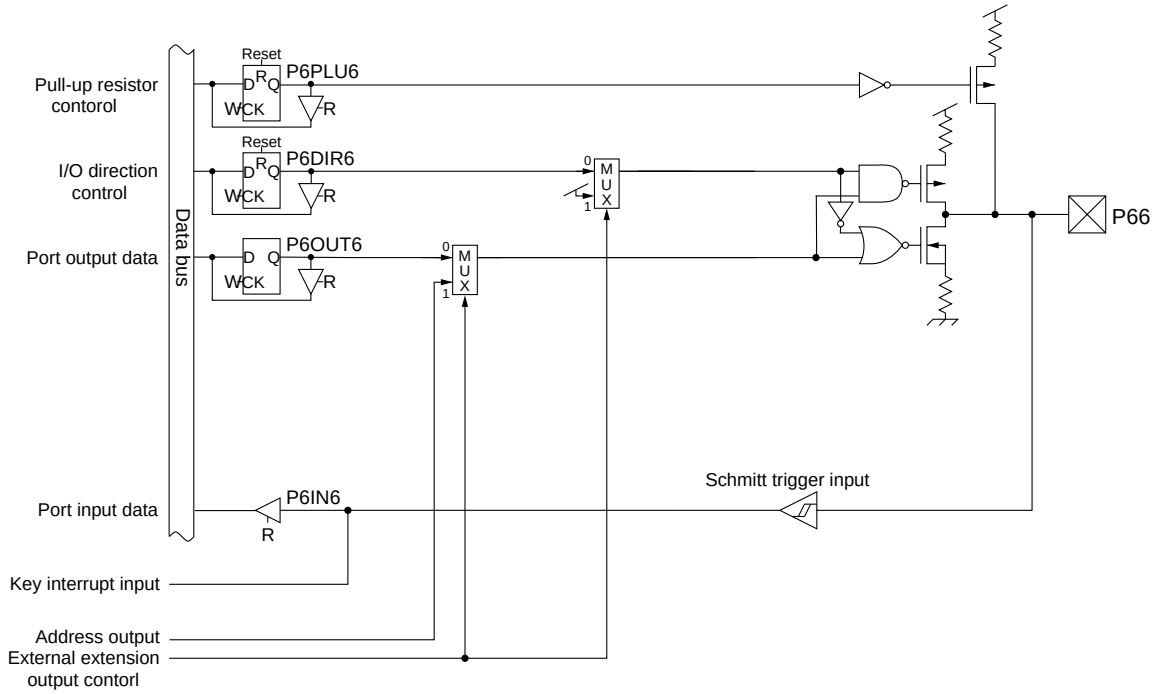


Figure:4.8.7 P66 Block Diagram

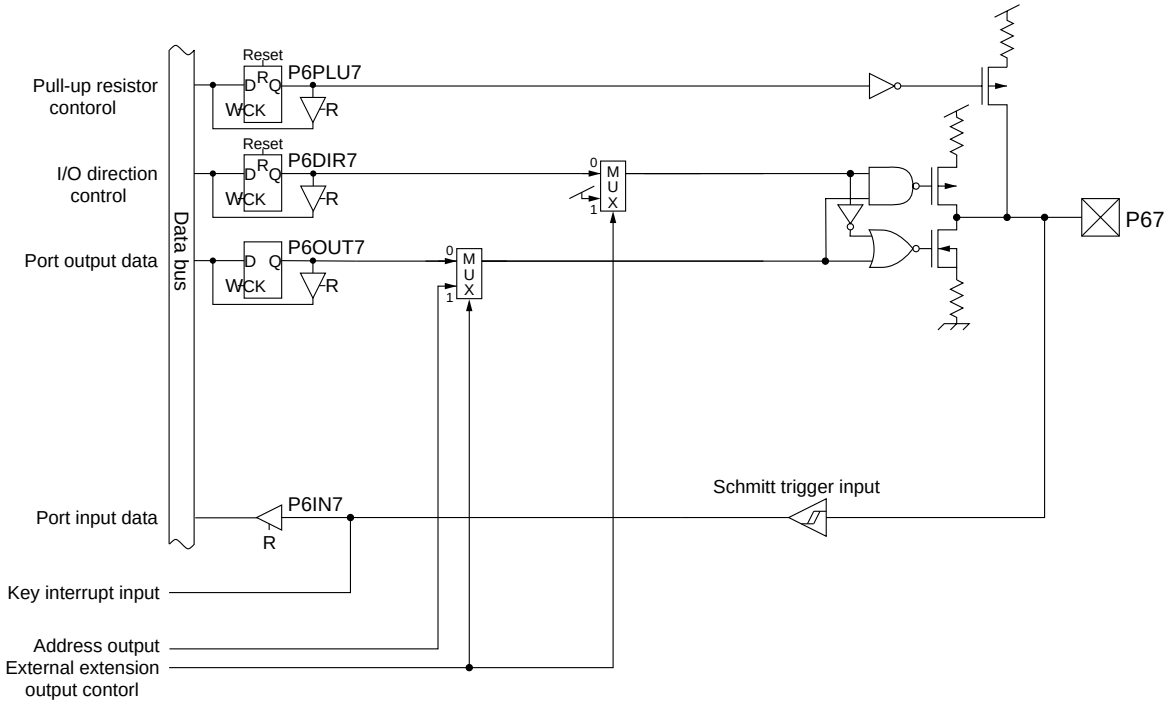


Figure:4.8.8 P67 Block Diagram

4.9 Port 7

4.9.1 Description

■ General Port Setup

To output the data to pins, set the control flag of the port 7 direction control register (P7DIR) to "1" to write the value of the port 7 output register (P7OUT).

To read input data of pins, set the control flag of the port 7 direction control register (P7DIR) to "0" to read the value of the port 7 input register (P7IN).

Each bit can be set individually as either an input or output by the port 7 I/O direction control register (P7DIR). The control flag of the port 7 direction control register (P7DIR) is set to "1" for output mode, and "0" for input mode.

Each bit can be set individually if pull-up or pull-down resistor is added or not, by the port 7 pull-up/pull-down resistor control register (P7PLU). Set the control flag of the port 7 pull-up/pull-down resistor control register (P7PLU) to "1" to add pull-up/pull-down resistor.

Port 7 can be selected to add pull-up resistor or pull-down resistor by bp1 of the pull-up/pull-down resistor selection register (SELUD).

Each bit can be selected individually as synchronous mode by the port 7 synchronous output control regiser (P7SYO). The port 7 synchronous output control register (P7SYO) is set to "1" for synchronous output, and "0" for the general port.

Port 7 can be selected to address output pin to the external extension memory or the general port pin at the memory extension mode by the address output control register (EXADV).

■ Special Function Pin Setup

P70 can be selected as synchronous output by each bit by the port 7 synchronous output control register (P7SYO). The port 7 synchronous output control register (P7SYO) is set to "1" for synchronous output, and "0" for general port. The port 7 synchronous output event selection register (P7SEV) can select the event that generates synchronous output. When bp1, bp0 of the port 7 synchronous output event selection register (P7SEV) is "00", IRQ2(P22/IRQ2A input) is selected and "01" for the TM7IRQ, "10" for the TM2IRQ, "11" for the TM7IRQ.

P71 can be selected as synchronous output by each bit by the port 7 synchronous output control register (P7SYO). The port 7 synchronous output control register (P7SYO) is set to "1" for synchronous output, and "0" for general port. The port 7 synchronous output event selection register (P7SEV) can select the event that generates synchronous output. When bp1, bp0 of the port 7 synchronous output event selection register (P7SEV) is "00", IRQ2(P22/IRQ2A input) is selected and "01" for the TM7IRQ, "10" for the TM2IRQ, "11" for the TM7IRQ.

P72 can be selected as synchronous output by each bit by the port 7 synchronous output control register (P7SYO). The port 7 synchronous output control register (P7SYO) is set to "1" for synchronous output, and "0" for general port. The port 7 synchronous output event selection register (P7SEV) can select the event that generates synchronous output. When bp1, bp0 of the port 7 synchronous output event selection register (P7SEV) is "00", IRQ2(P22/IRQ2A input) is selected and "01" for the TM7IRQ, "10" for the TM2IRQ, "11" for the TM7IRQ.

P73 can be selected as synchronous output by each bit by the port 7 synchronous output control register (P7SYO). The port 7 synchronous output control register (P7SYO) is set to "1" for synchronous output, and "0" for general port. The port 7 synchronous output event selection register (P7SEV) can select the event that generates synchronous output. When bp1, bp0 of the port 7 synchronous output event selection register (P7SEV) is "00", IRQ2(P22/IRQ2A input) is selected and "01" for the TM7IRQ, "10" for the TM2IRQ, "11" for the TM7IRQ.

P74 can be selected as synchronous output by each bit by the port 7 synchronous output control register (P7SYO). The port 7 synchronous output control register (P7SYO) is set to "1" for synchronous output, and "0" for general port. The port 7 synchronous output event selection register (P7SEV) can select the event that generates synchronous output. When bp1, bp0 of the port 7 synchronous output event selection register (P7SEV) is "00", IRQ2(P22/IRQ2A input) is selected and "01" for the TM7IRQ, "10" for the TM2IRQ, "11" for the TM7IRQ.

P75 can be selected as synchronous output by each bit by the port 7 synchronous output control register (P7SYO). The port 7 synchronous output control register (P7SYO) is set to "1" for synchronous output, and "0" for general port. The port 7 synchronous output event selection register (P7SEV) can select the event that generates synchronous output. When bp1, bp0 of the port 7 synchronous output event selection register (P7SEV) is "00", IRQ2(P22/IRQ2A input) is selected and "01" for the TM7IRQ, "10" for the TM2IRQ, "11" for the TM7IRQ.

P76 can be selected as synchronous output by each bit by the port 7 synchronous output control register (P7SYO). The port 7 synchronous output control register (P7SYO) is set to "1" for synchronous output, and "0" for general port. The port 7 synchronous output event selection register (P7SEV) can select the event that generates synchronous output. When bp1, bp0 of the port 7 synchronous output event selection register (P7SEV) is "00", IRQ2(P22/IRQ2A input) is selected and "01" for the TM7IRQ, "10" for the TM2IRQ, "11" for the TM7IRQ.

P77 can be selected as synchronous output by each bit by the port 7 synchronous output control register (P7SYO). The port 7 synchronous output control register (P7SYO) is set to "1" for synchronous output, and "0" for general port. The port 7 synchronous output event selection register (P7SEV) can select the event that generates synchronous output. When bp1, bp0 of the port 7 synchronous output event selection register (P7SEV) is "00", IRQ2(P22/IRQ2A input) is selected and "01" for the TM7IRQ, "10" for the TM2IRQ, "11" for the TM7IRQ.

P70 is address output pin to the external extension memory at the processor mode or the memory extension mode. However, bp7 of the address output control register (EXADV) should be set to use as the address output pin or the general port pin at the memory extension mode. When bp7 of the address output control register (EXADV) is "1" at the memory extension mode, or at the processor mode, it is output mode automatically.

P71 is address output pin to the external extension memory at the processor mode or the memory extension mode. However, bp7 of the address output control register (EXADV) should be set to use as the address output pin or the general port pin at the memory extension mode. When bp7 of the address output control register (EXADV) is "1" at the memory extension mode, or at the processor mode, it is output mode automatically.

P72 is address output pin to the external extension memory at the processor mode or the memory extension mode. However, bp7 of the address output control register (EXADV) should be set to use as the address output pin or the general port pin at the memory extension mode. When bp7 of the address output control register (EXADV) is "1" at the memory extension mode, or at the processor mode, it is output mode automatically.

P73 is address output pin to the external extension memory at the processor mode or the memory extension mode. However, bp7 of the address output control register (EXADV) should be set to use as the address output pin or the general port pin at the memory extension mode. When bp7 of the address output control register (EXADV) is "1" at the memory extension mode, or at the processor mode, it is output mode automatically.

P74 is output pin of the data chip select signal at the processor mode or the memory extension mode. These modes are set to the output modes automatically.

P75 is output pin of the data read enable signal at the processor mode or the memory extension mode. These modes are set to the output modes automatically.

P76 is output pin of the data write enable signal at the processor mode or the memory extension mode. These modes are set to the output modes automatically.

P77 is input pin of the data acknowledge signal at the processor mode or the memory extension mode. These modes are set to the input modes automatically.

4.9.2 Registers

The following Table shows registers that control the Port 7

Table:4.9.1 Port 7control register

Registers	Address	R/W	Function	Page
P7OUT	0x03F17	R/W	Port 7 Output Register	IV-67
P7IN	0x03F27	R	Port 7 Input Register	IV-68
P7DIR	0x03F37	R/W	Port 7 Direction Control Register	IV-68
P7PLU	0x03F47	R/W	Port 7 Pull-up/Pull-down Resistor Control Register	IV-69
P7SYO	0x03F1F	R/W	Port 7 Synchronous Output Control Register	IV-69
P7SEV	0x03F2F	R/W	Port 7 Synchronous Output Event Selection Register	IV-70
SELUD	0x03F4B	R/W	Pull-up/Pull-down Resistor Selection Register	IV-70
EXADV	0x03F0E	R/W	Address Output Control Register	IV-71

R/W:Readable/Writable

■ Port 7 Output Register(P7OUT:0x03F17)

bp	7	6	5	4	3	2	1	0
Flag	P7OUT7	P7OUT6	P7OUT5	P7OUT4	P7OUT3	P7OUT2	P7OUT1	P7OUT0
At reset	x	x	x	x	x	x	x	x
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bp	Flag	Description
7 6 5 4 3 2 1 0	P7OUT7 P7OUT6 P7OUT5 P7OUT4 P7OUT3 P7OUT2 P7OUT1 P7OUT0	Output data 0:Output L(VSS level) 1:Output H(VDD level)

■ Port 7 Input Register(P7IN:0x03F27)

bp	7	6	5	4	3	2	1	0
Flag	P7IN7	P7IN6	P7IN5	P7IN4	P7IN3	P7IN2	P7IN1	P7IN0
At reset	x	x	x	x	x	x	x	x
Access	R	R	R	R	R	R	R	R

bp	Flag	Description
7 6 5 4 3 2 1 0	P7IN7 P7IN6 P7IN5 P7IN4 P7IN3 P7IN2 P7IN1 P7IN0	Input data 0:Pin is L(VSS level) 1:Pin is H(VDD level)

■ Port 7 Direction Control Register(P7DIR:0x03F37)

bp	7	6	5	4	3	2	1	0
Flag	P7DIR7	P7DIR6	P7DIR5	P7DIR4	P7DIR3	P7DIR2	P7DIR1	P7DIR0
At reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bp	Flag	Description
7 6 5 4 3 2 1 0	P7DIR7 P7DIR6 P7DIR5 P7DIR4 P7DIR3 P7DIR2 P7DIR1 P7DIR0	I/O mode selection 0:Input mode 1:Output mode

■ Port 7 Pull-up/Pull-down Resistor Control Register(P7PLU:0x03F47)

bp	7	6	5	4	3	2	1	0
Flag	P7PLU7	P7PLU6	P7PLU5	P7PLU4	P7PLU3	P7PLU2	P7PLU1	P7PLU0
At reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bp	Flag	Description
7 6 5 4 3 2 1 0	P7PLU7 P7PLU6 P7PLU5 P7PLU4 P7PLU3 P7PLU2 P7PLU1 P7PLU0	Pull-up/pull-down resistor selection 0:Not added 1:Added

■ Port 7 Synchronous Output Control Register(P7SYO:0x03F1F)

bp	7	6	5	4	3	2	1	0
Flag	P7SYO7	P7SYO6	P7SYO5	P7SYO4	P7SYO3	P7SYO2	P7SYO1	P7SYO0
At reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bp	Flag	Description
7 6 5 4 3 2 1 0	P7SYO7 P7SYO6 P7SYO5 P7SYO4 P7SYO3 P7SYO2 P7SYO1 P7SYO0	Synchronous output selection 0:I/O port 1:Synchronous output

■ Port 7 Synchronous Output Event Selection Register(P7SEV:0x03F2F)

bp	7	6	5	4	3	2	1	0
Flag	-	-	-	-	-	-	P7SEV1	P7SEV0
At reset	-	-	-	-	-	-	0	0
Access	-	-	-	-	-	-	R/W	R/W

bp	Flag	Description
7 2	-	-
1 0	P7SEV1 P7SEV0	Synchronous output event selection 00: IRQ2(P22/IRQ2A input) 01: TM7IRQ 10: TM2IRQ 11: TM1IRQ

■ Pull-up/Pull-down Resistor Selection Register(SELUD:0x03F4B)

bp	7	6	5	4	3	2	1	0
Flag	-	-	-	-	-	PADWN	P7DWN	P4DWN
At reset	-	-	-	-	-	0	0	0
Access	-	-	-	-	-	R/W	R/W	R/W

bp	Flag	Description
7	-	-
6	-	-
5	-	-
4	-	-
3	-	-
2	PADWN	Port A pull-up/pull-down selection 0:Pull-up 1:Pull-down
1	P7DWN	Port 7 pull-up/pull-down selection 0:Pull-up 1:Pull-down
0	P4DWN	Port 4 pull-up/pull-down selection 0:Pull-up 1:Pull-down

■ Address Output Control Register(EXADV:0x03F0E)

bp	7	6	5	4	3	2	1	0
Flag	EXADV3	EXADV2	EXADV1	-	-	-	-	-
At reset	0	0	0	-	-	-	-	-
Access	R/W	R/W	R/W	-	-	-	-	-

bp	Flag	Description
7	EXADV3	P70,P71,P72,P73,Address output control 0:I/O port 1:address output
6	EXADV2	P64,P65,P66,P67,Address output control 0:I/O port 1:address output
5	EXADV1	P60,P61,P62,P63,Address output control 0:I/O port 1:address output
4-0	-	-

4.9.3 Block Diagram

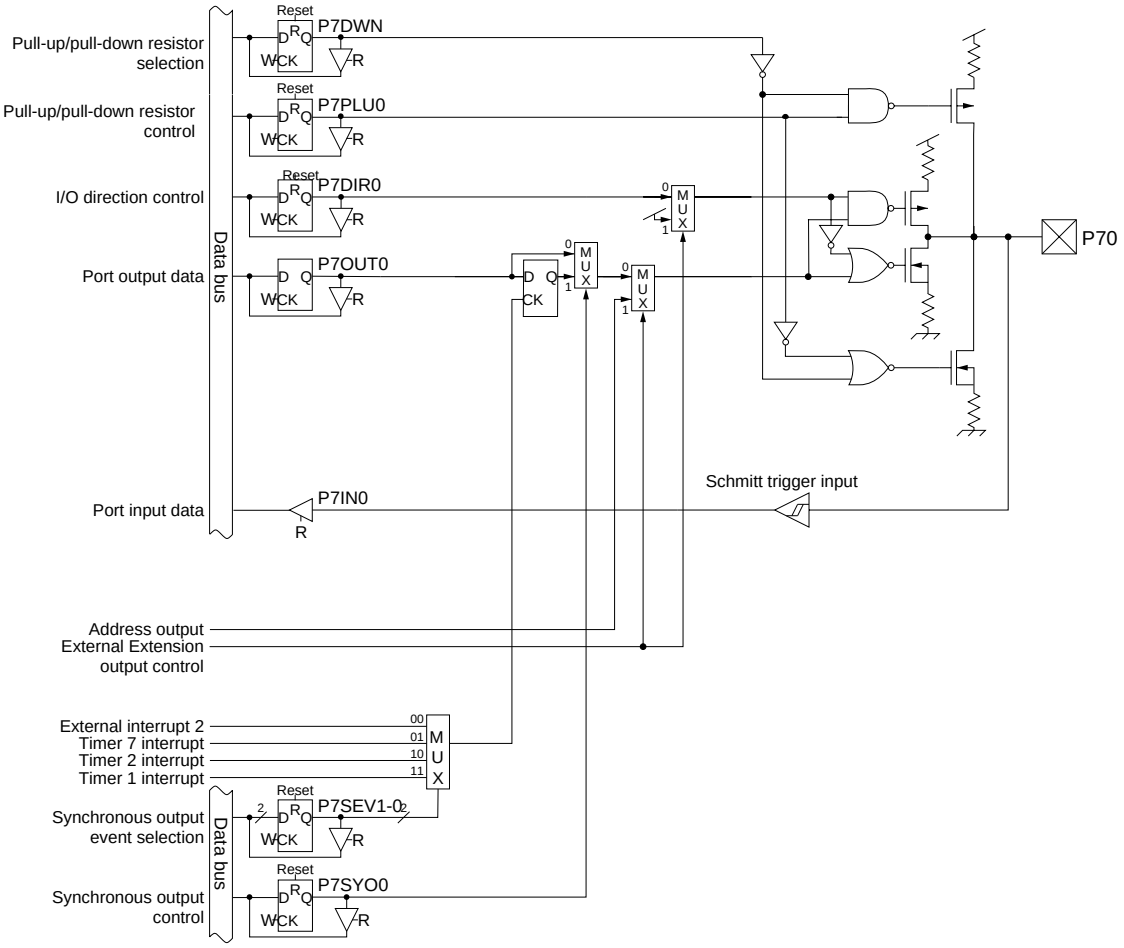


Figure:4.9.1 P70 Block Diagram

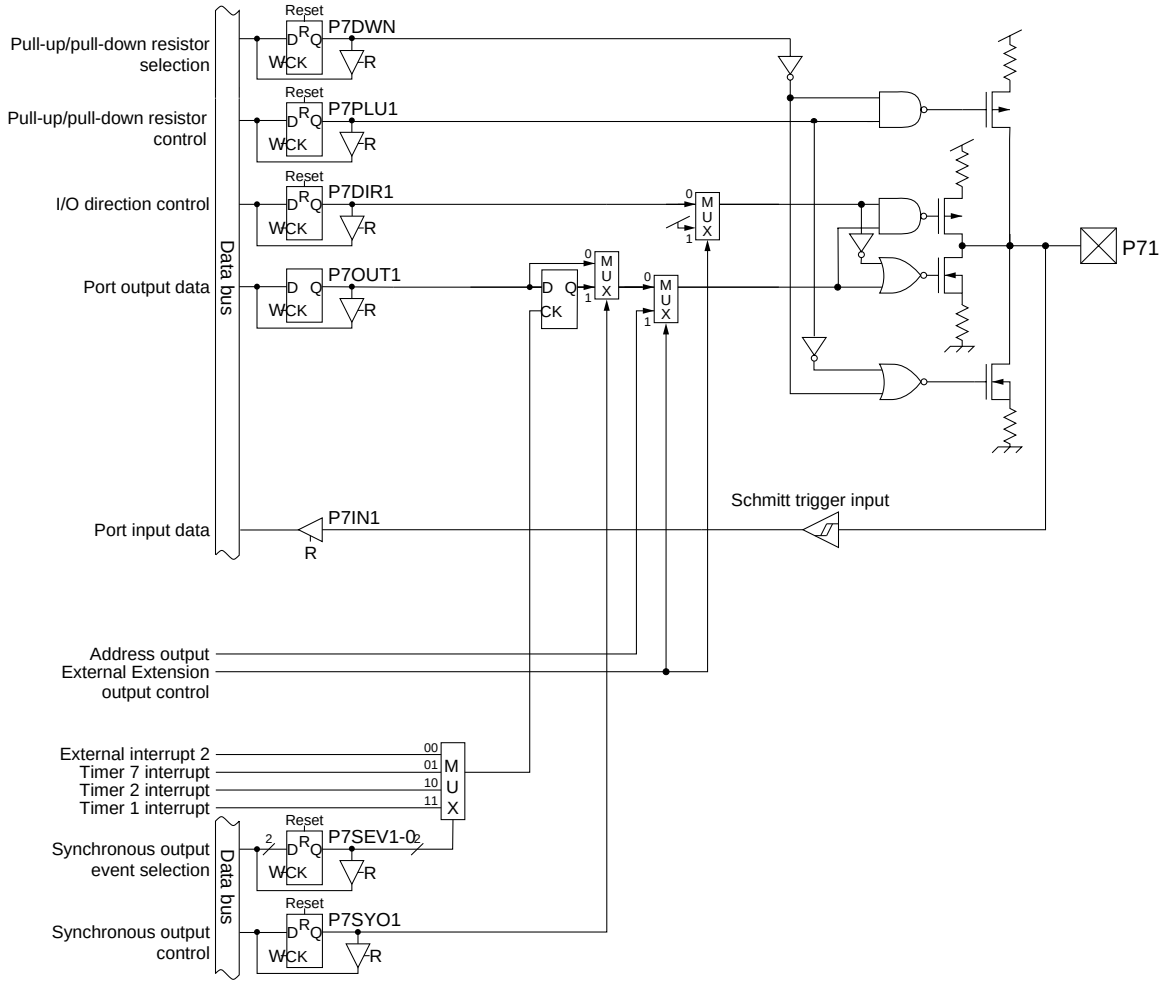


Figure:4.9.2 P71 Block Diagram

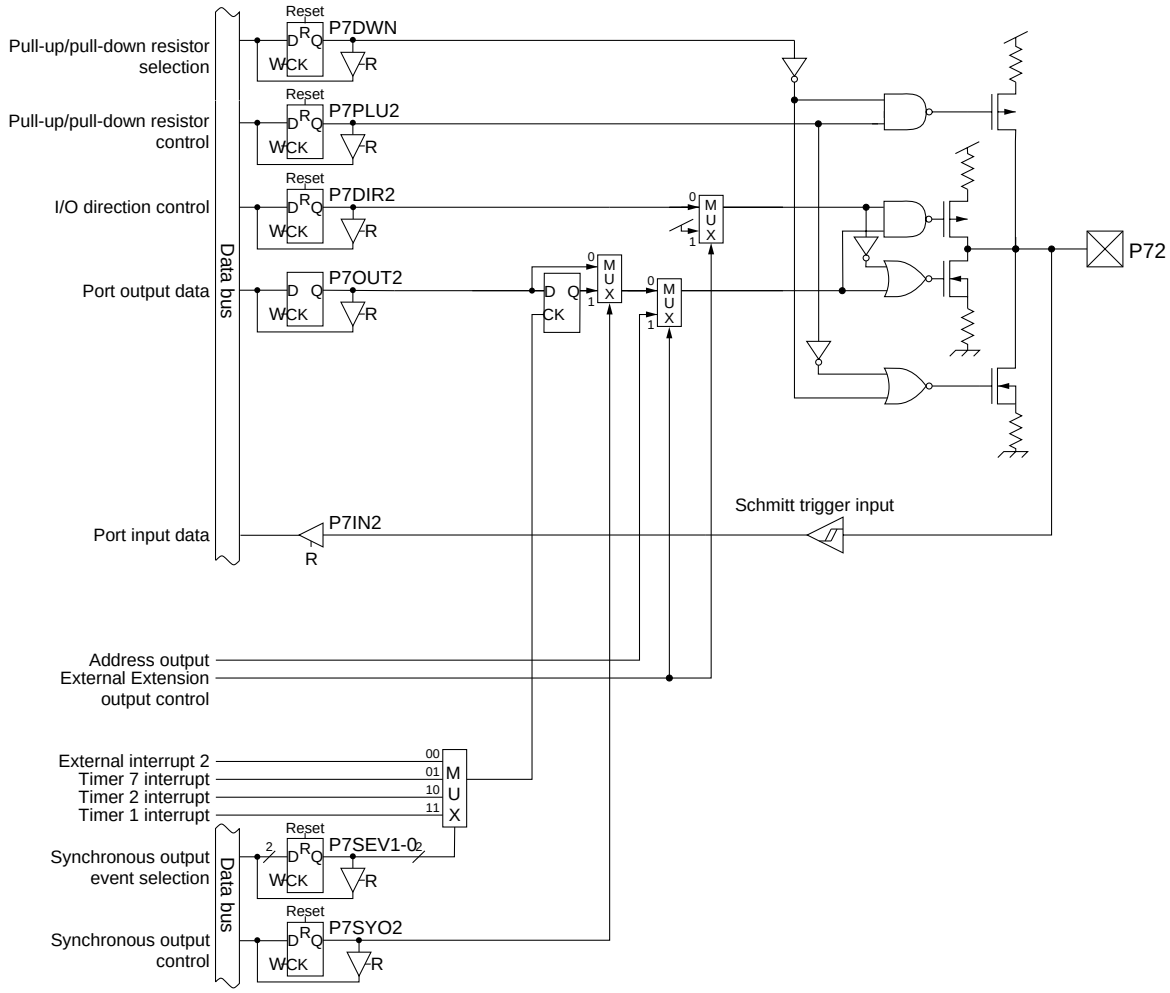


Figure:4.9.3 P72 Block Diagram

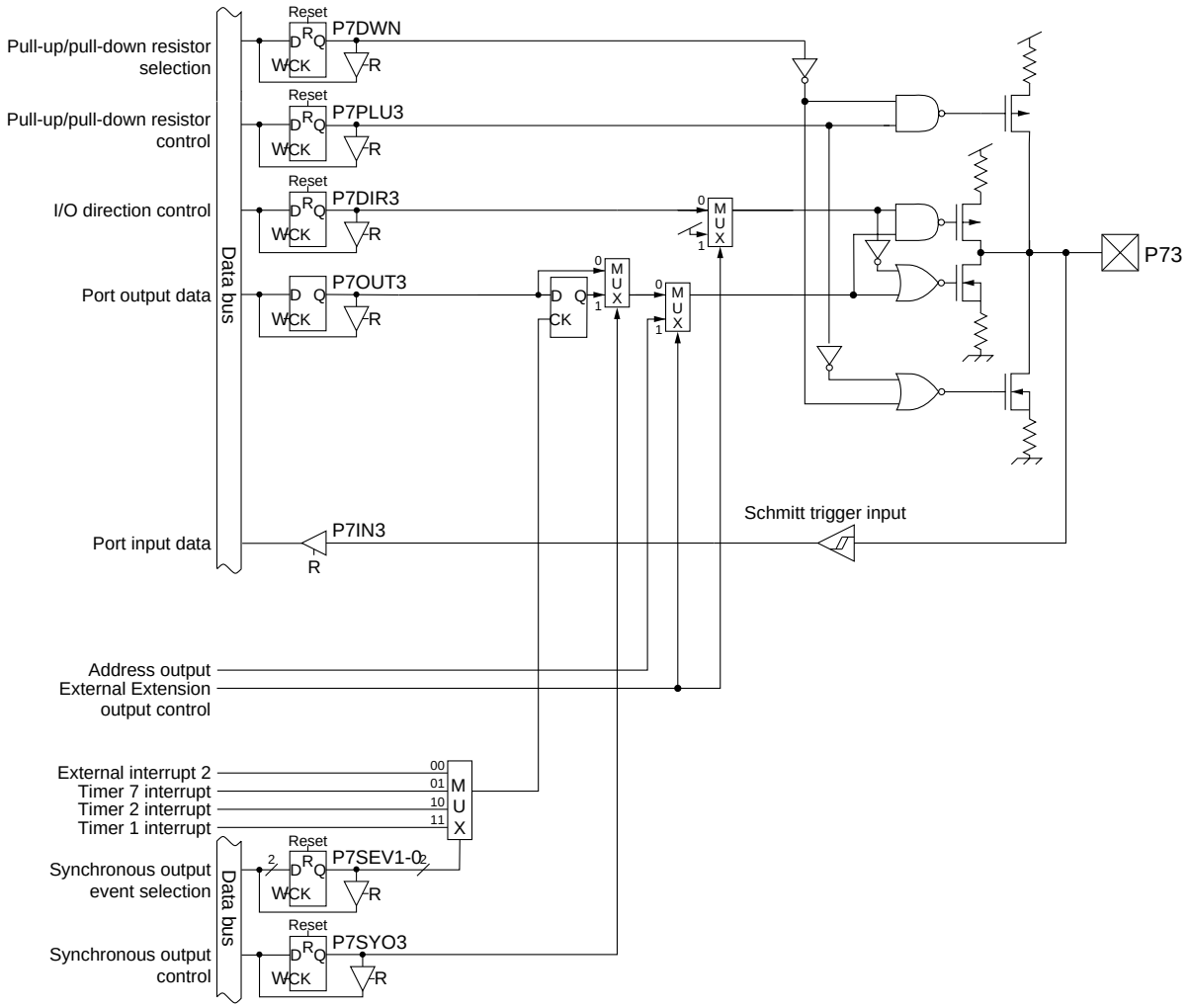


Figure:4.9.4 P73 Block Diagram

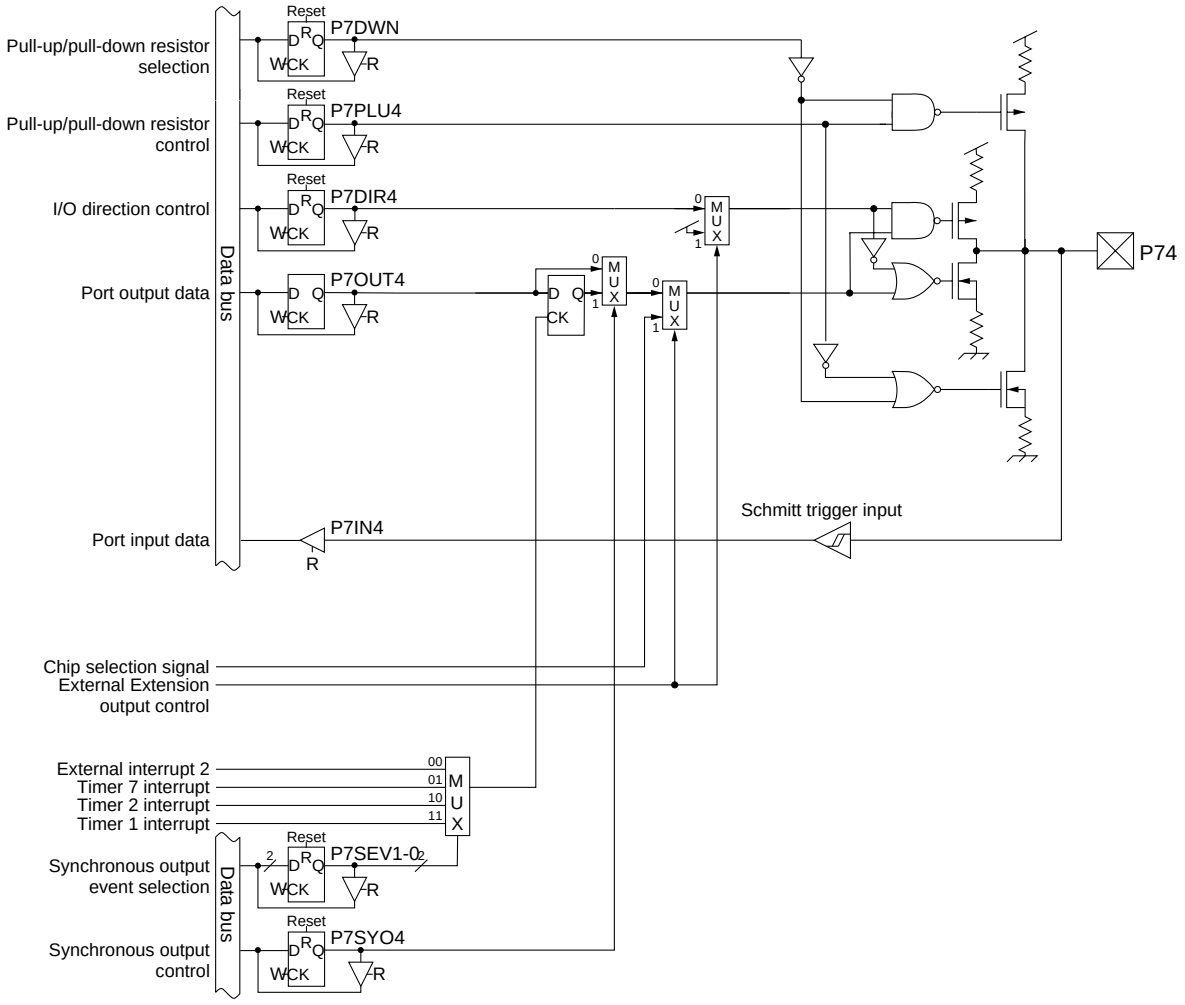


Figure:4.9.5 P74 Block Diagram

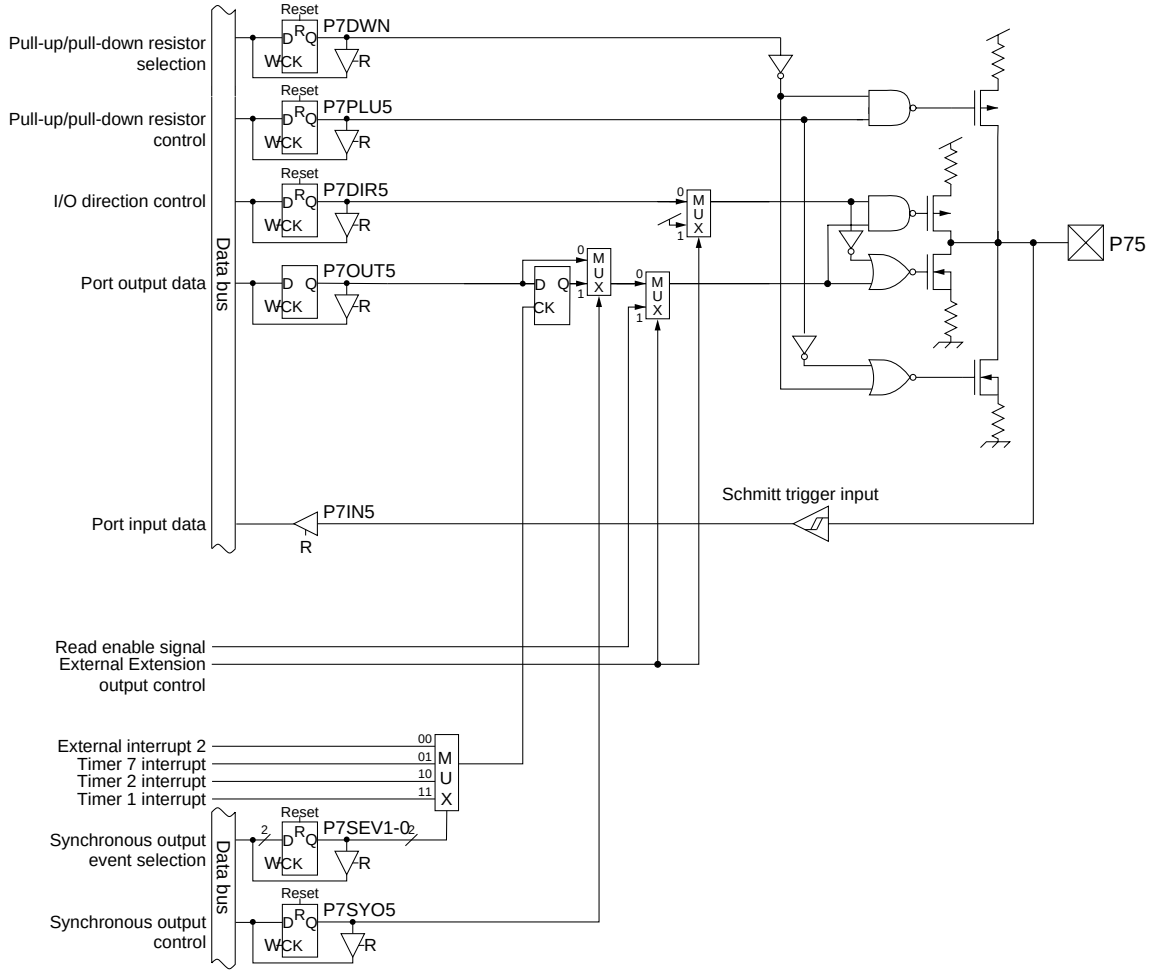


Figure:4.9.6 P75 Block Diagram

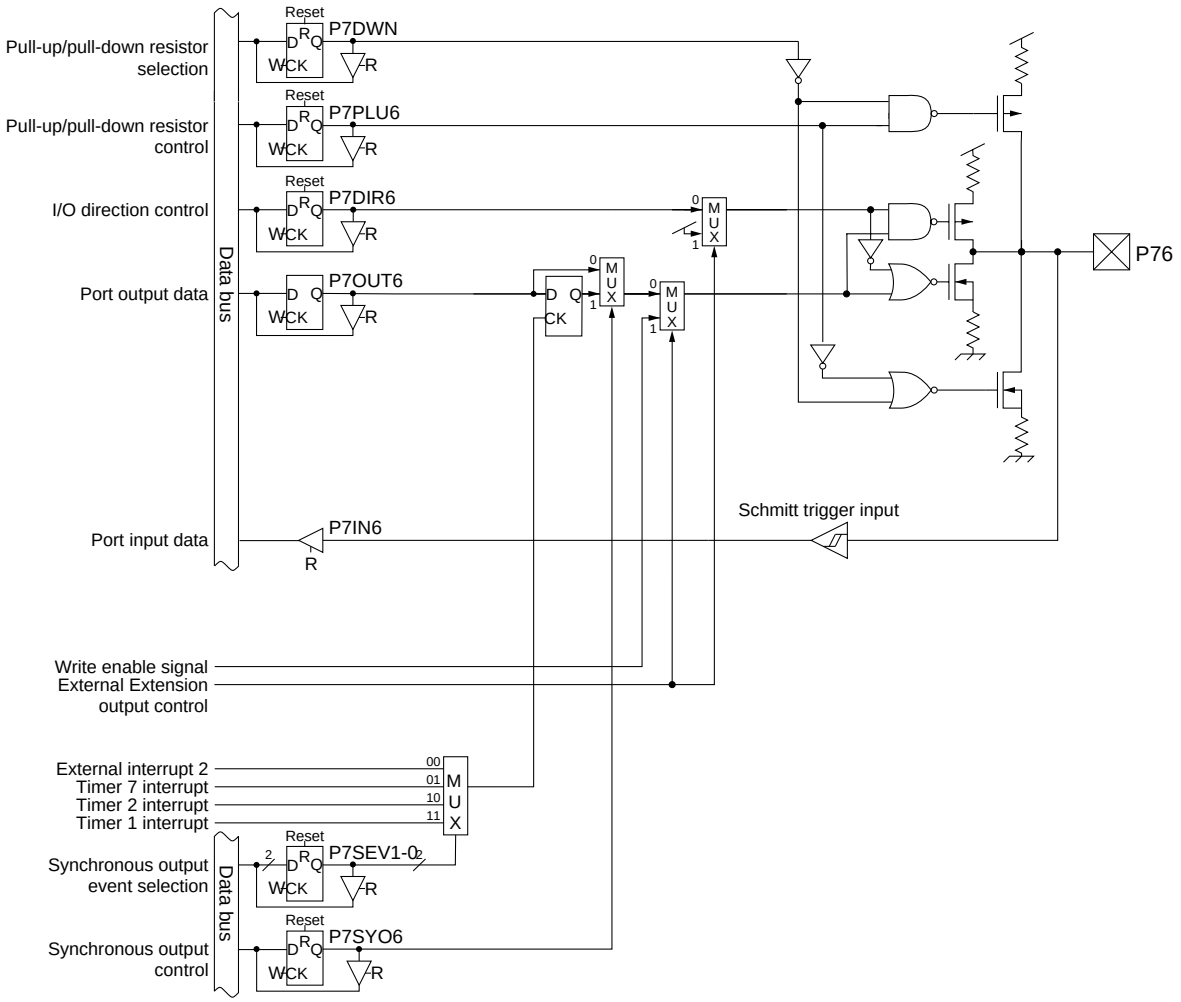


Figure:4.9.7 P76 Block Diagram

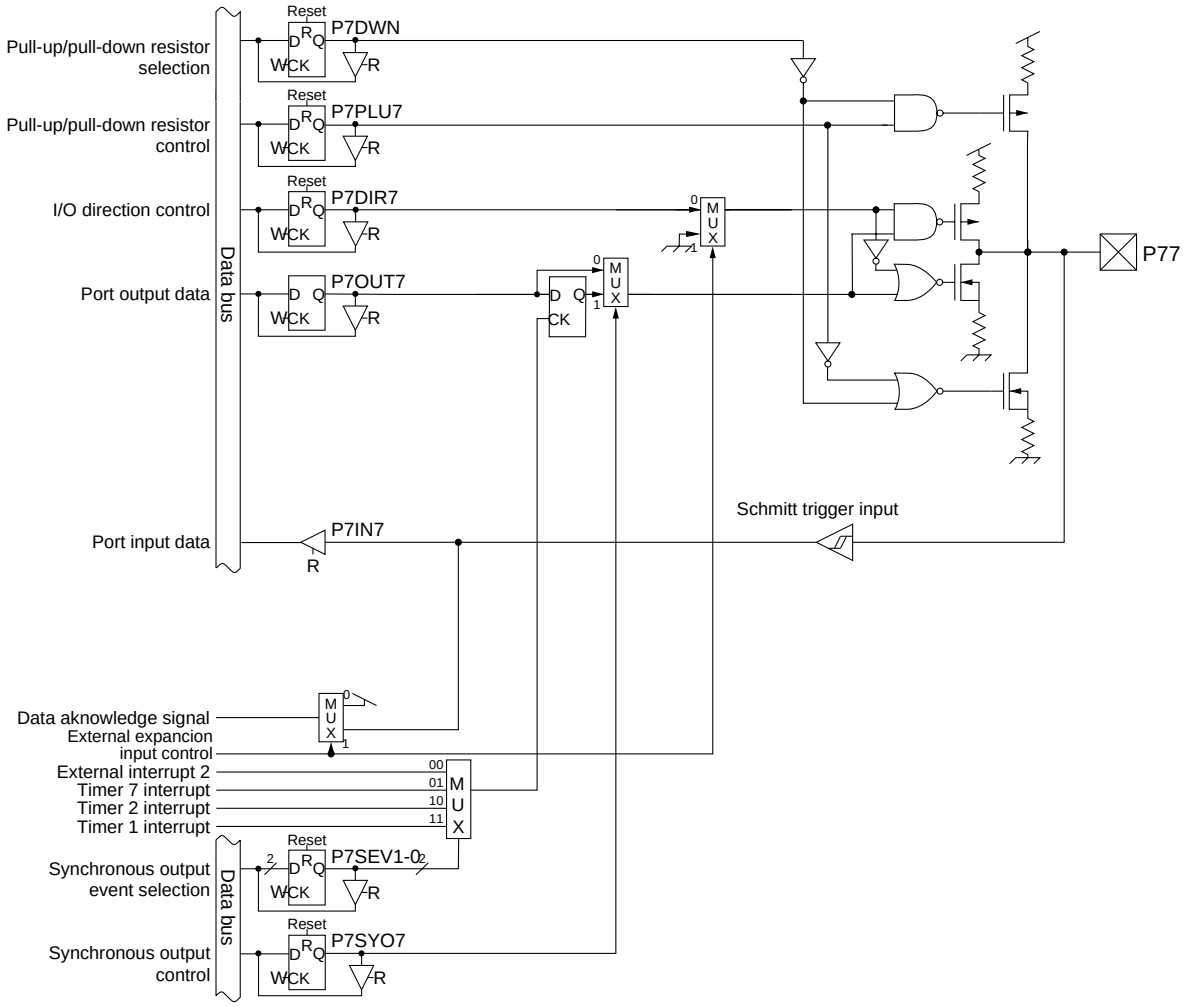


Figure:4.9.8 P77 Block Diagram

4.10 Port 8

4.10.1 Description

■ General Port Setup

To output the data to pins, set the control flag of the port 8 direction control register (P8DIR) to "1" to write the value of the port 8 output register (P8OUT).

To read input data of pins, set the control flag of the port 8 direction control register (P8DIR) to "0" to read the value of the port 8 input register (P8IN).

Each bit can be set individually as either an input or output by the port 8 I/O direction control register (P8DIR). The control flag of the port 8 direction control register (P8DIR) is set to "1" for output mode, and "0" for input mode.

Each bit can be set individually if pull-up resistor is added or not, by the port 8 pull-up resistor control register (P8PLU). Set the control flag of the port 8 pull-up resistor control register (P8PLU) to "1" to add pull-up resistor.

■ Special Function Pin Setup

P80 is used as LED drivering pin,as well.

P81 is used as LED drivering pin,as well.

P82 is used as LED drivering pin,as well.

P83 is used as LED drivering pin,as well.

P84 is used as LED drivering pin,as well.

P85 is used as LED drivering pin,as well.

P86 is used as LED drivering pin,as well.

P87 is used as LED drivering pin,as well.

P80 is data I/O pin with the external extension memory at the processor mode or the memory extension mode. These modes can not be controlled to I/O by the register.

P81 is data I/O pin with the external extension memory at the processor mode or the memory extension mode. These modes can not be controlled to I/O by the register.

P82 is data I/O pin with the external extension memory at the processor mode or the memory extension mode. These modes can not be controlled to I/O by the register.

P83 is data I/O pin with the external extension memory at the processor mode or the memory extension mode. These modes can not be controlled to I/O by the register.

P84 is data I/O pin with the external extension memory at the processor mode or the memory extension mode. These modes can not be controlled to I/O by the register.

P85 is data I/O pin with the external extension memory at the processor mode or the memory extension mode. These modes can not be controlled to I/O by the register.

P86 is data I/O pin with the external extension memory at the processor mode or the memory extension mode. These modes can not be controlled to I/O by the register.

P87 is data I/O pin with the external extension memory at the processor mode or the memory extension mode. These modes can not be controlled to I/O by the register.

4.10.2 Registers

The following Table shows registers that control the Port 8

Table:4.10.1 Port 8control register

Registers	Address	R/W	Function	Page
P8OUT	0x03F18	R/W	Port 8 Output Register	IV-81
P8IN	0x03F28	R	Port 8 Input Register	IV-82
P8DIR	0x03F38	R/W	Port 8 Direction Control Register	IV-82
P8PLU	0x03F48	R/W	Port 8 Pull-up Resistor Control Register	IV-83

R/W:Readable/Writable

■ Port 8 Output Register(P8OUT:0x03F18)

bp	7	6	5	4	3	2	1	0
Flag	P8OUT7	P8OUT6	P8OUT5	P8OUT4	P8OUT3	P8OUT2	P8OUT1	P8OUT0
At reset	x	x	x	x	x	x	x	x
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bp	Flag	Description
7 6 5 4 3 2 1 0	P8OUT7 P8OUT6 P8OUT5 P8OUT4 P8OUT3 P8OUT2 P8OUT1 P8OUT0	Output data 0:Output L(VSS level) 1:Output H(VDD level)

■ Port 8 Input Register(P8IN:0x03F28)

bp	7	6	5	4	3	2	1	0
Flag	P8IN7	P8IN6	P8IN5	P8IN4	P8IN3	P8IN2	P8IN1	P8IN0
At reset	x	x	x	x	x	x	x	x
Access	R	R	R	R	R	R	R	R

bp	Flag	Description
7 6 5 4 3 2 1 0	P8IN7 P8IN6 P8IN5 P8IN4 P8IN3 P8IN2 P8IN1 P8IN0	Input data 0:Pin is L(VSS level) 1:Pin is H(VDD level)

■ Port 8 Direction Control Register(P8DIR:0x03F38)

bp	7	6	5	4	3	2	1	0
Flag	P8DIR7	P8DIR6	P8DIR5	P8DIR4	P8DIR3	P8DIR2	P8DIR1	P8DIR0
At reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bp	Flag	Description
7 6 5 4 3 2 1 0	P8DIR7 P8DIR6 P8DIR5 P8DIR4 P8DIR3 P8DIR2 P8DIR1 P8DIR0	I/O mode selection 0:Input mode 1:Output mode

■ Port 8 Pull-up Resistor Control Register(P8PLU:0x03F48)

bp	7	6	5	4	3	2	1	0
Flag	P8PLU7	P8PLU6	P8PLU5	P8PLU4	P8PLU3	P8PLU2	P8PLU1	P8PLU0
At reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bp	Flag	Description
7 6 5 4 3 2 1 0	P8PLU7 P8PLU6 P8PLU5 P8PLU4 P8PLU3 P8PLU2 P8PLU1 P8PLU0	Pull-up resistor selection 0:Not added 1:Added

4.10.3 Block Diagram

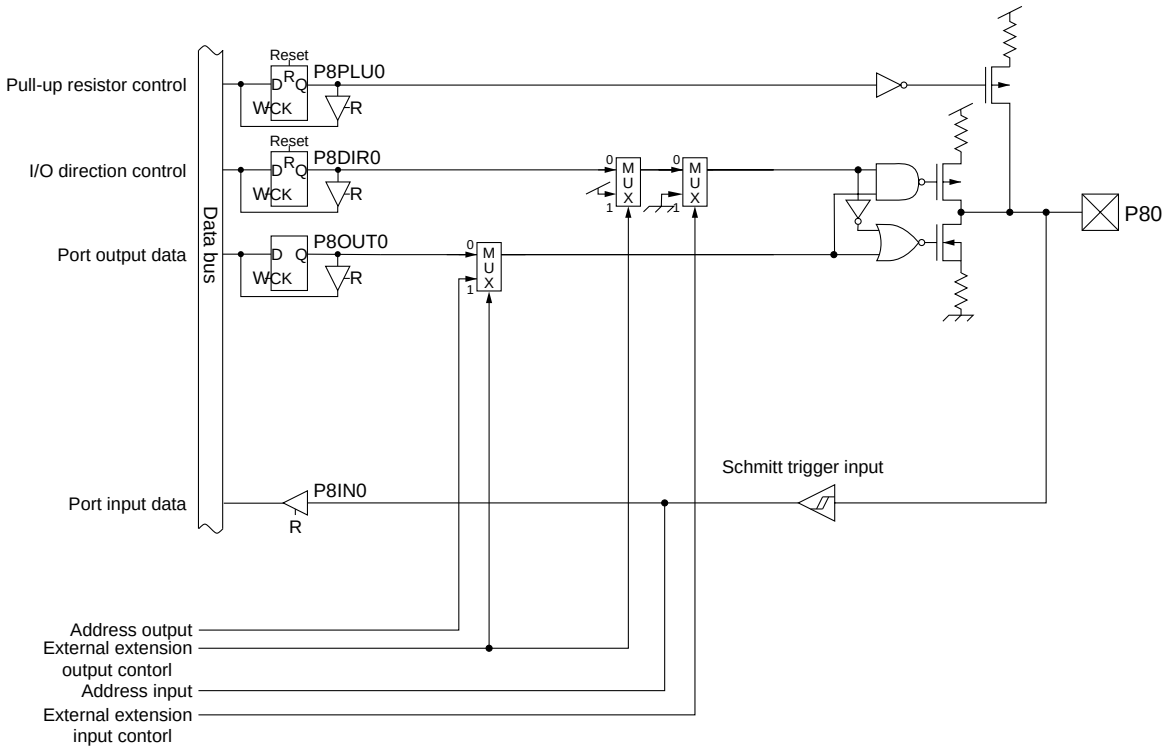


Figure:4.10.1 P80 Block Diagram

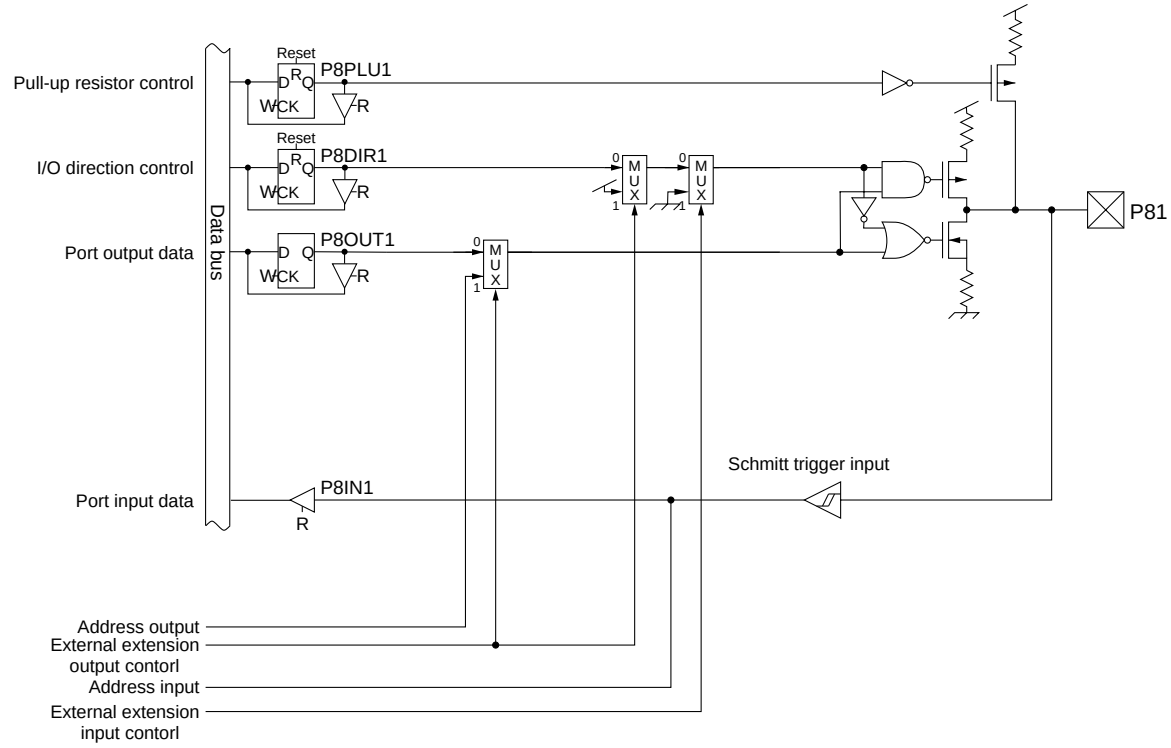


Figure:4.10.2 P81 Block Diagram

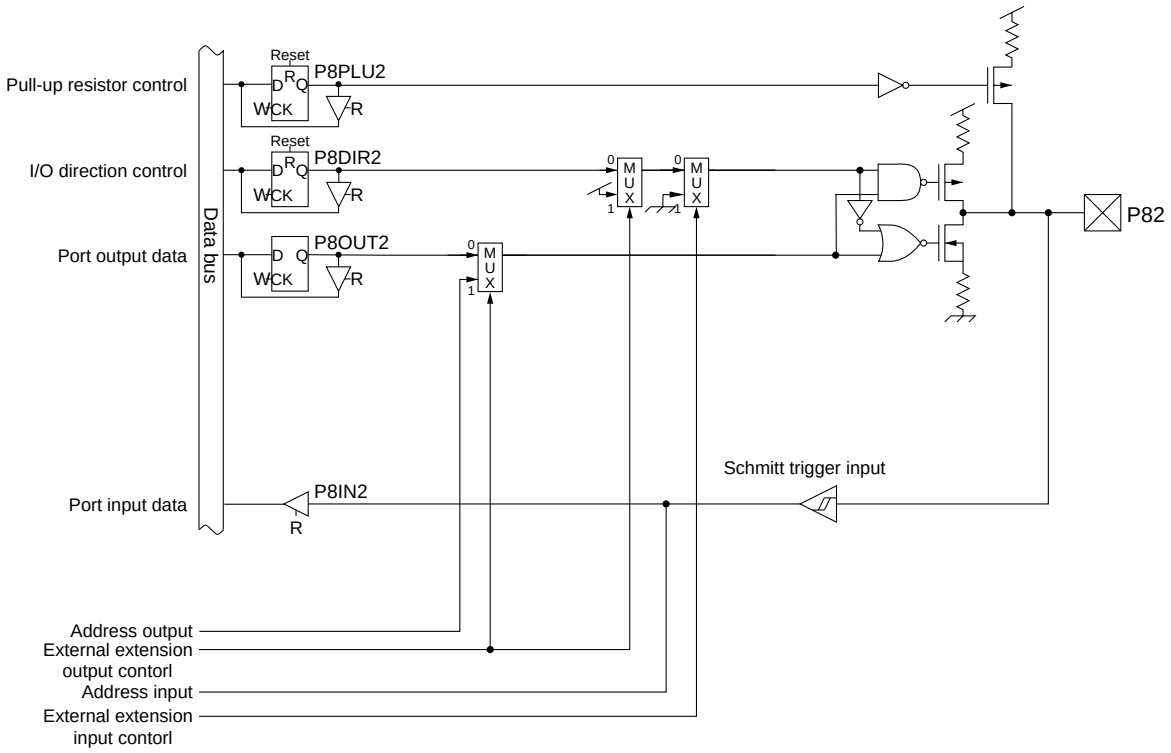


Figure:4.10.3 P82 Block Diagram

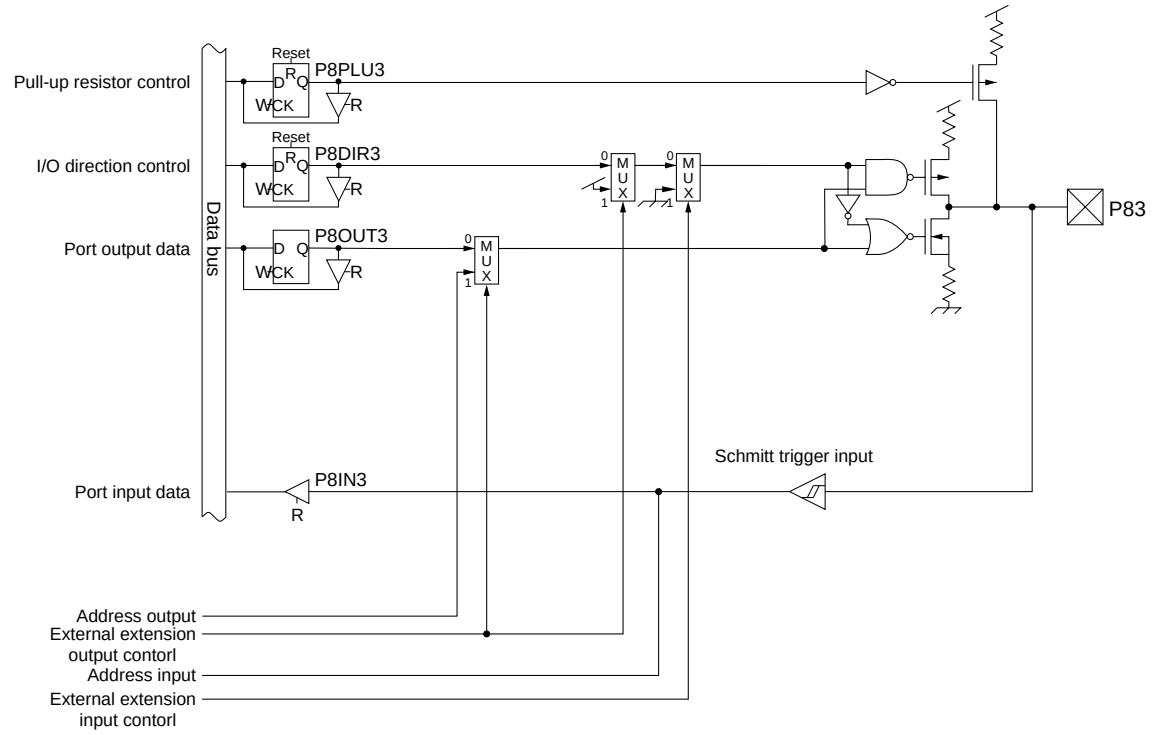


Figure:4.10.4 P83 Block Diagram

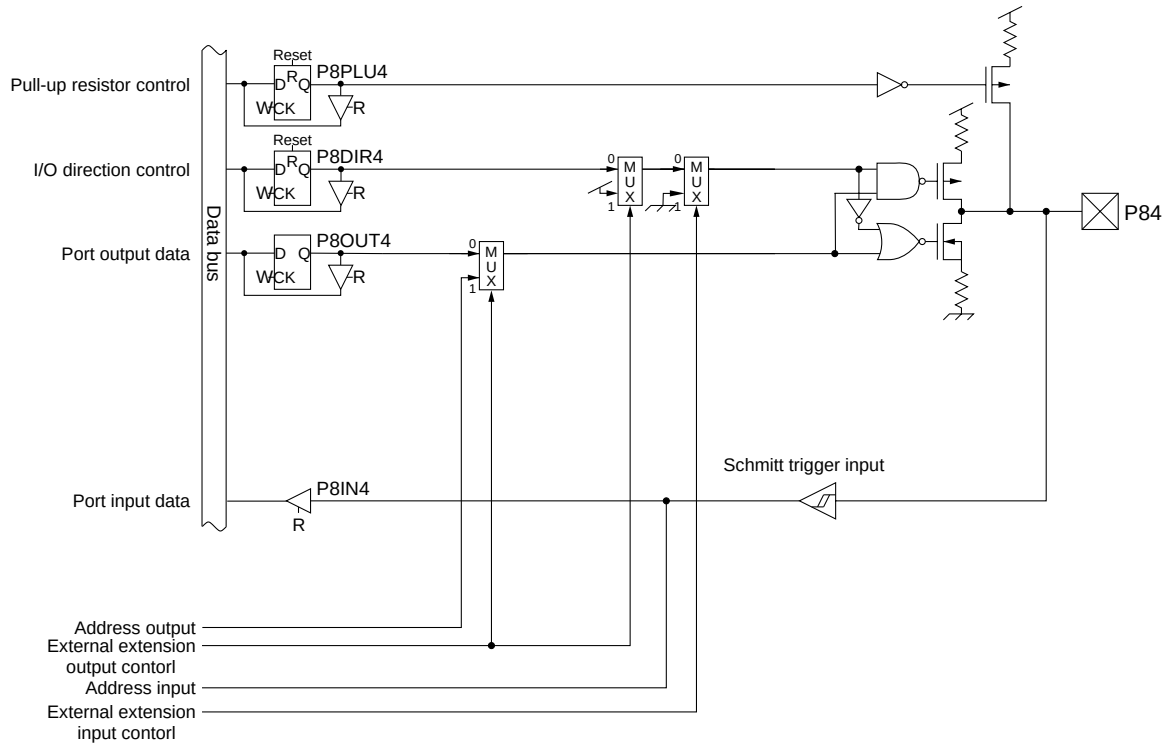


Figure:4.10.5 P84 Block Diagram

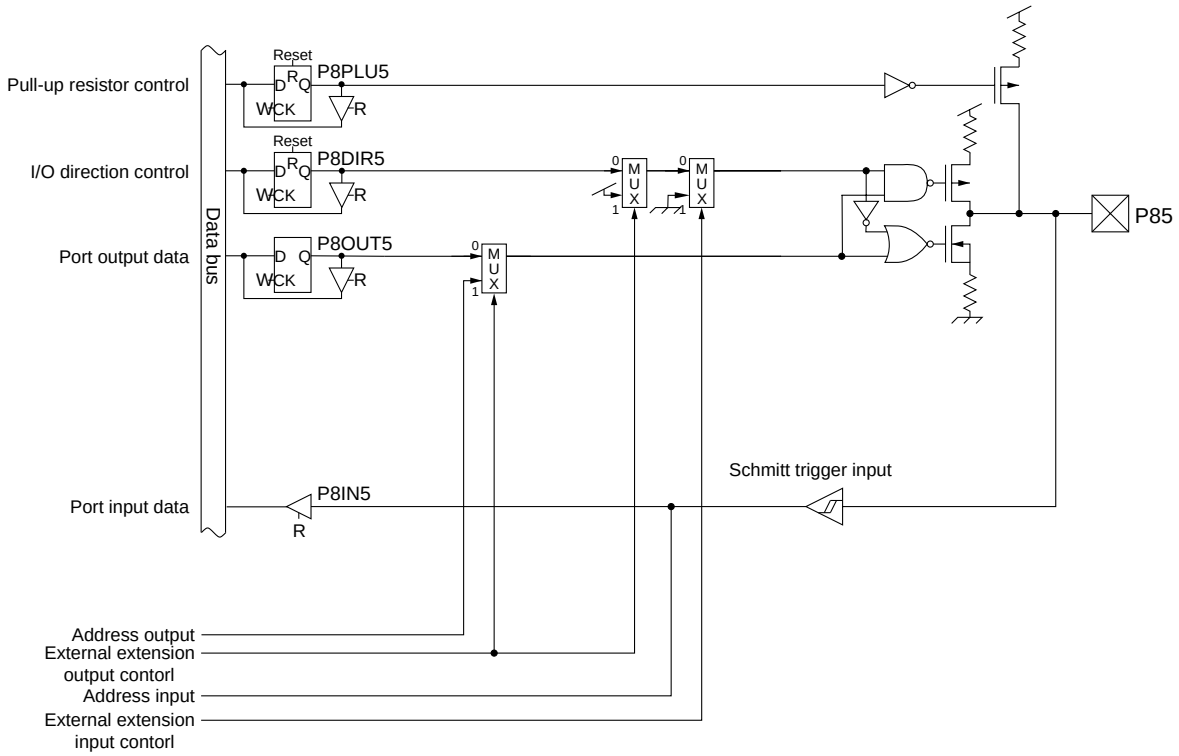


Figure:4.10.6 P85 Block Diagram

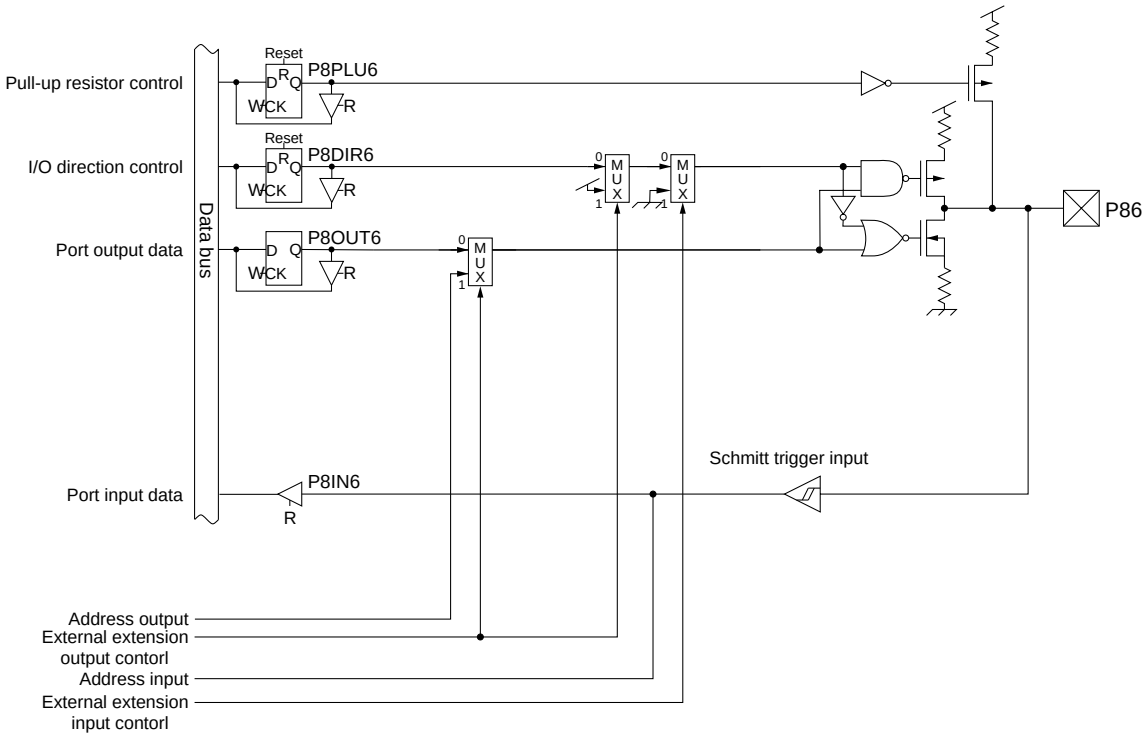


Figure:4.10.7 P86 Block Diagram

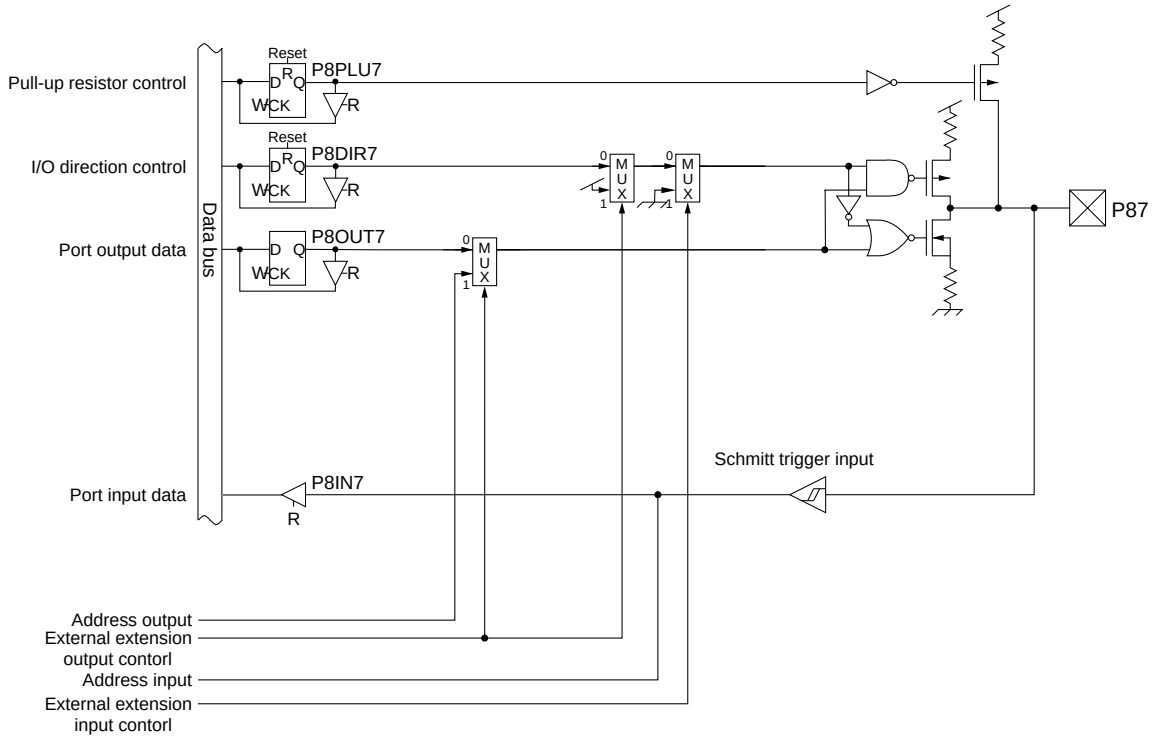


Figure:4.10.8 P87 Block Diagram

4.11 Port 9

4.11.1 Description

■ General Port Setup

To output the data to pins, set the control flag of the port 9 direction control register (P9DIR) to "1" to write the value of the port 9 output register (P9OUT).

To read input data of pins, set the control flag of the port 9 direction control register (P9DIR) to "0" to read the value of the port 9 input register (P9IN).

Each bit can be set individually as either an input or output by the port 9 I/O direction control register (P9DIR). The control flag of the port 9 direction control register (P9DIR) is set to "1" for output mode, and "0" for input mode.

Each bit can be set individually if pull-up resistor is added or not, by the port 9 pull-up resistor control register (P9PLU). Set the control flag of the port 9 pull-up resistor control register (P9PLU) to "1" to add pull-up resistor.

P90, P92, P93, and P95 can select the Nch open-drain output by each bit by the port 9 Nch open-drain control register (P9ODC). The port 9 Nch open-drain control register (P9ODC) is set to "1" for the Nch open-drain output and "0" for the push-pull output.

■ Special Function Pin Setup

P90 is used as output pin of the serial 0 transmission data or the UART 0 transmission data, as well. When the SC0SBOS flag of the serial interface 0 mode register 1 (SC0MD1) is set to "1", it is output pin of the serial data. Also, the push-pull output or the Nch open-drain output can be selected by the setup of the port 9 Nch open-drain control register (P9ODC).

P91 is used as input pin of the serial 0 reception data or the UART 0 reception data, as well.

P92 is used as I/O pin of the serial 0 clock, as well. When the SC0SBTS flag of the serial interface 0 mode register 1 (SC0MD1) is set to "1", it is output pin of the serial clock. Also, the push-pull output or the Nch open-drain output can be selected by the setup of the port 9 Nch open-drain control register (P9ODC).

Also, serial 0 I/O pin can be selected by setting of serial I/O pin switching control register (SCSEL). When SC0SEL flag of serial I/O pin switching control register (SCSEL) is 0, for P00 to P02, and 1 for P90 to P92.

P93 is used as output pin of the serial 0 transmission data or the IIC3 transmission data, as well. When the SC3SBOS flag of the serial interface 3 mode register 1 (SC3MD1) is set to "1", it is output pin of the serial data. Also, the push-pull output or the Nch open-drain output can be selected by the setup of the port 9 Nch open-drain control register (P9ODC).

P94 is used as input pin of the serial 3 reception data or the IIC 3 reception data.

P95 is used as I/O pin of the serial 3 clock, as well. When the SC3SBTS flag of the serial interface 3 mode register 1 (SC3MD1) is set to "1", it is output pin of the serial clock. Also, the push-pull output or the Nch open-drain output can be selected by the setup of the port 9 Nch open-drain control register (P9ODC).

Also, serial 3 I/O pin can be selected by setting of serial I/O pin switching control register (SCSEL). When SC3SEL flag of serial I/O pin switching control register (SCSEL) is 0, for P33 to P35, and 1 for P93 to P95.

4.11.2 Registers

The following Table shows registers that control the Port 9

Table:4.11.1 Port 9control register

Registers	Address	R/W	Function	Page
P9OUT	0x03F19	R/W	Port 9 Output Register	IV-90
P9IN	0x03F29	R	Port 9 Input Register	IV-91
P9DIR	0x03F39	R/W	Port 9 Direction Control Register	IV-91
P9PLU	0x03F49	R/W	Port 9 Pull-up Resistor Control Register	IV-92
P9ODC	0x03F4C	R/W	Port 9 Nch Open-drain Control Register	IV-92

R/W:Readable/Writable

■ Port 9 Output Register(P9OUT:0x03F19)

bp	7	6	5	4	3	2	1	0
Flag	-	-	P9OUT5	P9OUT4	P9OUT3	P9OUT2	P9OUT1	P9OUT0
At reset	-	-	x	x	x	x	x	x
Access	-	-	R/W	R/W	R/W	R/W	R/W	R/W

bp	Flag	Description
7 6 5 4 3 2 1 0	- - P9OUT5 P9OUT4 P9OUT3 P9OUT2 P9OUT1 P9OUT0	Output data 0:Output L(VSS level) 1:Output H(VDD level)

■ Port 9 Input Register(P9IN:0x03F29)

bp	7	6	5	4	3	2	1	0
Flag	-	-	P9IN5	P9IN4	P9IN3	P9IN2	P9IN1	P9IN0
At reset	-	-	x	x	x	x	x	x
Access	-	-	R	R	R	R	R	R

bp	Flag	Description
7 6 5 4 3 2 1 0	- - P9IN5 P9IN4 P9IN3 P9IN2 P9IN1 P9IN0	Input data 0:Pin is L(VSS level) 1:Pin is H(VDD level)

■ Port 9 Direction Control Register(P9DIR:0x03F39)

bp	7	6	5	4	3	2	1	0
Flag	-	-	P9DIR5	P9DIR4	P9DIR3	P9DIR2	P9DIR1	P9DIR0
At reset	-	-	0	0	0	0	0	0
Access	-	-	R/W	R/W	R/W	R/W	R/W	R/W

bp	Flag	Description
7 6 5 4 3 2 1 0	- - P9DIR5 P9DIR4 P9DIR3 P9DIR2 P9DIR1 P9DIR0	I/O mode selection 0:Input mode 1:Output mode

■ Port 9 Pull-up Resistor Control Register(P9PLU:0x03F49)

bp	7	6	5	4	3	2	1	0
Flag	-	-	P9PLU5	P9PLU4	P9PLU3	P9PLU2	P9PLU1	P9PLU0
At reset	-	-	0	0	0	0	0	0
Access	-	-	R/W	R/W	R/W	R/W	R/W	R/W

bp	Flag	Description
7 6 5 4 3 2 1 0	- - P9PLU5 P9PLU4 P9PLU3 P9PLU2 P9PLU1 P9PLU0	Pull-up resistor selection 0:Not added 1:Added

■ Port 9 Nch Open-drain Control Register(P9ODC:0x03F4C)

bp	7	6	5	4	3	2	1	0
Flag	-	-	P9ODC5	-	P9ODC3	P9ODC2	-	P9ODC0
At reset	-	-	0	-	0	0	-	0
Access	-	-	R/W	-	R/W	R/W	-	R/W

bp	Flag	Description
7 6 5 4 3 2 1 0	- - P9ODC5 - P9ODC3 P9ODC2 - P9ODC0	Nch open-drain output selection 0:Push/pull output 1:Nch open-drain output

4.11.3 Block Diagram

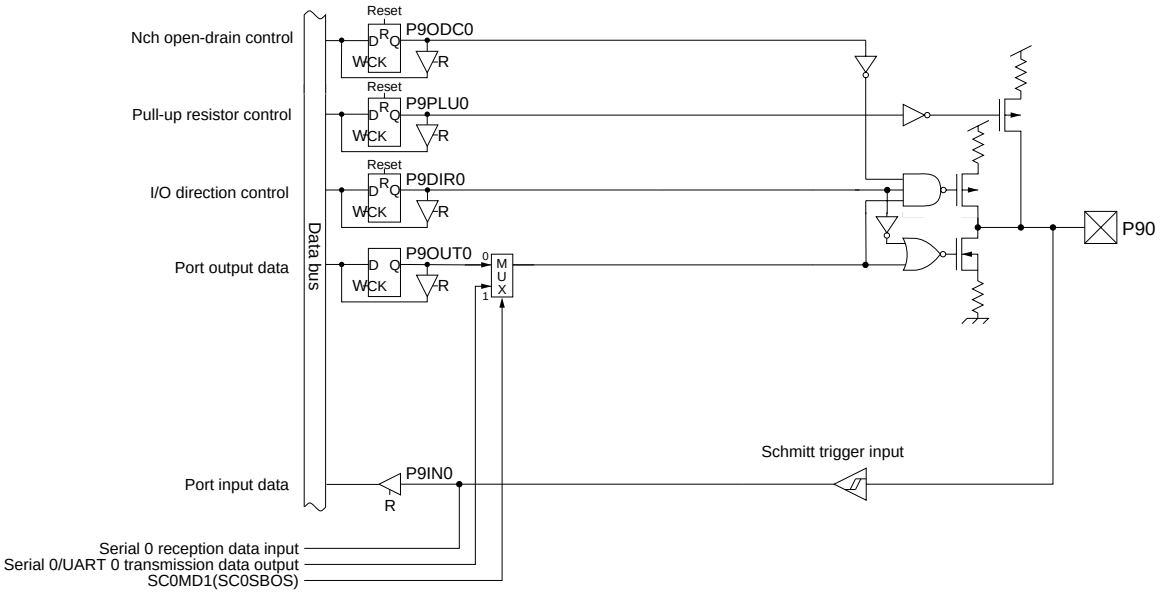


Figure:4.11.1 P90 Block Diagram

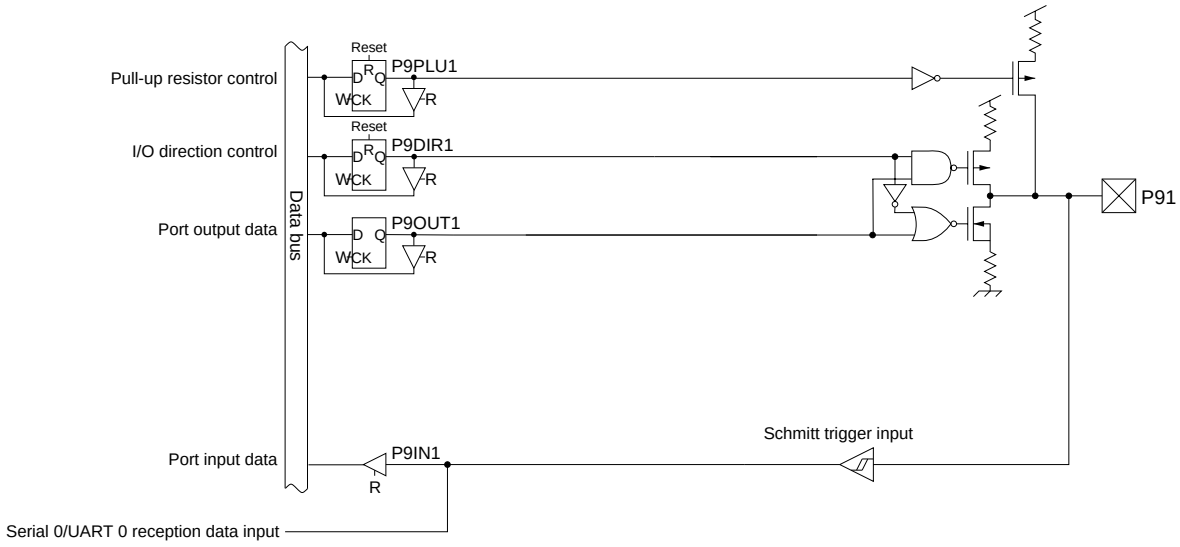


Figure:4.11.2 P91 Block Diagram

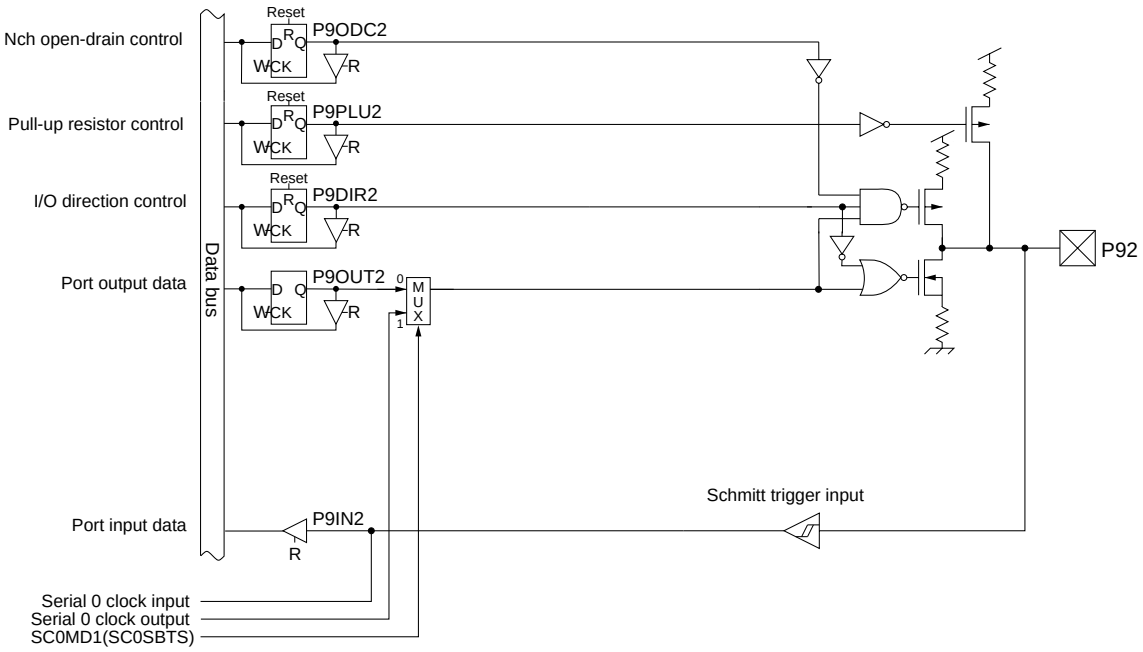


Figure:4.11.3 P92 Block Diagram

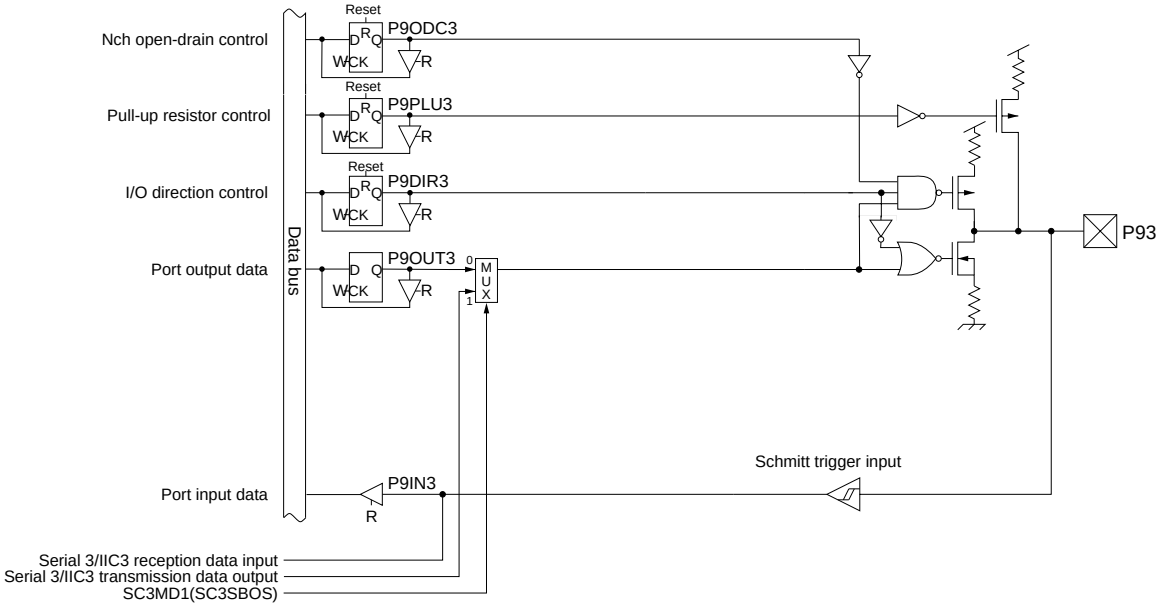


Figure:4.11.4 P93 Block Diagram

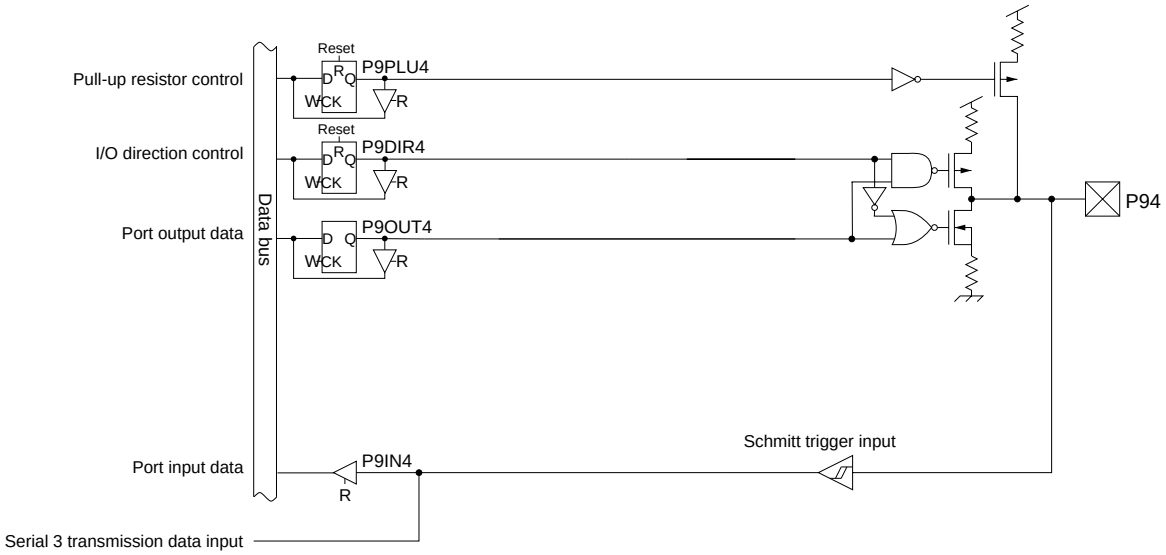


Figure:4.11.5 P94 Block Diagram

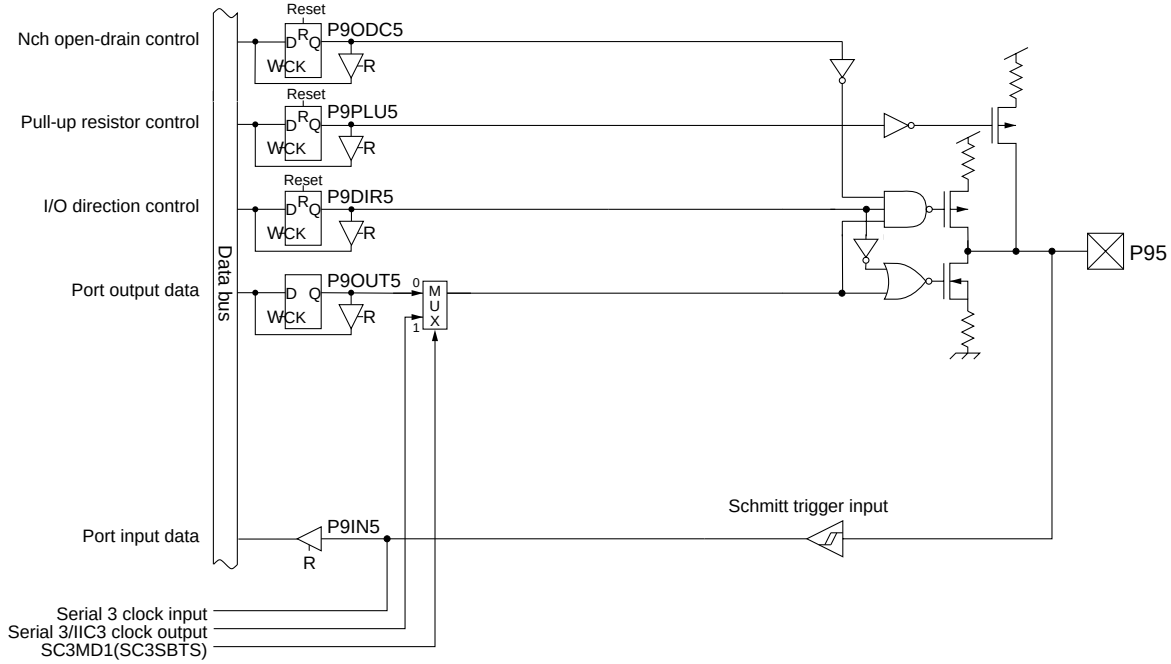


Figure:4.11.6 P95 Block Diagram

4.12 Port A

4.12.1 Description

■ General Port Setup

To output the data to pins, set the control flag of the port A direction control register (PADIR) to "1" to write the value of the port A output register (PAOUT).

To read input data of pins, set the control flag of the port A direction control register (PADIR) to "0" to read the value of the port A input register (PAIN).

Each bit can be set individually as either an input or output by the port A I/O direction control register (PADIR). The control flag of the port A direction control register (PADIR) is set to "1" for output mode, and "0" for input mode.

Each bit can be set individually if pull-up or pull-down resistor is added or not, by the port A pull-up/pull-down resistor control register (PAPLU). Set the control flag of the port A pull-up/pull-down resistor control register (PAPLU) to "1" to add pull-up/pull-down resistor.

Port A can be selected to add pull-up resistor or pull-down resistor by bp2 of the pull-up/pull-down resistor selection register (SELUD).

Each bit can be selected individually as input mode by the port A input mode register (PAIMD). The port A input mode register (PAIMD) is set to "1" to input the special function data and 1 is read out from the portA input register (PAIN), and "0" to use as the general port.

■ Special Function Pin Setup

PA0 is used as input pin for analog, as well. Each bit can be set individually as an input by the port A input mode register (PAIMD). When it is used as the analog input pin, set the port A input mode register to "1".Then, the value of the port A is read to be "1".

PA1 is used as input pin for analog, as well. Each bit can be set individually as an input by the port A input mode register (PAIMD). When it is used as the analog input pin, set the port A input mode register to "1".Then, the value of the port A is read to be "1".

PA2 is used as input pin for analog, as well. Each bit can be set individually as an input by the port A input mode register (PAIMD). When it is used as the analog input pin, set the port A input mode register to "1".Then, the value of the port A is read to be "1".

PA3 is used as input pin for analog, as well. Each bit can be set individually as an input by the port A input mode register (PAIMD). When it is used as the analog input pin, set the port A input mode register to "1".Then, the value of the port A is read to be "1".

PA4 is used as input pin for analog, as well. Each bit can be set individually as an input by the port A input mode register (PAIMD). When it is used as the analog input pin, set the port A input mode register to "1".Then, the value of the port A is read to be "1".

PA5 is used as input pin for analog, as well. Each bit can be set individually as an input by the port A input mode register (PAIMD). When it is used as the analog input pin, set the port A input mode register to "1".Then, the value of the port A is read to be "1".

PA6 is used as input pin for analog, as well. Each bit can be set individually as an input by the port A input mode register (PAIMD). When it is used as the analog input pin, set the port A input mode register to "1".Then, the value of the port A is read to be "1".

PA7 is used as input pin for analog, as well. Each bit can be set individually as an input by the port A input mode register (PAIMD). When it is used as the analog input pin, set the port A input mode register to "1".Then, the value of the port A is read to be "1".

4.12.2 Registers

The following Table shows registers that control the Port A

Table:4.12.1 Port A control register

Registers	Address	R/W	Function	Page
PAOUT	0x03F1A	R/W	Port A Output Register	IV-97
PAIN	0x03F2A	R	Port A Input Register	IV-98
PADIR	0x03F3A	R/W	Port A Direction Control Register	IV-98
PAPLU	0x03F4A	R/W	Port A Pull-up/Pull-down Resistor Control Register	IV-99
PAIMD	0x03F3B	R/W	Port A Input Mode Register	IV-99
SELUD	0x03F4B	R/W	Pull-up/Pull-down Resistor Selection Register	IV-100

R/W:Readable/Writable

■ Port A Output Register(PAOUT:0x03F1A)

bp	7	6	5	4	3	2	1	0
Flag	PAOUT7	PAOUT6	PAOUT5	PAOUT4	PAOUT3	PAOUT2	PAOUT1	PAOUT0
At reset	x	x	x	x	x	x	x	x
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bp	Flag	Description
7 6 5 4 3 2 1 0	PAOUT7 PAOUT6 PAOUT5 PAOUT4 PAOUT3 PAOUT2 PAOUT1 PAOUT0	Output data 0:Output L(VSS level) 1:Output H(VDD level)

■ Port A Input Register(PAIN:0x03F2A)

bp	7	6	5	4	3	2	1	0
Flag	PAIN7	PAIN6	PAIN5	PAIN4	PAIN3	PAIN2	PAIN1	PAIN0
At reset	x	x	x	x	x	x	x	x
Access	R	R	R	R	R	R	R	R

bp	Flag	Description
7 6 5 4 3 2 1 0	PAIN7 PAIN6 PAIN5 PAIN4 PAIN3 PAIN2 PAIN1 PAIN0	Input data 0:Pin is L(VSS level) 1:Pin is H(VDD level)

■ Port A Direction Control Register(PADIR:0x03F3A)

bp	7	6	5	4	3	2	1	0
Flag	PADIR7	PADIR6	PADIR5	PADIR4	PADIR3	PADIR2	PADIR1	PADIR0
At reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bp	Flag	Description
7 6 5 4 3 2 1 0	PADIR7 PADIR6 PADIR5 PADIR4 PADIR3 PADIR2 PADIR1 PADIR0	I/O mode selection 0:Input mode 1:Output mode

■ Port A Pull-up/Pull-down Resistor Control Register(PAPLU:0x03F4A)

bp	7	6	5	4	3	2	1	0
Flag	PAPLU7	PAPLU6	PAPLU5	PAPLU4	PAPLU3	PAPLU2	PAPLU1	PAPLU0
At reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bp	Flag	Description
7 6 5 4 3 2 1 0	PAPLU7 PAPLU6 PAPLU5 PAPLU4 PAPLU3 PAPLU2 PAPLU1 PAPLU0	Pull-up/pull-down resistor selection 0:Not added 1:Added

■ Port A Input Mode Register(PAIMD:0x03F3B)

bp	7	6	5	4	3	2	1	0
Flag	PAIMD7	PAIMD6	PAIMD5	PAIMD4	PAIMD3	PAIMD2	PAIMD1	PAIMD0
At reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bp	Flag	Description
7 6 5 4 3 2 1 0	PAIMD7 PAIMD6 PAIMD5 PAIMD4 PAIMD3 PAIMD2 PAIMD1 PAIMD0	Analog input selection 0:I/O port 1:Analog input

■ Pull-up/Pull-down Resistor Selection Register(SELUD:0x03F4B)

bp	7	6	5	4	3	2	1	0
Flag	-	-	-	-	-	PADWN	P7DWN	P4DWN
At reset	-	-	-	-	-	0	0	0
Access	-	-	-	-	-	R/W	R/W	R/W

bp	Flag	Description
7	-	-
6	-	-
5	-	-
4	-	-
3	-	-
2	PADWN	Port A pull-up/pull-down selection 0:Pull-up 1:Pull-down
1	P7DWN	Port 7 pull-up/pull-down selection 0:Pull-up 1:Pull-down
0	P4DWN	Port 4 pull-up/pull-down selection 0:Pull-up 1:Pull-down

4.12.3 Block Diagram

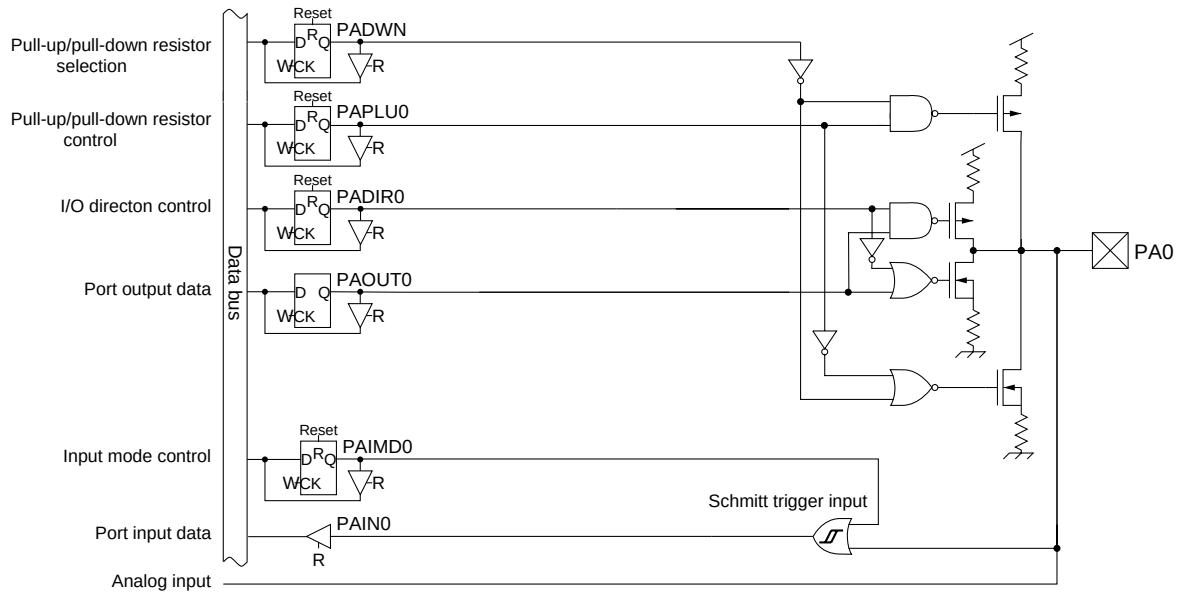


Figure:4.12.1 PA0 Block Diagram

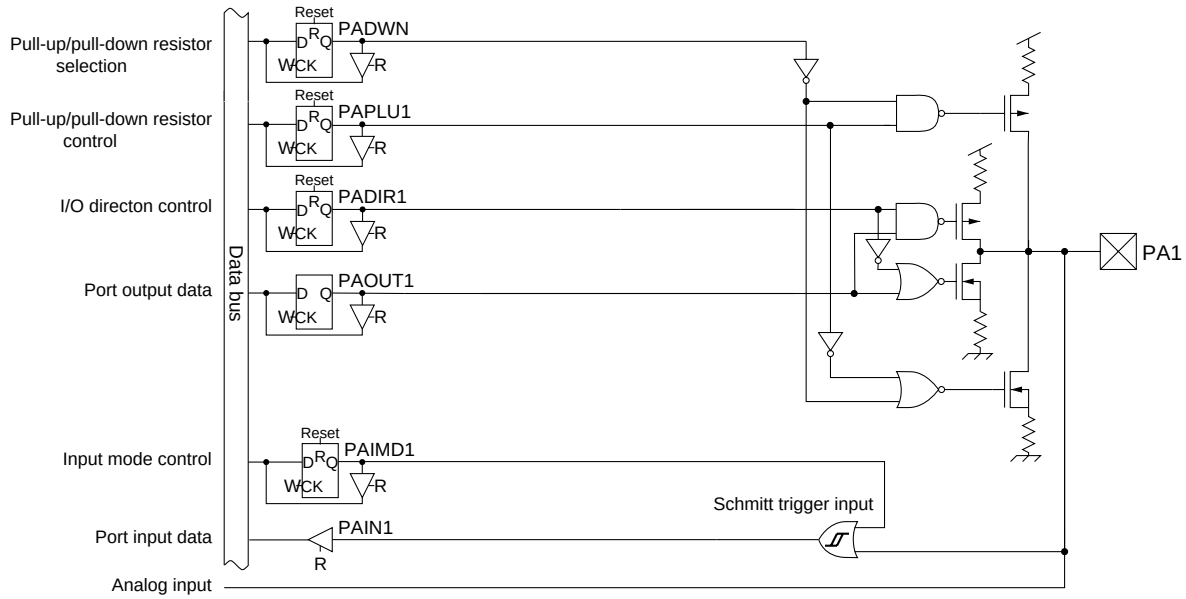


Figure:4.12.2 PA1 Block Diagram

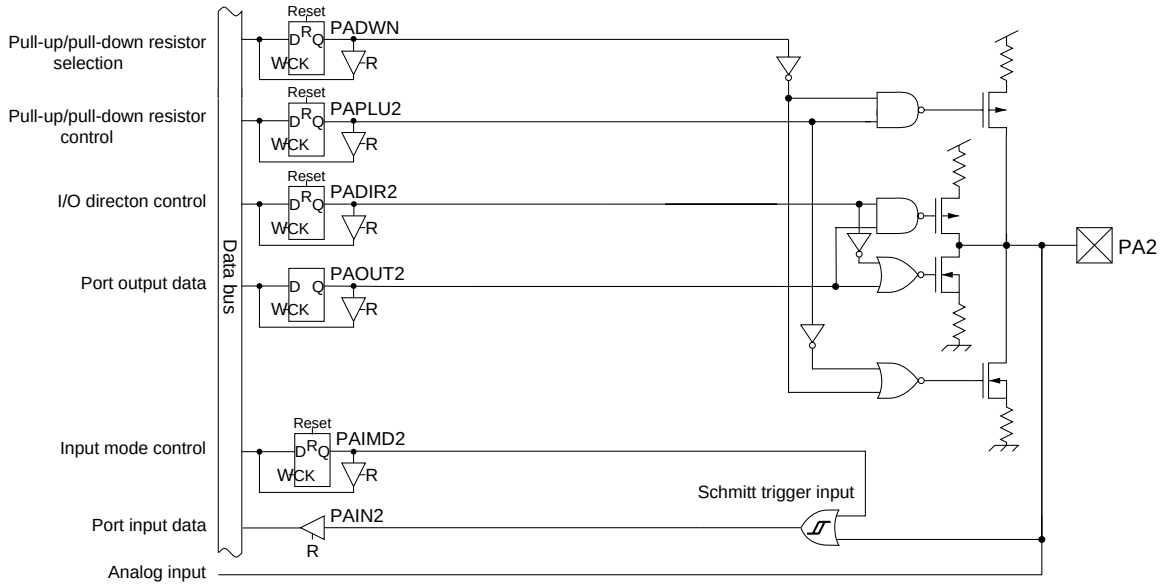


Figure:4.12.3 PA2 Block Diagram

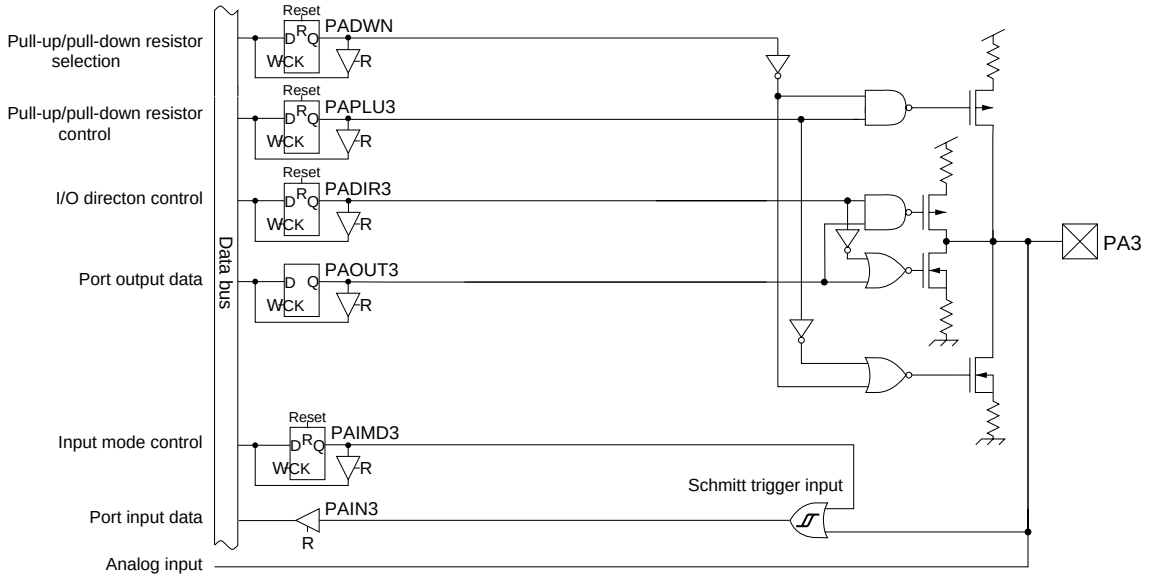


Figure:4.12.4 PA3 Block Diagram

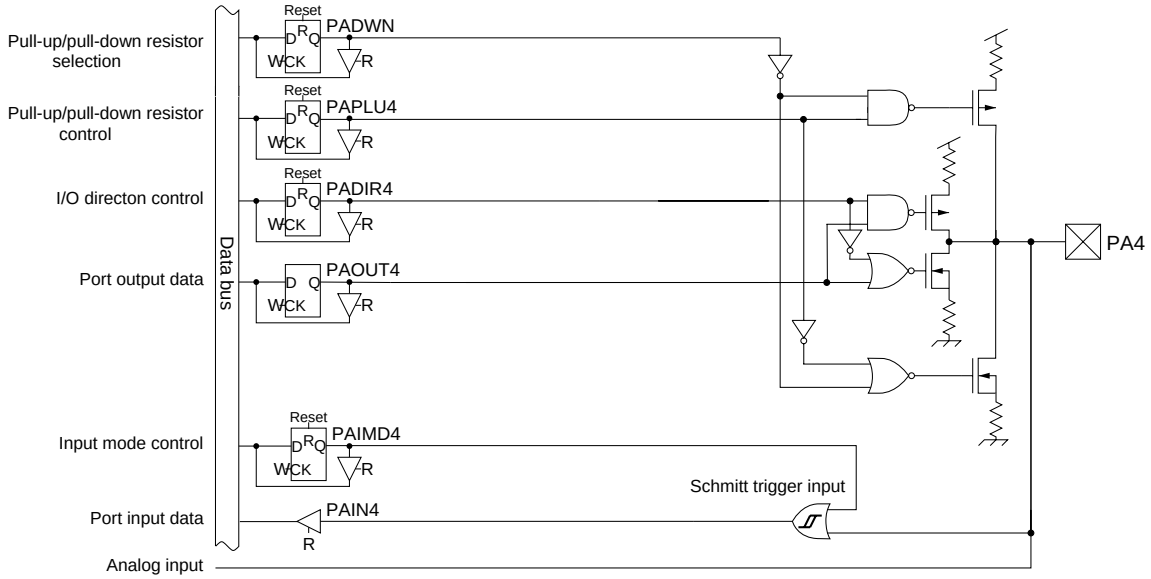


Figure:4.12.5 PA4 Block Diagram

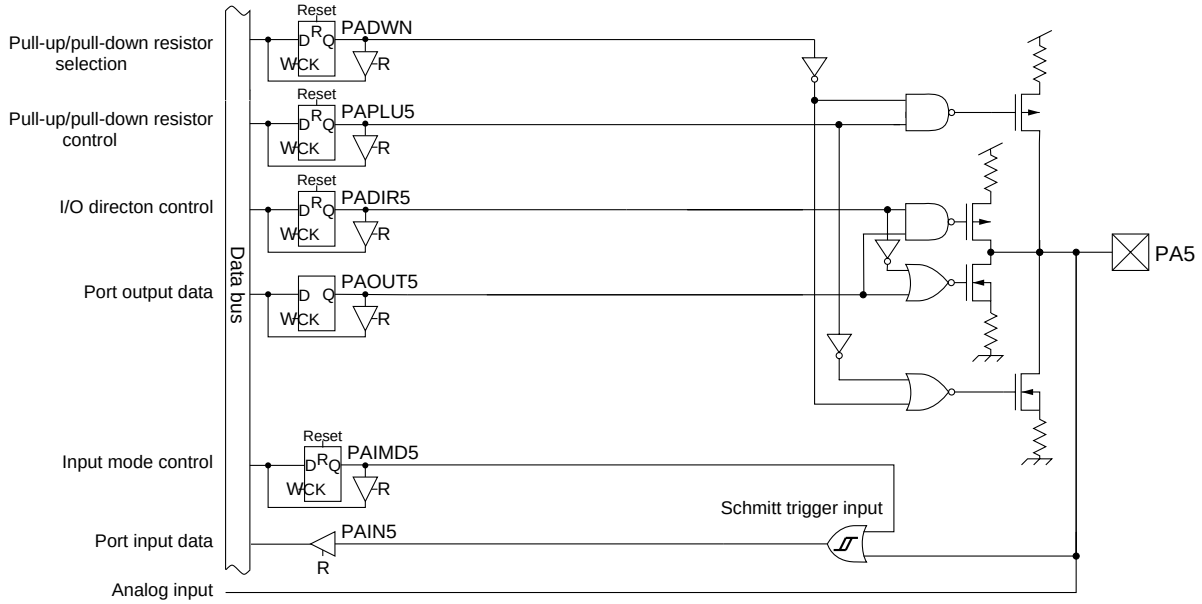


Figure:4.12.6 PA5 Block Diagram

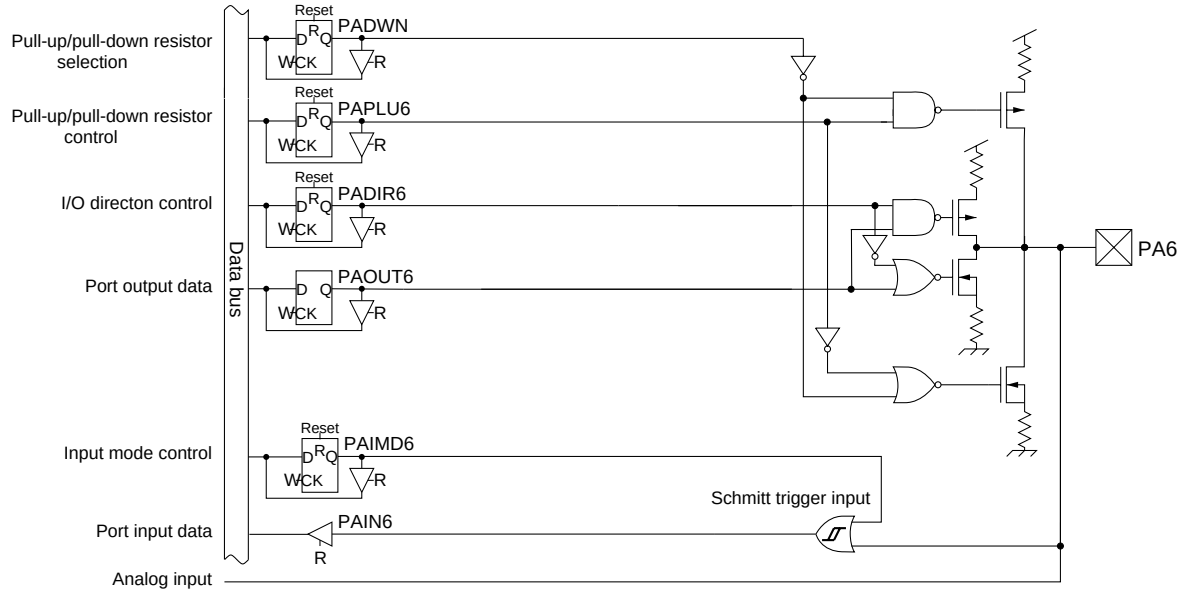


Figure:4.12.7 PA6 Block Diagram

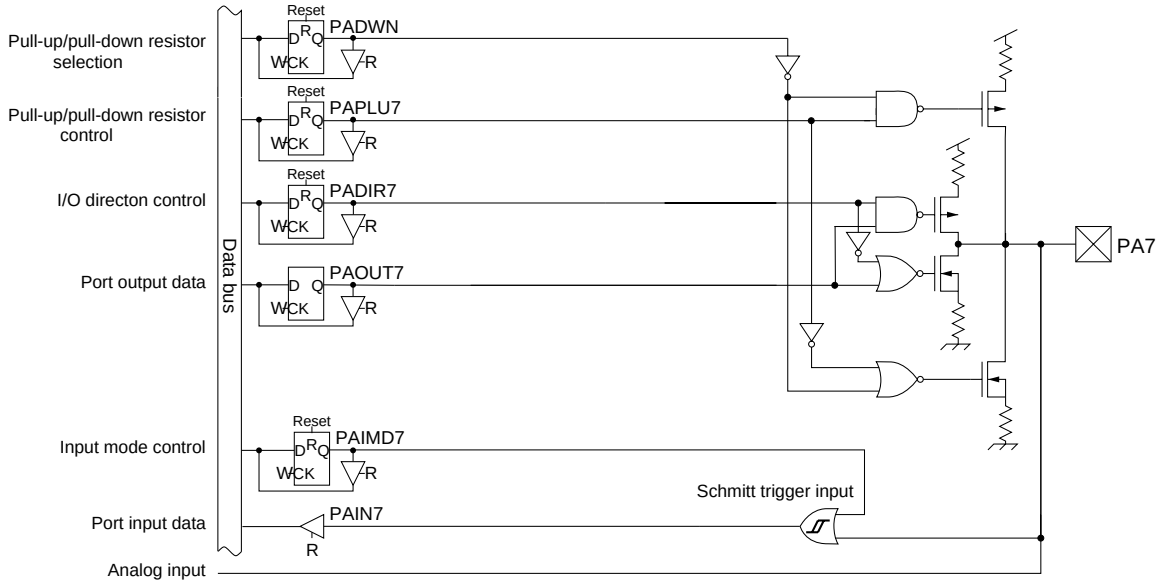


Figure:4.12.8 PA7 Block Diagram

4.13 Port D

4.13.1 Description

■ General Port Setup

To output the data to pins, set the control flag of the port D direction control register (PDDIR) to "1" to write the value of the port D output register (PDOUT).

To read input data of pins, set the control flag of the port D direction control register (PDDIR) to "0" to read the value of the port D input register (PDIN).

Each bit can be set individually as either an input or output by the port D I/O direction control register (PDDIR). The control flag of the port D direction control register (PDDIR) is set to "1" for output mode, and "0" for input mode.

Each bit can be set individually if pull-up resistor is added or not, by the port D pull-up resistor control register (PDPLU). Set the control flag of the port D pull-up resistor control register (PDPLU) to "1" to add pull-up resistor.

Each bit can be selected individually as output mode by the port D output mode register (PDOMD). The port D output mode register (PDOMD) is set to "1" to output the special function data, and "0" to use as the general port.

■ Special Function Pin Setup

PD0 is used as external interrupt 1 pin, as well.

External interrupt 2 can select either P22 or PD0 by setting of the external interrupt pin switching control register (IRQSEL). When IRQ2SEL flag of the external interrupt pin switching control register (IRQSEL) is 0, P22 is selected and 1, PD0 is selected.

PD1 is used as external interrupt 3 pin, as well.

External interrupt 3 can select either P23 or PD1 by setting of the external interrupt pin switching control register (IRQSEL). When IRQ3SEL flag of the external interrupt pin switching control register (IRQSEL) is 0, P23 is selected and 1, PD1 is selected.

PD2 is used as I/O pin of the timer 4, as well. The output mode can be selected by bp2 of the port D output mode register (PDOMD) by each bit. The port D output mode register (PDOMD) is set to "1" to output the special function data, and "0" to use as the general port.

I/O pins of the timer 4 can select either P14 or PD2 by setting of the timer I/O pin switching control register (TMSEL). When TM4SEL flag of the timer I/O pin switching control register (TMSEL) is 0, P14 is selected and 1, PD2 is selected.

PD3 is used as I/O pin of the timer 5, as well. The output mode can be selected by bp3 of the port D output mode register (PDOMD) by each bit. The port D output mode register (PDOMD) is set to "1" to output the special function data, and "0" to use as the general port.

I/O pins of the timer 5 can select either P15 or PD3 by setting of the timer I/O pin switching control register (TMSEL). When TM5SEL flag of the timer I/O pin switching control register (TMSEL) is 0, P15 is selected and 1, PD3 is selected.

PD4 is used as I/O pin of the timer 7, as well. The output mode can be selected by bp4 of the port D output mode register (PDOMD) by each bit. The port D output mode register (PDOMD) is set to "1" to output the special function data, and "0" to use as the general port.

I/O pins of the timer 7 can select either P16 or PD4 by setting of the the timer I/O pin switching control register (TMSEL). When TM7SEL flag of the timer I/O pin switching control register (TMSEL) is 0, P16 is selected and 1, PD4 is selected.

PD5 is used as buzzer output pin, as well. When bp7 of the oscillation stabilization wait control register (DLYCTR) is set to "1" , the buzzer output is enabled.

PD6 is uses as output pin of the system clock at the processor mode or the memory extension mode.These modes are set to the output mode automatically.

4.13.2 Registers

The following Table shows registers that control the Port D

Table:4.13.1 Port D control register

Registers	Address	R/W	Function	Page
PDOUT	0x03F1D	R/W	Port D Output Register	IV-107
PDIN	0x03F2D	R	Port D Input Register	IV-108
PDDIR	0x03F3D	R/W	Port D Direction Control Register	IV-108
PDPLU	0x03F4D	R/W	Port D Pull-up Resistor Control Register	IV-109
PDOMD	0x03F1B	R/W	Port D Output Mode Register	IV-109

R/W:Readable/Writable

■ Port D Output Register(PDOUT:0x03F1D)

bp	7	6	5	4	3	2	1	0
Flag	PDOUT7	PDOUT6	PDOUT5	PDOUT4	PDOUT3	PDOUT2	PDOUT1	PDOUT0
At reset	x	x	x	x	x	x	x	x
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bp	Flag	Description
7 6 5 4 3 2 1 0	PDOUT7 PDOUT6 PDOUT5 PDOUT4 PDOUT3 PDOUT2 PDOUT1 PDOUT0	Output data 0:Output L(VSS level) 1:Output H(VDD level)

■ Port D Input Register(PDIN:0x03F2D)

bp	7	6	5	4	3	2	1	0
Flag	PDIN7	PDIN6	PDIN5	PDIN4	PDIN3	PDIN2	PDIN1	PDIN0
At reset	x	x	x	x	x	x	x	x
Access	R	R	R	R	R	R	R	R

bp	Flag	Description
7 6 5 4 3 2 1 0	PDIN7 PDIN6 PDIN5 PDIN4 PDIN3 PDIN2 PDIN1 PDIN0	Input data 0:Pin is L(VSS level) 1:Pin is H(VDD level)

■ Port D Direction Control Register(PDDIR:0x03F3D)

bp	7	6	5	4	3	2	1	0
Flag	PDDIR7	PDDIR6	PDDIR5	PDDIR4	PDDIR3	PDDIR2	PDDIR1	PDDIR0
At reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bp	Flag	Description
7 6 5 4 3 2 1 0	PDDIR7 PDDIR6 PDDIR5 PDDIR4 PDDIR3 PDDIR2 PDDIR1 PDDIR0	I/O mode selection 0:Input mode 1:Output mode

■ Port D Pull-up Resistor Control Register(PDPLU:0x03F4D)

bp	7	6	5	4	3	2	1	0
Flag	PDPLU7	PDPLU6	PDPLU5	PDPLU4	PDPLU3	PDPLU2	PDPLU1	PDPLU0
At reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bp	Flag	Description
7 6 5 4 3 2 1 0	PDPLU7 PDPLU6 PDPLU5 PDPLU4 PDPLU3 PDPLU2 PDPLU1 PDPLU0	Pull-up resistor selection 0:Not added 1:Added

■ Port D Output Mode Register(PDOMD:0x03F1B)

bp	7	6	5	4	3	2	1	0
Flag	-	-	-	PDOMD4	PDOMD3	PDOMD2	-	
At reset	-	-	-	0	0	0	-	-
Access	-	-	-	R/W	R/W	R/W	-	-

bp	Flag	Description
7	-	-
6	-	-
5	-	-
4	PDOMD4	I/O port, TM7IO selection 0:I/O port 1:TM7IO
3	PDOMD3	I/O port, TM5IO selection 0:I/O port 1:TM5IO
2	PDOMD2	I/O port, TM4IO selection 0:I/O port 1:TM4IO
1	-	-
0	-	-

4.13.3 Block Diagram

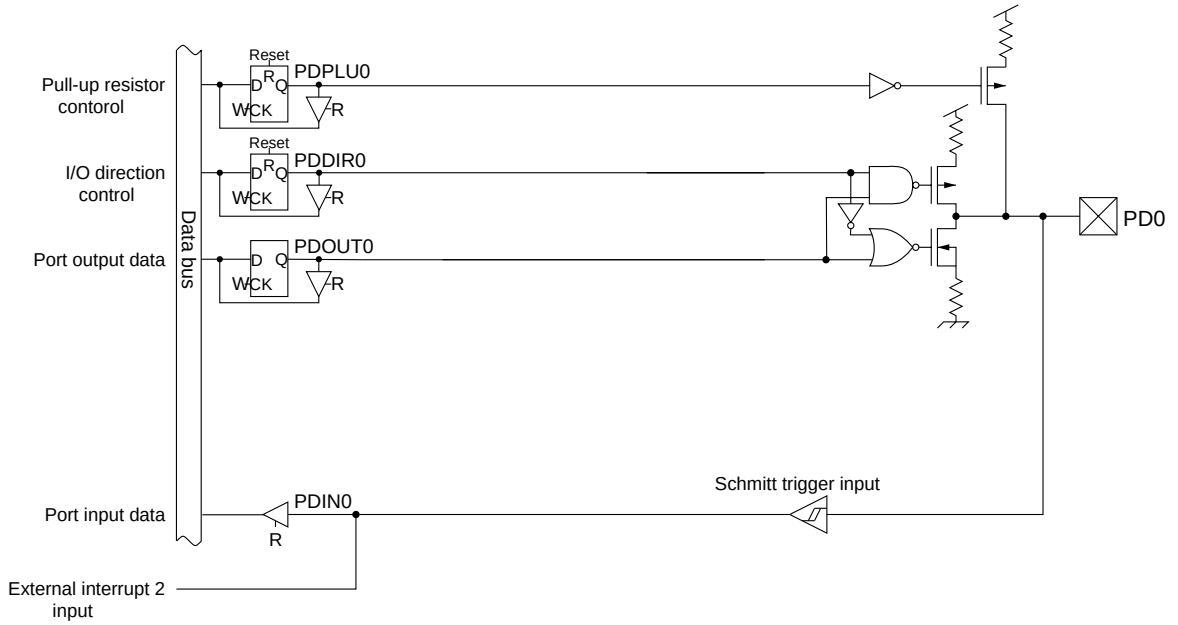


Figure:4.13.1 PD0 Block Diagram

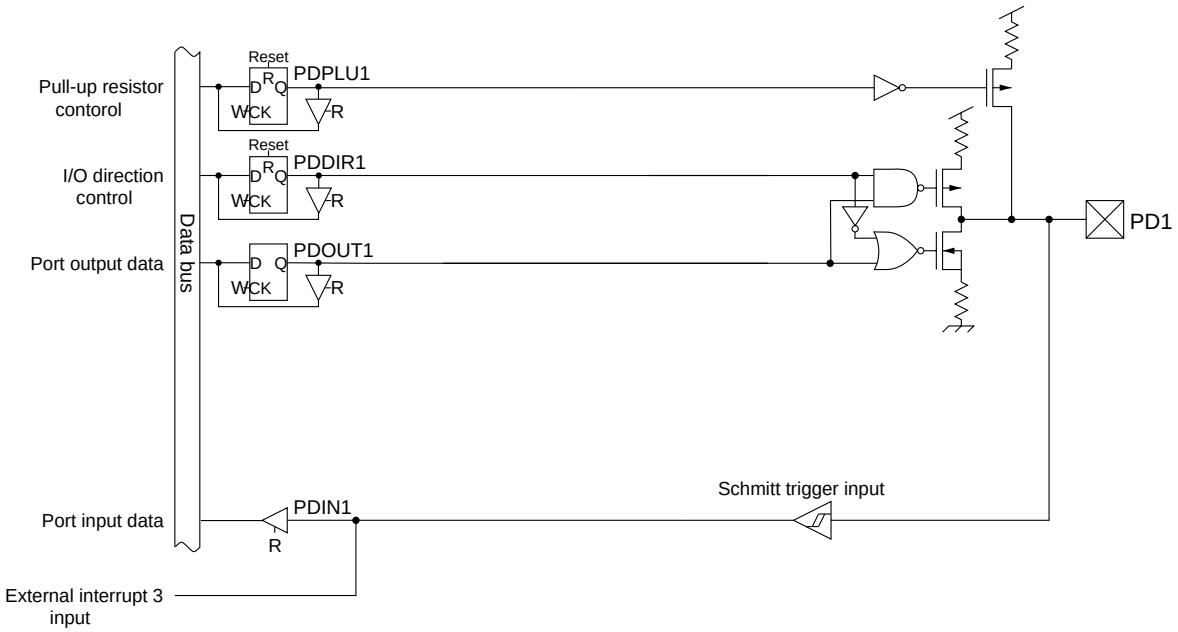


Figure:4.13.2 PD1 Block Diagram

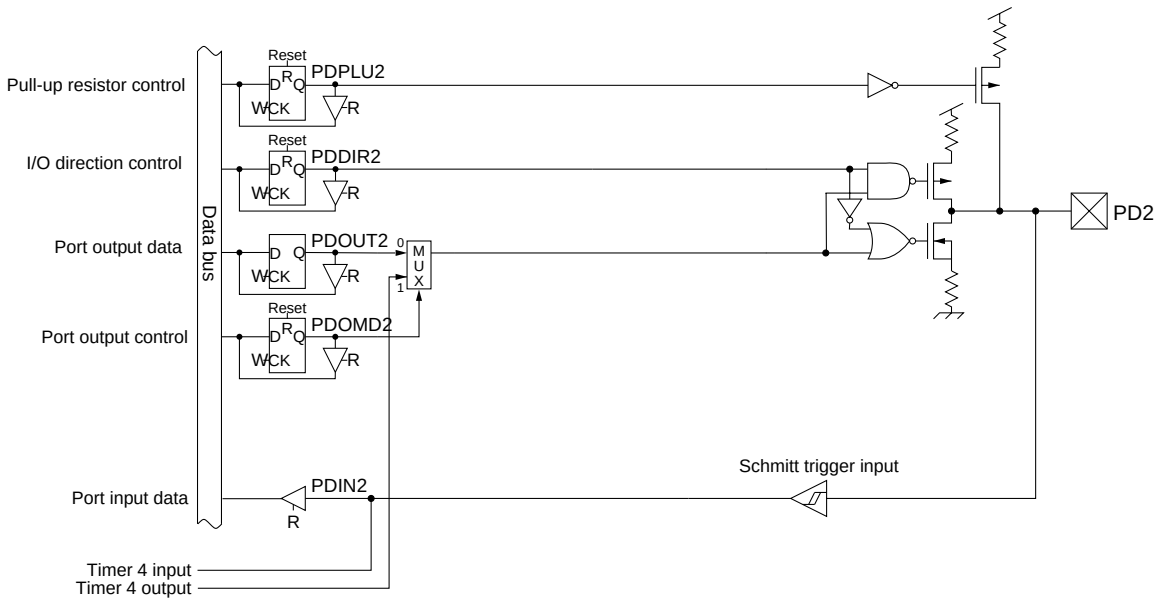


Figure:4.13.3 PD2 Block Diagram

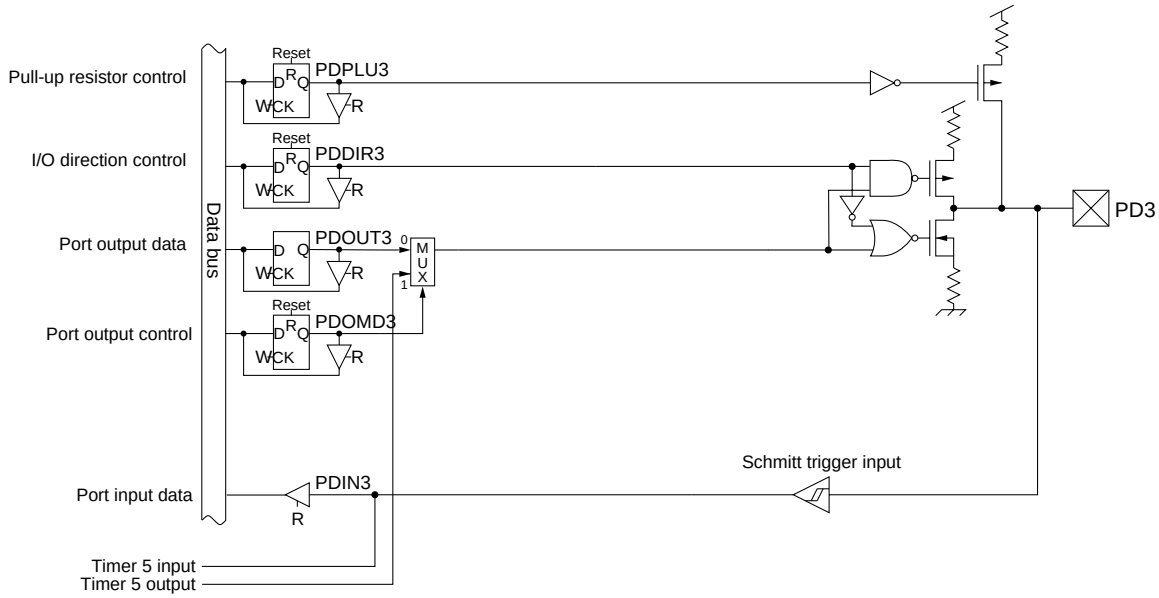


Figure:4.13.4 PD3 Block Diagram

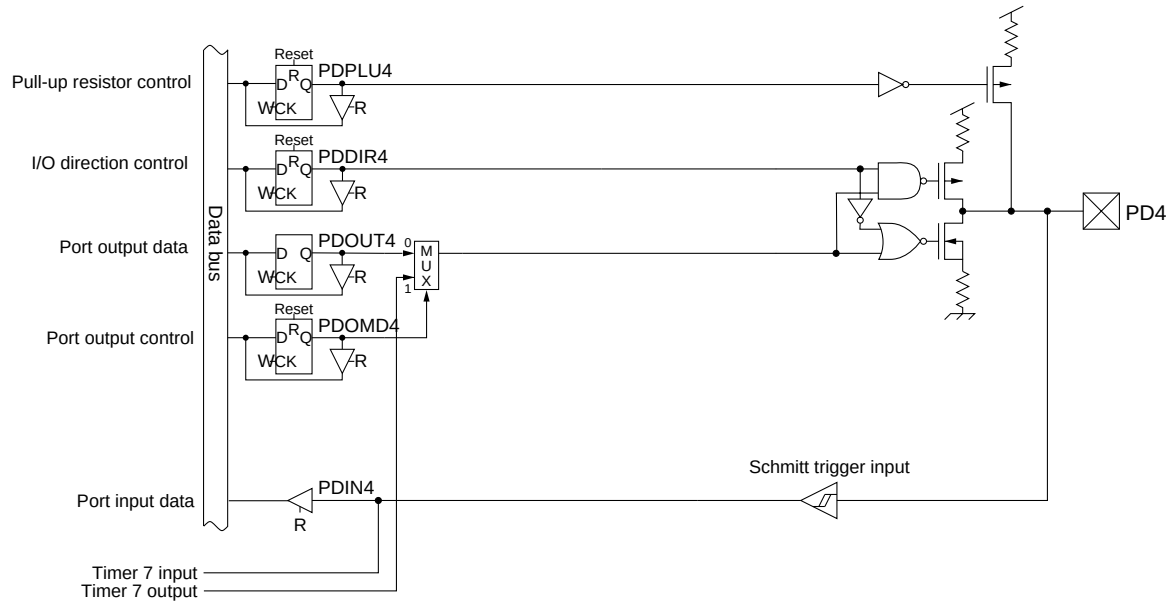


Figure:4.13.5 PD4 Block Diagram

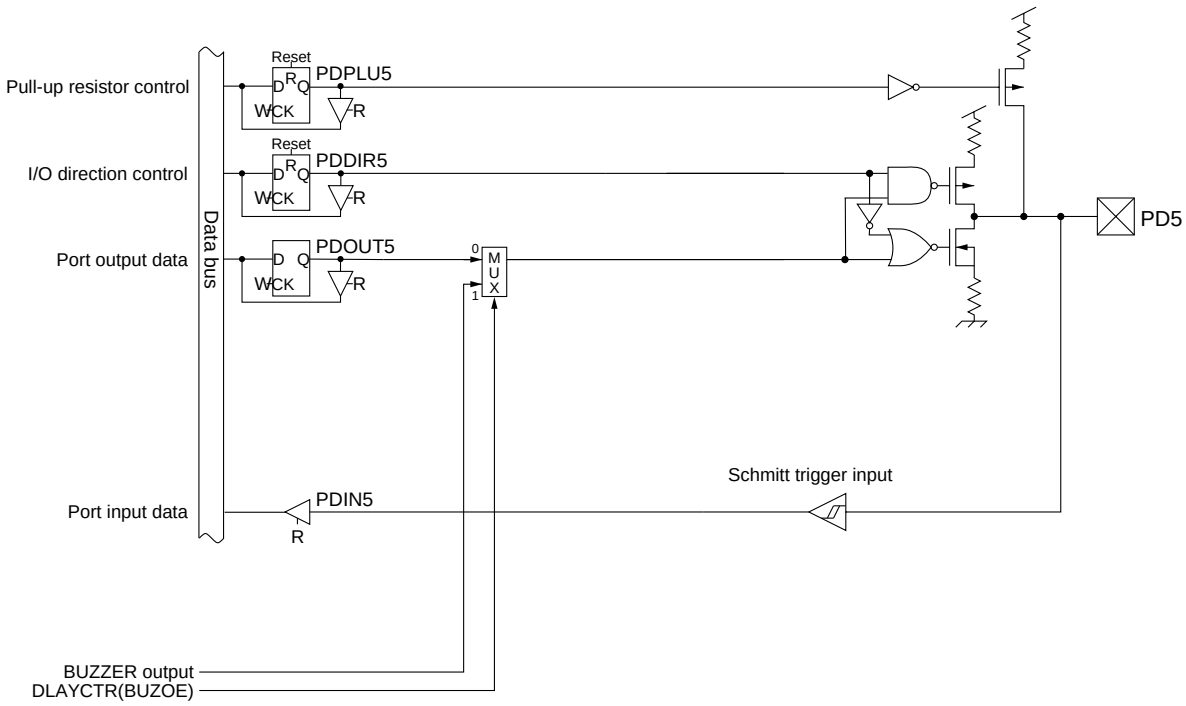


Figure:4.13.6 PD5 Block Diagram

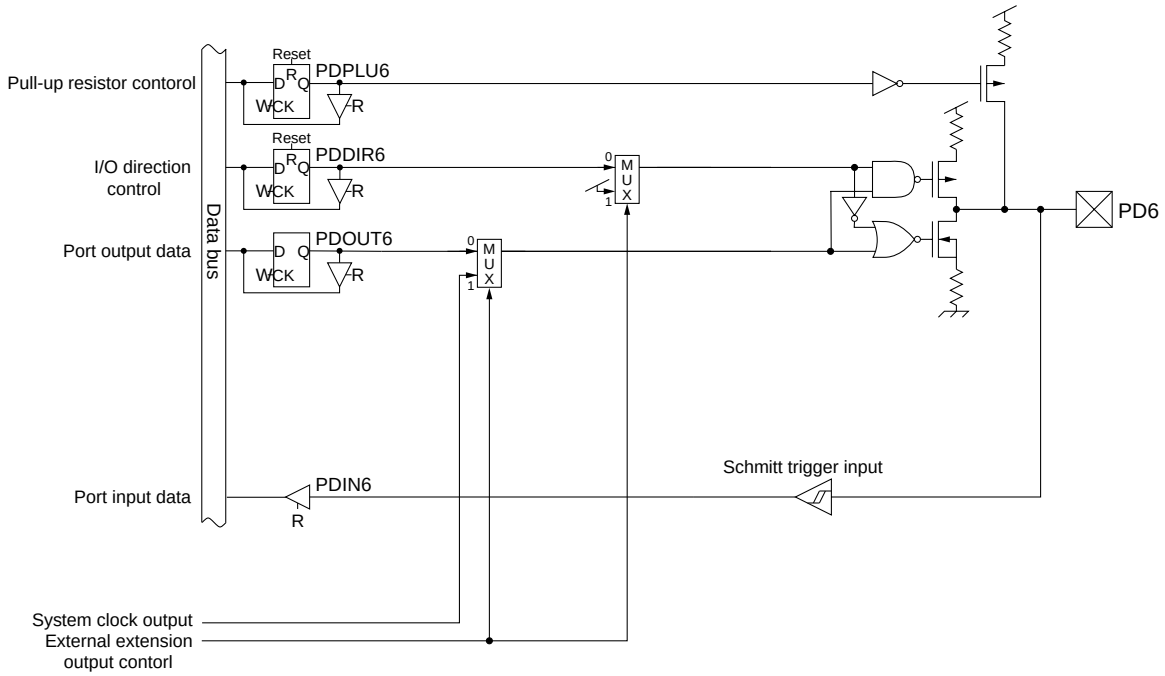


Figure:4.13.7 PD6 Block Diagram

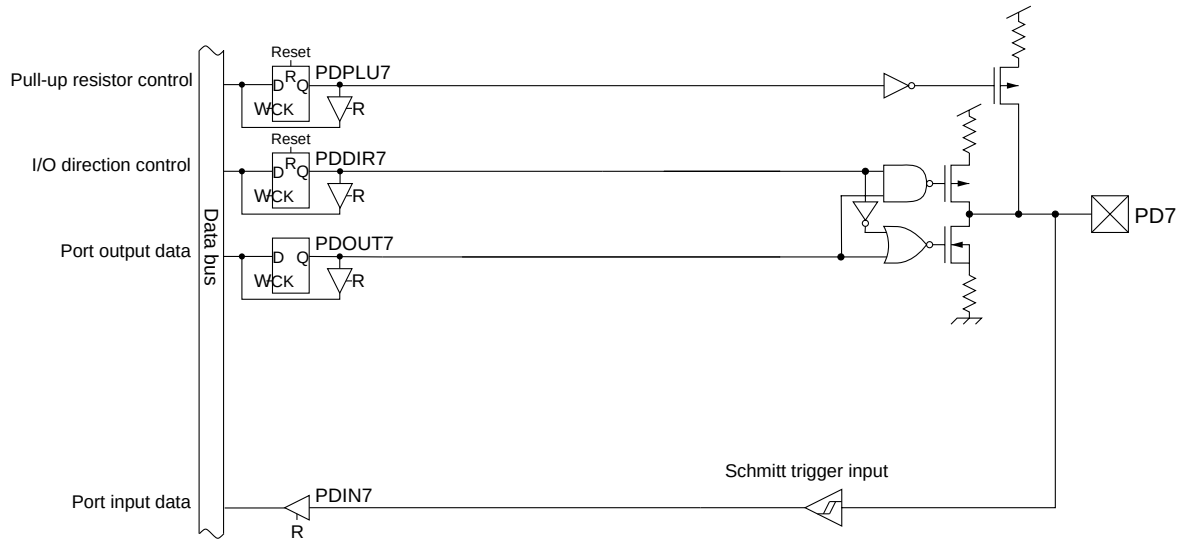


Figure:4.13.8 PD7 Block Diagram

4.14 Real Time Output Control

P10, P12, P14 have the real time output function that can switch pin output at the falling edge event of the external interrupt 0 pin (P20/IRQ0).
The real time control is the function that can change the timer output signal (PWM output, timer pulse output, remote control career output) synchronized with the external event without setting the program. Switchable output values at the event generation are “0”, “1”, “Hi-impedance (Hi-z)”.

4.14.1 Registers

Table:4.14.1 shows the real time output control registers of port 1.

Table:4.14.1 Real Time Outpt Control Registers

	Register	Address	R/W	Function	Page
Port 1	P1OUT	0x03F11	R/W	Port 1 output register	IV-15
	P1DIR	0x03F31	R/W	Port 1 direction control register	IV-16
	P1PLU	0x03F41	R/W	Port 1 pull-up resistor control register	IV-17
	P1OMD	0x03F2B	R/W	Port 1 output mode register	IV-18
	P1CNT0	0x03F7E	R/W	Port 1 real time output control register	IV-19

4.14.2 Operation

■ Real Time Output Pin Setup

The real time output pin setup should be done at the port 1 output control register (P1CNTO). Selectable pins are P10, P12, P14 and each of them can be specified by each bit. The output mode should be selected at the port 1 direction control register (P1DIR).
The pin output that is switched at the falling edge event of the external interrupt 0 pin (P20/IRQ0) is “0”, “1”, “Hi-impedance”. Port is input mode at the hi-impedance.

The real time control is the function that changes the timer output signal (PWM output, timer pulse output remote control career output) synchronized with the external event. It is also available to normal port output.
When I/O port (real time control disabled) is selected at the port 1 output control register (P1CNT0), if switching event is generated, the value is not be changed. Set this mode when it is used as the general port.

■ Real Time Output Control Operation

After the setup of the port 1 output control register (P1CNT0), selected function at the port 1 output mode register (P1OMD) is output to the pin until the falling edge is generated at the external interrupt 0 pin (P20/IRQ0).
When the falling edge is generated, pin output is switched to the set value. The falling edge event is taken in the edge event hold function that is shown below and the setup value of the port 1 output control register (P1CNT0) is held until that information is cleared.

■ Real Time Output Release (Clearance of edge event hold function)

After the event generation, when the write operation is done to the port 1 output register (P1OUT), the information of the edge event hold function is cleared and all output pins are reset to the output data before the event generation. The event is generated again, it is switched to the setup value of the port 1 output control register (P1CNT0). When the real time control is canceled, set the port 1 output control register (P1CNT0) to I/O port (real time control disabled).

In spite of the setup at the external interrupt 0 control register (IRQ0ICR), valid edge of IRQ0 is only the falling edge.

When the real time output control function is use the port 1 output register (P1OUT) in advance and clear the information of the edge event hold function.

■ Timing of Real Time Output Control

P1CNT0 setvalue:”0” (Low) output

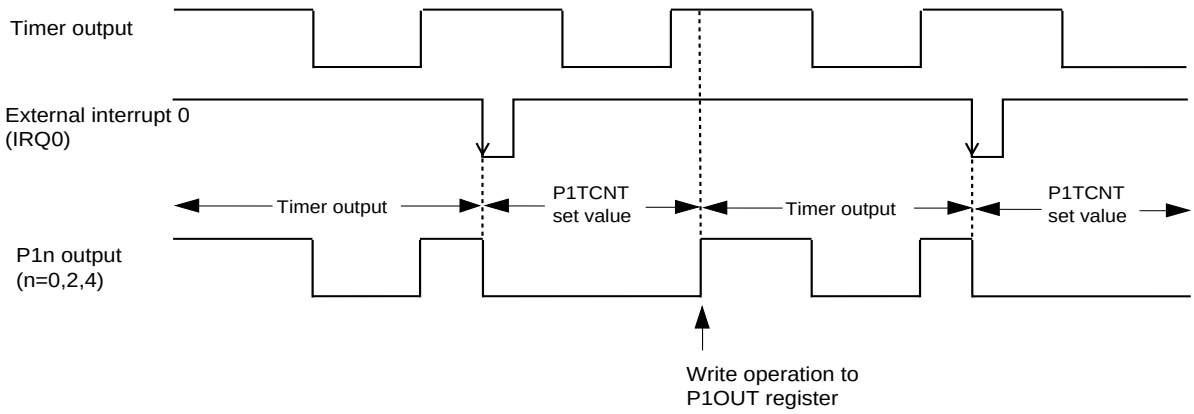


Figure:4.14.1 Timing of Real Time Output Control

4.15 Synchronous Output

Port 7 has the synchronous output function that outputs the arbitrary set data to pins, in synchronization with the generation of the specified event, without setting program. Synchronous event is selected from the external interrupt 2 (P22/IRQ2), timer 1 interrupt, timer 2 interrupt or timer 7 interrupt signal.

4.15.1 Registers

Table:4.15.1 shows the synchronous output control registers of the port 4.

Table:4.15.1 Synchronous Output Control Registers

	Register	Address	R/W	Function	Page
Port 7	P7OUT	0x03F17	R/W	Port 7 output register	IV-67
	P7DIR	0x03F37	R/W	Port 7 direction control register	IV-68
	P7PLU	0x03F47	R/W	Port 7 pull-up/pull-down resistor control register	IV-70
	P7SYO	0x03F1F	R/W	Port 7 synchronous output control register	IV-69
	P7SEV	0x03F2F	R/W	Port 7 synchronous output event selection register	IV-70

4.15.2 Operation

■ Synchronous Output Setup

The synchronous output control register (P7SYO) selects the synchronous output pin of the port 7, in each bit. The synchronous output event is selected by the pin control register (P7SEV).

When the external interrupt 2 (IRQ2) is selected, it is synchronized with the falling edge in spite of the edge specification of IRQ2ICR.

■ Synchronous Output Operation

When the synchronous output control register (P7SYO) is set to disable the synchronous output (I/O port), the port 7 is functioned as a general port. When the port 7 is set to disable the synchronous output, the same value to the port 7 output register (P7OUT) is always loaded to the synchronous output value stored register.

After the output mode is selected by the port 7 direction control register (P7DIR), if the synchronous output is enabled by the synchronous output control register (P7SYO), the value of the synchronous output value stored register is output from pins. If the synchronous output event that is set by the pin control register (P7SEV) is never generated, the synchronous output value stored register holds the same value when the synchronous output event is enabled.

Before the synchronous output is enabled by the synchronous output control register (P7SYO), set the initial value of the synchronous output to the port 7 output register (P7OUT), in advance.

■ Port 7 Synchronous Output (External interrupt 2 IRQ2)

The synchronous output timing when the synchronous output event is set to the external interrupt 2, is shown below. The latched data on port 7 is output in synchronization with the falling edge of the IRQ2.

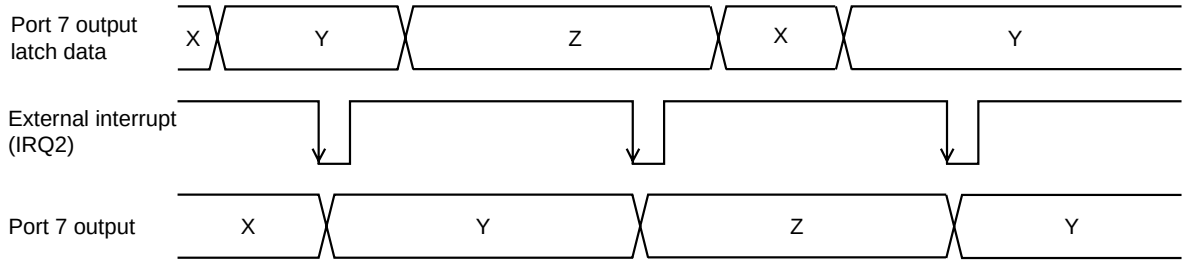


Figure:4.15.1 Synchronous Output Timing by Event Generation (IRQ2)

■ Port 7 Synchronous Output (Timer 1, Timer 2, Timer 7)

The timer interrupt flag TMnIRQ is generated when the set values of binary counter and compare register are matched. The latched data on port 7 is output from the port 7 in synchronization with the rising edge of the TMnIRQ.

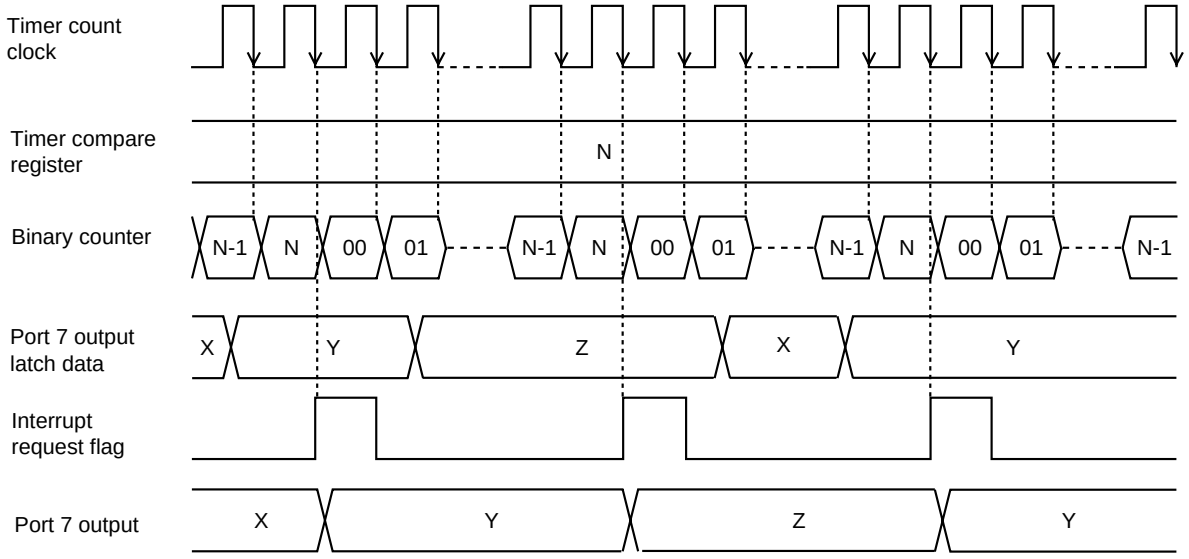


Figure:4.15.2 Synchronous Output Timing by Event Generation (Timer 1, Timer 2, Timer 7)

4.16 Input Rejection Function

4.16.1 Registers

Table:4.16.1 shows the input rejection control registers.

Table:4.16.1 Input Rejection Control Registers

	Register	Address	R/W	Function	Page
Input rejection	I0CTR	0x03F6E	R/W	Input rejection control register	IV-110

4.16.2 Operation

■ Input Rejection Control Register (IOCTR:0x03F6E)

bp	7	6	5	4	3	2	1	0
Flag	I0EN	-	-	-	-	-	-	Reserved
At reset	0	-	-	-	-	-	-	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Input data of 5V I/O port (Port 4, 8, 9, A, and D) is not read during input rejection by input rejection control register.

bp	Flag	Description
7	I0EN	Input rejection control 0 : normal input 1 : input rejection
6-1	-	-
0	Reserved	set always ”0”

Chapter 5 8-bit Timers

5

5.1 Overview

This LSI contains two general purpose 8-bit timers (Timers 0 and 1) and four 8-bit timers (Timers 2, 3, 4 and 5) combined baud rate timers. Timers 0 and 1 or Timers 2 and 3 or Timers 4 and 5 can be used as 16-bit timer with cascade connection. In a cascade connection, Timers 0, 2 and 4 form the "timer 0", or the lower 8 bits of 16-bit counter, and Timers 1, 3 and 5 form the "timer 1", or the upper 8 bits.

8-bit timer contains two prescalers which can use at the same time. Each prescaler counts fosc, fs as the base clock. Configurations of hard ware are shown below.

Prescaler 0 (fosc base) 7 bits Prescaler

Prescaler 1 (fs base) 3 bits Prescaler

Prescaler 0 outputs fosc/4, fosc/16, fosc/32, fosc/64, fosc/128.

Prescaler 1 outputs fs/2, fs/4, fs/8.

Fosc or fs can be selected as the clock source for each timer by using the prescaler.

5.1.1 Functions

Table:5.1.1 shows functions that can be used with each timer.

Table:5.1.1 Timer Functions

	Timer 0 (8-bit)	Timer 1 (8-bit)	Timer 2 (8-bit)	Timer 3 (8-bit)	Timer 4 (8-bit)	Timer 5 (8-bit)
Interrupt source	TM0IRQ	TM1IRQ	TM2IRQ	TM3IRQ	TM4IRQ	TM5IRQ
Timer operation	O	O	O	O	O	O
Event count	TM0IO input (P10)	TM1IO input (P11)	TM2IO input (P12)	TM3IO input (P13)	TM4IO input (P14)	TM5IO input (P15)
Timer pulse output	TM0IO output (P10)	TM1IO output (P11)	TM2IO output (P12)	TM3IO output (P13)	TM4IO output (P14, PD2)	TM5IO output (P15, PD3)
PWM output	TM0IO output pin (P10)	-	TM2IO output pin (P12)	-	TM4IO output pin (P14, PD2)	-
Synchronous output	-	Port 7	Port 7	-	-	-
Serial transfer clock output	-	-	-	-	-	-
Pulse width measurement	External interrupt 2 (P22/IRQ2A) (PD0/IRQ2B)	-	External interrupt 3 (P23/IRQ3A) (PD1/IRQ3B)	-	External interrupt 4 (P24/IRQ4)	-
Cascade connection	O		O		O	
Clock source	fosc fosc/4 fosc/16 fosc/32 fosc/64 fs/2 fs/4 fx TM0IO input synchronous fx synchronous TM0IO input	fosc fosc/4 fosc/16 fosc/64 fosc/128 fs/2 fs/8 fx TM1IO input synchronous fx synchronous TM1IO input	fosc fosc/4 fosc/16 fosc/32 fosc/64 fs/2 fs/4 fx TM2IO input synchronous fx synchronous TM2IO input	fosc fosc/4 fosc/16 fosc/64 fosc/128 fs/2 fs/8 fx TM3IO input synchronous fx synchronous TM3IO input	fosc fosc/4 fosc/16 fosc/32 fosc/64 fs/2 fs/4 fx TM4IO input synchronous fx synchronous TM4IO input	fosc fosc/4 fosc/16 fosc/64 fosc/128 fs/2 fs/8 fx TM5IO input synchronous fx synchronous TM5IO input
fosc:Machine clock (High frequency oscillation) fx:Machine clock (Low frequency oscillation) fs:System clock [Chapter 2. 2.5 Clock Switching]						

5.1.2 Block Diagram

■ Prescaler Block Diagram

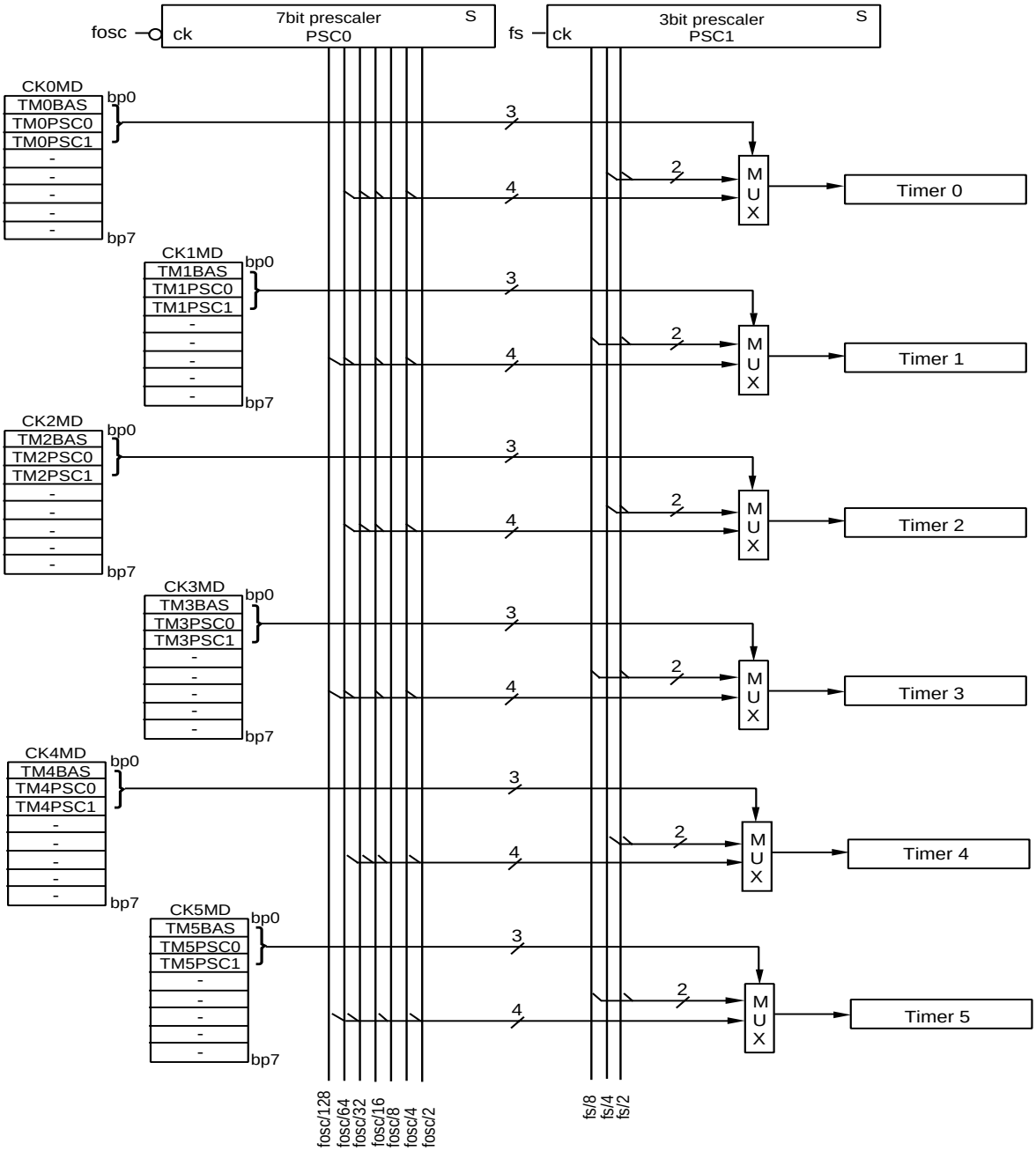


Figure:5.1.1 Prescaler Block Diagram

■ Timers 0 and 1 Block Diagram

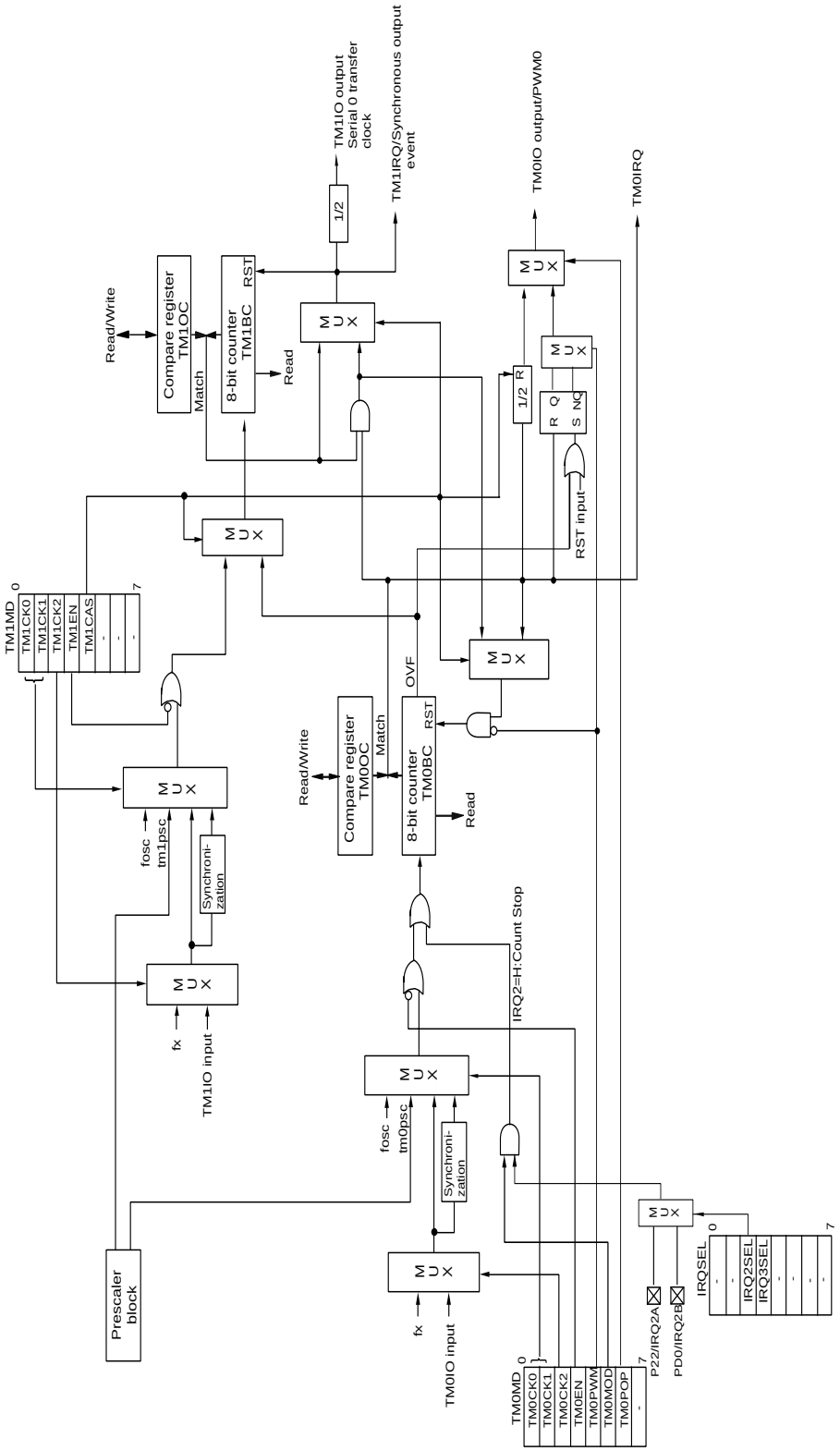


Figure:5.1.2 Timers 0 and 1 Block Diagram

■ Timers 2 and 3 Block Diagram

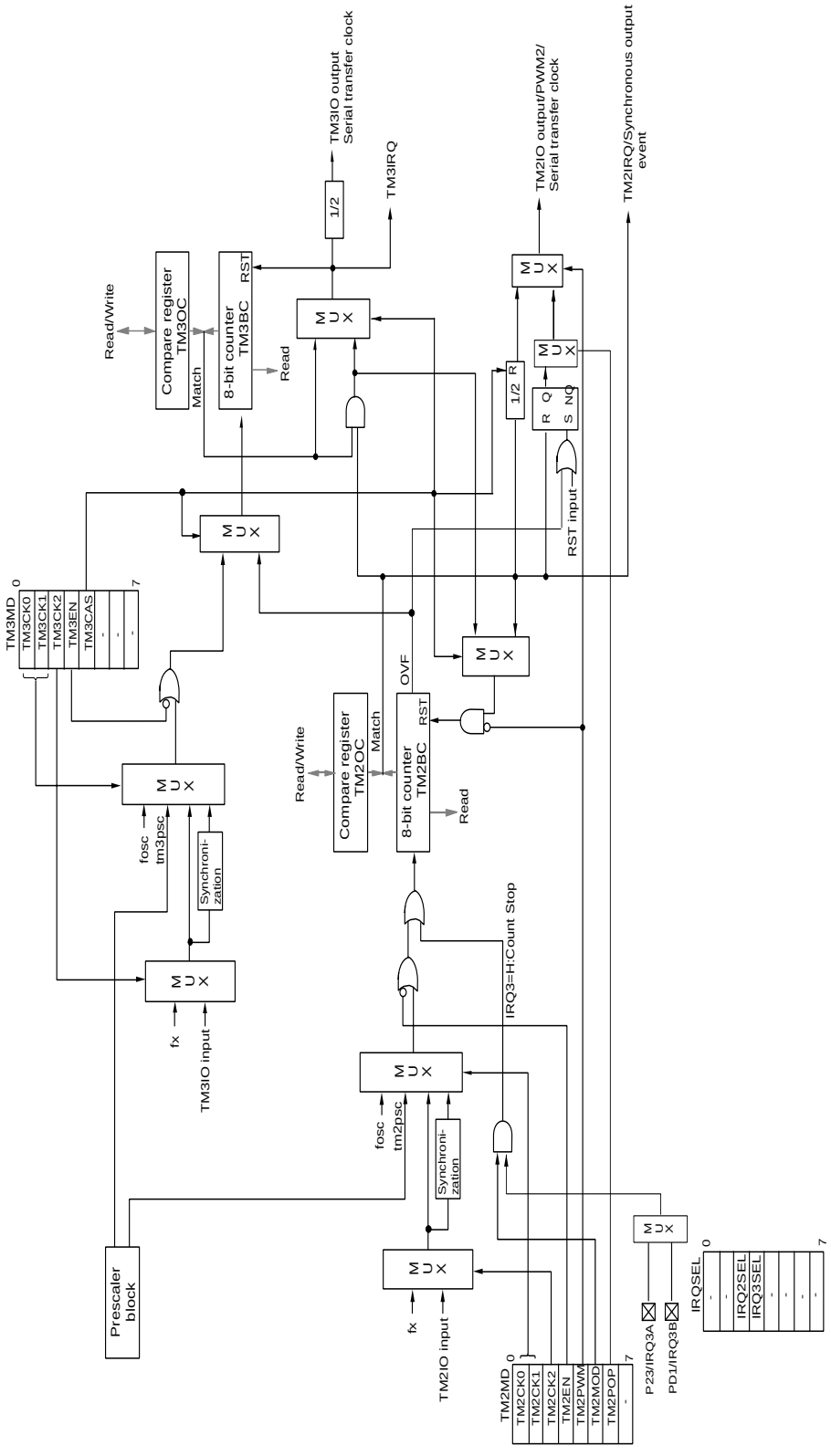


Figure:5.1.3 Timers 2 and 3 Block Diagram

■ Timers 4 and 5 Block Diagram

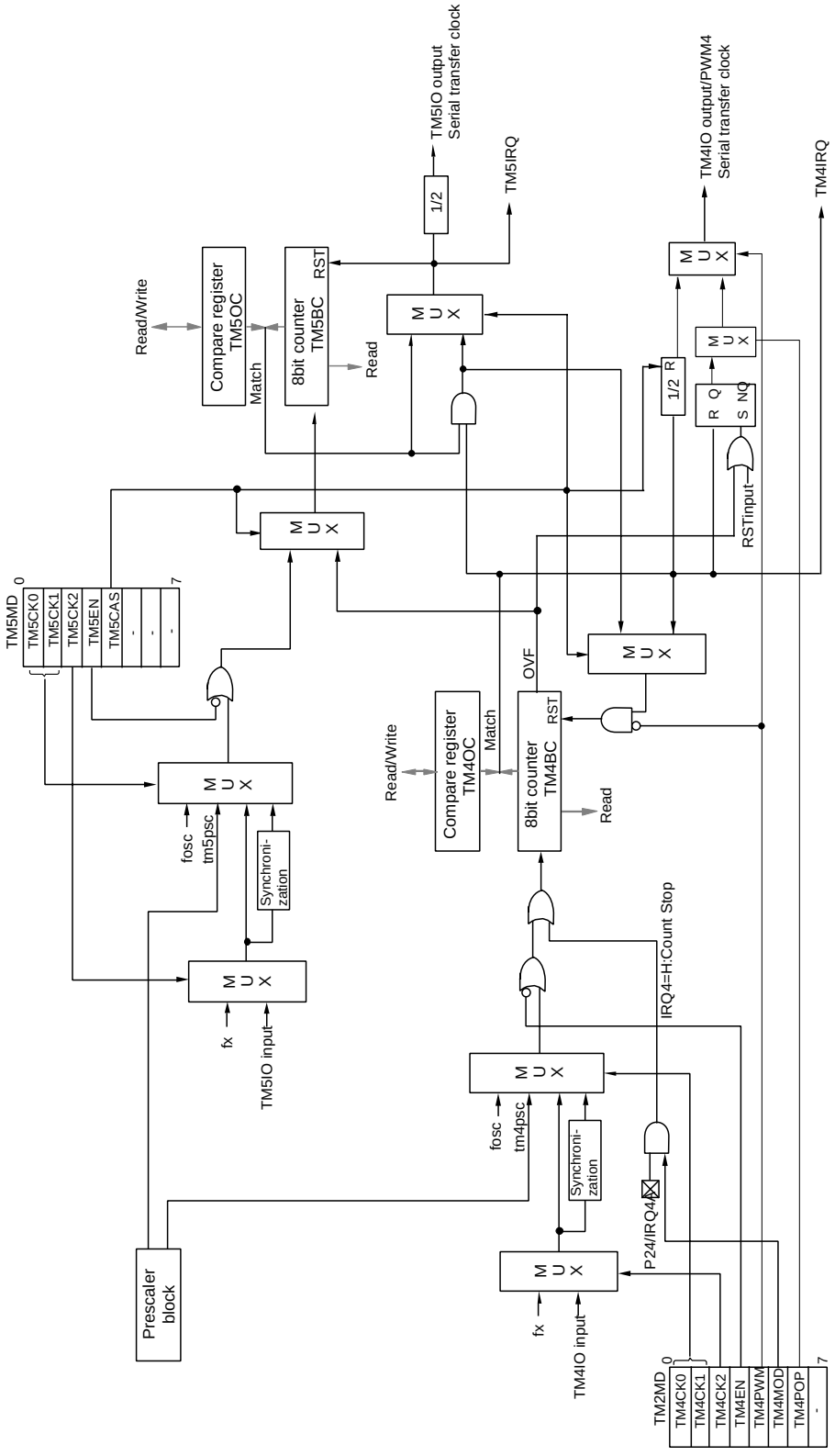


Figure:5.1.4 Timers 4 and 5 Block Diagram

5.2 Control Registers

Timers 0 to 5 consist of the binary counter (TMnBC) and the compare register (TMnOC). And they are controlled by the mode register (TMnMD).

When the prescaler output is selected as the count clock source of timers 0 to 5, they should be controlled by the prescaler selection register (CKnMD).

5.2.1 Registers

Table:5.2.1 shows registers that control timers 0 to 5.

Table:5.2.1 8-bit Timer Control Registers

	Register	Address	R/W	Function	Page
Timer 0	TM0BC	0x03F50	R	Timer 0 binary counter	V-15
	TM0OC	0x03F52	R/W	Timer 0 compare register	V-14
	TM0MD	0x03F54	R/W	Timer 0 mode register	V-17
	CK0MD	0x03F56	R/W	Timer 0 prescaler selection register	V-10
	TM0ICR	0x03FE8	R/W	Timer 0 interrupt control register	III-26
	P1OMD	0x03F2B	R/W	Port 1 output mode register	IV-13
	P1DIR	0x03F31	R/W	Port 1 direction control register	IV-13
	IRQSEL	0x03F4E	R/W	External interrupt pin switching control register	IV-13
Timer 1	TM1BC	0x03F51	R	Timer 1 binary counter	V-15
	TM1OC	0x03F53	R/W	Timer 1 compare register	V-14
	TM1MD	0x03F55	R/W	Timer 1 mode register	V-18
	CK1MD	0x03F57	R/W	Timer 1 prescaler selection register	V-11
	TM1ICR	0x03FE9	R/W	Timer 1 interrupt control register	III-27
	P1OMD	0x03F2B	R/W	Port 1 output mode register	IV-13
	P1DIR	0x03F31	R/W	Port 1 direction control register	IV-13
Timer 2	TM2BC	0x03F58	R	Timer 2 binary counter	V-16
	TM2OC	0x03F5A	R/W	Timer 2 compare register	V-14
	TM2MD	0x03F5C	R/W	Timer 2 mode register	V-19
	CK2MD	0x03F5E	R/W	Timer 2 prescaler selection register	V-11
	TM2ICR	0x03FEA	R/W	Timer 2 interrupt control register	III-28
	P1OMD	0x03F2B	R/W	Port 1 output mode register	IV-13
	P1DIR	0x03F31	R/W	Port 1 direction control register	IV-13
	IRQSEL	0x03F4E	R/W	External interrupt pin switching control register	III-53

	Register	Address	R/W	Function	Page
Timer 3	TM3BC	0x03F59	R	Timer 3 binary counter	V-16
	TM3OC	0x03F5B	R/W	Timer 3 compare register	V-14
	TM3MD	0x03F5D	R/W	Timer 3 mode register	V-20
	CK3MD	0x03F5F	R/W	Timer 3 prescaler selection register	V-12
	TM3ICR	0x03FEB	R/W	Timer 3 interrupt control register	III-29
	P1OMD	0x03F2B	R/W	Port 1 output mode register	IV-18
	P1DIR	0x03F31	R/W	Port 1 direction control register	IV-16
Timer 4	TM4BC	0x03F60	R	Timer 4 binary counter	V-16
	TM4OC	0x03F62	R/W	Timer 4 compare register	V-15
	TM4MD	0x03F64	R/W	Timer 4 mode register	V-21
	CK4MD	0x03F66	R/W	Timer 4 prescaler selection register	V-12
	TM4ICR	0x03FEC	R/W	Timer 4 interrupt control register	III-30
	P1OMD	0x03F2B	R/W	Port 1 output mode register	IV-18
	P1DIR	0x03F31	R/W	Port 1 direction control register	IV-16
	PDOMD	0x03F1B	R/W	Port D output control register	IV-107
	PDDIR	0x03F3D	R/W	Port D direction control register	IV-108
	TMSEL	0x03F3F	R/W	Timer I/O pin switching register	V-23
Timer 5	TM5BC	0x03F61	R	Timer 5 binary counter	V-16
	TM5OC	0x03F63	R/W	Timer 5 compare register	V-15
	TM5MD	0x03F65	R/W	Timer 5 mode register	V-22
	CK5MD	0x03F67	R/W	Timer 5 prescaler selection register	V-13
	TM5ICR	0x03FED	R/W	Timer 5 interrupt control register	III-31
	P1OMD	0x03F2B	R/W	Port 1 output mode register	IV-49
	P1DIR	0x03F31	R/W	Port 1 direction control register	IV-50
	PDOMD	0x03F1B	R/W	Port D output control register	IV-107
	PDDIR	0x03F3D	R/W	Port D direction control register	IV-108
	TMSEL	0x03F3F	R/W	Timer I/O pin switching register	V-23

R/W:Readable / Writable

R:Readable only

5.2.2 Timer Prescaler Registers

Timer prescaler selection register selects the count clock for 8-bit timer.

The register which selects prescaler output is consisted by the timer prescaler selection register (CKnMD).

■ Timer 0 prescaler selection register (CK0MD:0x03F56)

bp	7	6	5	4	3	2	1	0
Flag	-	-	-	-	-	TM0PSC1	TM0PSC0	TM0BAS
At reset	-	-	-	-	-	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bp	Flag	Description
7-3	-	-
2-0	TM0PSC1 TM0PSC0 TM0BAS	Select the clock source 000:fosc/4 010:fosc/16 100:fosc/32 110:fosc/64 X01:fs/2 X11:fs/4

■ Timer 1 prescaler selection register (CK1MD:0x03F57)

bp	7	6	5	4	3	2	1	0
Flag	-	-	-	-	-	TM1PSC1	TM1PSC0	TM1BAS
At reset	-	-	-	-	-	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bp	Flag	Description
7-3	-	-
2-0	TM1PSC1 TM1PSC0 TM1BAS	Select the clock source 000:fosc/4 010:fosc/16 100:fosc/64 110:fosc/128 X01:fs/2 X11:fs/8

■ Timer 2 prescaler selection register (CK2MD:0x03F5E)

bp	7	6	5	4	3	2	1	0
Flag	-	-	-	-	-	TM2PSC1	TM2PSC0	TM2BAS
At reset	-	-	-	-	-	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bp	Flag	Description
7-3	-	-
2-0	TM2PSC1 TM2PSC0 TM2BAS	Select the clock source 000:fosc/4 010:fosc/16 100:fosc/32 110:fosc/64 X01:fs/2 X11:fs/4

■ Timer 3 prescaler selection register (CK3MD:0x03F5F)

bp	7	6	5	4	3	2	1	0
Flag	-	-	-	-	-	TM3PSC1	TM3PSC0	TM3BAS
At reset	-	-	-	-	-	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bp	Flag	Description
7-3	-	-
2-0	TM3PSC1 TM3PSC0 TM3BAS	Select the clock source 000:fosc/4 010:fosc/16 100:fosc/64 110:fosc/128 X01:fs/2 X11:fs/8

■ Timer 4 prescaler selection register (CK4MD:0x03F66)

bp	7	6	5	4	3	2	1	0
Flag	-	-	-	-	-	TM4PSC1	TM4PSC0	TM4BAS
At reset	-	-	-	-	-	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bp	Flag	Description
7-3	-	-
2-0	TM4PSC1 TM4PSC0 TM4BAS	Select the clock source 000:fosc/4 010:fosc/16 100:fosc/32 110:fosc/64 X01:fs/2 X11:fs/4

■ Timer 5 prescaler selection register (CK5MD:0x03F67)

bp	7	6	5	4	3	2	1	0
Flag	-	-	-	-	-	TM5PSC1	TM5PSC0	TM5BAS
At reset	-	-	-	-	-	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bp	Flag	Description
7-3	-	-
2-0	TM5PSC1 TM5PSC0 TM5BAS	Select the clock source 000:fosc/4 010:fosc/16 100:fosc/64 110:fosc/128 X01:fs/2 X11:fs/8

5.2.3 Programmable Timer Registers

Each of timers 0 to 5 has 8-bit programmable timer registers.

Programmable timer register consists of compare register and binary counter.

Compare register is 8-bit register which stores the value to be compared to binary counter are stocked.

■ Timer 0 Compare Register (TM0OC:0x03F52)

bp	7	6	5	4	3	2	1	0
Flag	TM0OC7	TM0OC6	TM0OC5	TM0OC4	TM0OC3	TM0OC2	TM0OC1	TM0OC0
At reset	X	X	X	X	X	X	X	X
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

■ Timer 1 Compare Register (TM1OC:0x03F53)

bp	7	6	5	4	3	2	1	0
Flag	TM1OC7	TM1OC6	TM1OC5	TM1OC4	T1OC3	TM1OC2	TM1OC1	TM1OC0
At reset	X	X	X	X	X	X	X	X
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

■ Timer 2 Compare Register (TM2OC:0x03F5A)

bp	7	6	5	4	3	2	1	0
Flag	TM2OC7	TM2OC6	TM2OC5	TM2OC4	T2OC3	TM2OC2	TM2OC1	TM2OC0
At reset	X	X	X	X	X	X	X	X
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

■ Timer 3 Compare Register (TM3OC:0x03F5B)

bp	7	6	5	4	3	2	1	0
Flag	TM3OC7	TM3OC6	TM3OC5	TM3OC4	T3OC3	TM3OC2	TM3OC1	TM3OC0
At reset	X	X	X	X	X	X	X	X
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

■ Timer 4 Compare Register (TM4OC:0x03F62)

bp	7	6	5	4	3	2	1	0
Flag	TM4OC7	TM4OC6	TM4OC5	TM4OC4	TM4OC3	TM4OC2	TM4OC1	TM4OC0
At reset	X	X	X	X	X	X	X	X
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

■ Timer 5 Compare Register (TM5OC:0x03F63)

bp	7	6	5	4	3	2	1	0
Flag	TM5OC7	TM5OC6	TM5OC5	TM5OC4	TM5OC3	TM5OC2	TM5OC1	TM5OC0
At reset	X	X	X	X	X	X	X	X
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Binary counter is 8-bit up counter. If any data is written to compare register the counting is stopped and binary counter is cleared to 0x00.

■ Timer 0 Binary Counter (TM0BC:0x03F50)

bp	7	6	5	4	3	2	1	0
Flag	TM0BC7	TM0BC6	TM0BC5	TM0BC4	TM0BC3	TM0BC2	TM0BC1	TM0BC0
At reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R

■ Timer 1 Binary Counter (TM1BC:0x03F51)

bp	7	6	5	4	3	2	1	0
Flag	TM1BC7	TM1BC6	TM1BC5	TM1BC4	TM1BC3	TM1BC2	TM1BC1	TM1BC0
At reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R

■ Timer 2 Binary Counter (TM2BC:0x03F58)

bp	7	6	5	4	3	2	1	0
Flag	TM2BC7	TM2BC6	TM2BC5	TM2BC4	TM2BC3	TM2BC2	TM2BC1	TM2BC0
At reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R

■ Timer 3 Binary Counter (TM3BC:0x03F59)

bp	7	6	5	4	3	2	1	0
Flag	TM3BC7	TM3BC6	TM3BC5	TM3BC4	TM3BC3	TM3BC2	TM3BC1	TM3BC0
At reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R

■ Timer 4 Binary Counter (TM4BC:0x03F60)

bp	7	6	5	4	3	2	1	0
Flag	TM4BC7	TM4BC6	TM4BC5	TM4BC4	TM4BC3	TM4BC2	TM4BC1	TM4BC0
At reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R

■ Timer 5 Binary Counter (TM5BC:0x03F61)

bp	7	6	5	4	3	2	1	0
Flag	TM5BC7	TM5BC6	TM5BC5	TM5BC4	TM5BC3	TM5BC2	TM5BC1	TM5BC0
At reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R

5.2.4 Timer Mode Registers

Timer mode register is readable/writable register that controls timers 0 to 5.

■ Timer 0 Mode Register (TM0MD:0x03F54)

bp	7	6	5	4	3	2	1	0
Flag	-	TM0POP	TM0MOD	TM0PWM	TM0EN	TM0CK2	TM0CK1	TM0CK0
At reset	-	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bp	Flag	Description
7	-	-
6	TM0POP	On PWM mode, select start compulsion of output signal 0:timer output L→H, H→L 1:timer output H→L, L→H
5	TM0MOD	Pulse width measurement control 0:Normal timer operation 1:P22/PD0 pulse width measurement
4	TM0PWM	Select timer 0 operation mode 0:Normal timer operation 1:PWM operation
3	TM0EN	Timer 0 count control 0:Halt the count 1:Operate the count
2-0	TM0CK2 TM0CK1 TM0CK0	Select the clock source X00:fosc X01:TM0PSC (Prescaler output) 010:fx 011:Synchronous fx 110:TM0IO input 111:Synchronous TM0IO output

■ Timer 1 Mode Register (TM1MD:0x03F55)

bp	7	6	5	4	3	2	1	0
Flag	-	-	-	TM1CAS	TM1EN	TM1CK2	TM1CK1	TM1CK0
At reset	-	-	-	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bp	Flag	Description
7-5	-	-
4	TM1CAS	Select timer 1 operation mode 0:Normal timer operation 1:Cascade connection
3	TM1EN	Timer 1 count control 0:Halt the count 1:Operate the count
2-0	TM1CK2 TM1CK1 TM1CK0	Select the clock source X00:fosc X01:TM1PSC (Prescaler output) 010:fx 011:Synchronous fx 110:TM1IO input 111:Synchronous TM0IO input

■ Timer 2 Mode Register (TM2MD:0x03F5C)

bp	7	6	5	4	3	2	1	0
Flag	-	TM2POP	TM2MOD	TM2PWM	TM2EN	TM2CK2	TM2CK1	TM2CK0
At reset	-	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bp	Flag	Description
7	-	-
6	TM2POP	On PWM mode, select start compulsion of output signal 0:timer output L→H, H→L 1:timer output H→L, L→H
5	TM2MOD	Pulse width measurement control 0:Normal timer operation 1:P23/PD1 pulse width measurement
4	TM2PWM	Select timer 2 operation mode 0:Normal timer operation 1:PWM operation
3	TM2EN	Timer 2 count control 0:Halt the count 1:Operate the count
2-0	TM2CK2 TM2CK1 TM2CK0	Select the clock source X00:fosc X01:TM2PSC (Prescaler output) 010:fx 011:Synchronou fx 110:TM2IO input 111:Synchronous TM2IO output

■ Timer 3 Mode Register (TM3MD:0x03F5D)

bp	7	6	5	4	3	2	1	0
Flag	-	-	-	TM3CAS	TM3EN	TM3CK2	TM3CK1	TM3CK0
At reset	-	-	-	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bp	Flag	Description
7-5	-	-
4	TM3CAS	Select timer 3 operation mode 0:Normal timer operation 1:Cascade connection
3	TM3EN	Timer 3 count control 0:Halt the count 1:Operate the count
2-0	TM3CK2 TM3CK1 TM3CK0	Select clock source X00:fosc X01:TM3PSC (Prescaler output) 010:fx 011:Synchronous fx 110:TM3IO input 111:Synchronous TM3IO input

■ Timer 4 Mode Register (TM4MD:0x03F64)

bp	7	6	5	4	3	2	1	0
Flag	-	TM4POP	TM4MOD	TM4PWM	TM4EN	TM4CK2	TM4CK1	TM4CK0
At reset	-	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bp	Flag	Description
7	-	-
6	TM4POP	On PWM mode, select start compulsion of output signal 0:timer output L→H, H→L 1:timer output H→L, L→H
5	TM4MOD	Pulse width measurement control 0:Normal timer operation 1:P24 pulse width measurement
4	TM4PWM	Select timer 4 operation mode 0:Normal timer operation 1:PWM operation
3	TM4EN	Timer 4 count control 0:Halt the count 1:Operate the count
2-0	TM4CK2 TM4CK1 TM4CK0	Select the clock source X00:fosc X01:TM4PSC (Prescaler output) 010:fx 011:Synchronou fx 110:TM4IO input 111:Synchronous TM4IO output

■ Timer 5 Mode Register (TM5MD:0x03F65)

bp	7	6	5	4	3	2	1	0
Flag	-	-	-	TM5CAS	TM5EN	TM5CK2	TM5CK1	TM5CK0
At reset	-	-	-	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bp	Flag	Description
7-5	-	-
4	TM5CAS	Select timer 5 operation mode 0:Normal timer operation 1:Cascade connection
3	TM5EN	Timer 5 count control 0:Halt the count 1:Operate the count
2-0	TM5CK2 TM5CK1 TM5CK0	Select clock source X00:fosc X01:TM5PSC (Prescaler output) 010:fx 011:Synchronous fx 110:TM5IO input 111:Synchronous TM5IO input

■ Timer I/O pin Switching Control Register (TMSEL:0x03F3F)

bp	7	6	5	4	3	2	1	0
Flag	-	TM7SEL	TM5SEL	TM4SEL	-	-	-	-
At reset	-	0	0	0	-	-	-	-
Access	-	R/W	R/W	R/W	-	-	-	-

bp	Flag	Description
7	-	-
6	TM7SEL	Switch timer 7 I/O pin 0:P16/TM7IOA 1:PD4/TM7IOB
5	TM5SEL	Switch timer 5 I/O pin 0:P15/TM5IOA 1:PD3/TM5IOB
4	TM4SEL	Switch timer 4 I/O pin 0:P14/TM4IOA 1:PD2/TM4IOB
3-0	-	-

■ External Interrupt Pin Switching Control Register (IRQSEL:0x03F4E)

bp	7	6	5	4	3	2	1	0
Flag	-	-	-	-	IRQ3SEL	IRQ2SEL	-	-
At reset	-	-	-	-	0	0	-	-
Access	-	-	-	-	R/W	R/W	-	-

bp	Flag	Description
7-4	-	-
3	IRQ3SEL	External interrupt 3 input pin switching 0:P23 1:PD1
2	IRQ2SEL	External interrupt 2 input pin switching 0:P22 1:PD0
1-0	-	-

5.3 Prescaler

5.3.1 Prescaler Operation

■ Prescaler Operation (Prescaler 0 to 1)

Prescaler 0, prescaler 1 are each free-run counter of 7 bits, 3 bits and output the dividing clock of the reference clock. This count up operation starts automatically when any TMnEN flags of 8-bit timer are set to "1" and operate the timer n counting. Also, it stops automatically when all TMnEN flags of 8-bit timer are set to "0" and stop all timer counting.

■ Count Timing of Prescaler Operation (Prescaler 0 to 1)

Prescaler 0 counts up at the falling edge of fosc.

Prescaler 1 counts up at the rising edge of fs.

■ Peripheral Functions

Peripheral functions which can use the prescaler output dividing clock, or registers which control the dividing clock selections are shown below.

Timer 0 Count Clock	CK0MD
Timer 1 Count Clock	CK1MD
Timer 2 Count Clock	CK2MD
Timer 3 Count Clock	CK3MD
Timer 4 Count Clock	CK4MD
Timer 5 Count Clock	CK5MD

Start the timer operation after the prescaler setup. Also, at the timer, the prescaler output should be set up by the timer mode register. The prescaler starts counting at the start of the timer operation.

5.3.2 Setup Example

■ Prescaler Operation Setup Example

fs/2 clock which is output from the prescaler 1 is selected to the count clock of the timer 0.

A setup procedure example, with a description of each step is shown below

Setup Procedure	Description
(1) Select the prescaler output CK0MD(0x03F56) bp2-1 :TM0PSC1-0 =X0 bp0 :TM0BAS =1	(1) Select fs/2 to the prescaler output by the TM0PSC 1 to 0, TM0BAS flag of the timer 0 prescaler selection register.

At the timer, prescaler output selection should be set up by the timer mode register.

5.4 8-bit Timer Count

5.4.1 8-bit Timer Operation

Timer operation can constantly generates interrupts.

■ 8-bit Timer Operation (Timers 0,1,2,3,4 and 5)

The generation cycle of timer interrupts is set by the clock source selection and the setting value of the compare register (TMnOC), in advance. If the binary counter (TMnBC) reaches the setting value of the compare register, an interrupt is generated at the next count clock, then binary counter is cleared and counting is restarted from 0x00.

Table shows clock source that can be selected by timer.

Clock source	per Count	Timer 0 (8-bit)	Timer 1 (8-bit)	Timer 2 (8-bit)	Timer 3 (8-bit)	Timer 4 (8-bit)	Timer 5 (8-bit)
fosc	50 ns	O	O	O	O	O	O
fosc/4	200 ns	O	O	O	O	O	O
fosc/16	800 ns	O	O	O	O	O	O
fosc/32	1.6 µs	O	-	O	-	O	-
fosc/64	3.2 µs	O	O	O	O	O	O
fosc/128	6.4 µs	-	O	-	O	-	O
fs/2	200 ns	O	O	O	O	O	O
fs/4	400 ns	O	-	O	-	O	-
fs/8	800 ns	-	O	-	O	-	O
fx	30.5 µs	O	O	O	O	O	O
fosc=20 MHz fx=32.768 kHz fs=fosc/2=10 MHz							

When fs/2, fs/4, fs/8 are used as clock source, they are counted at the rising of the count clock and when others are used, they are counted at the falling of the count clock.

■ Count Timing of Timer Operation (Timers 0,1,2,3,4 and 5)

Binary counter counts up with selected clock source as a count clock. The basic operation of the whole function of 8-bit timer is as follows:

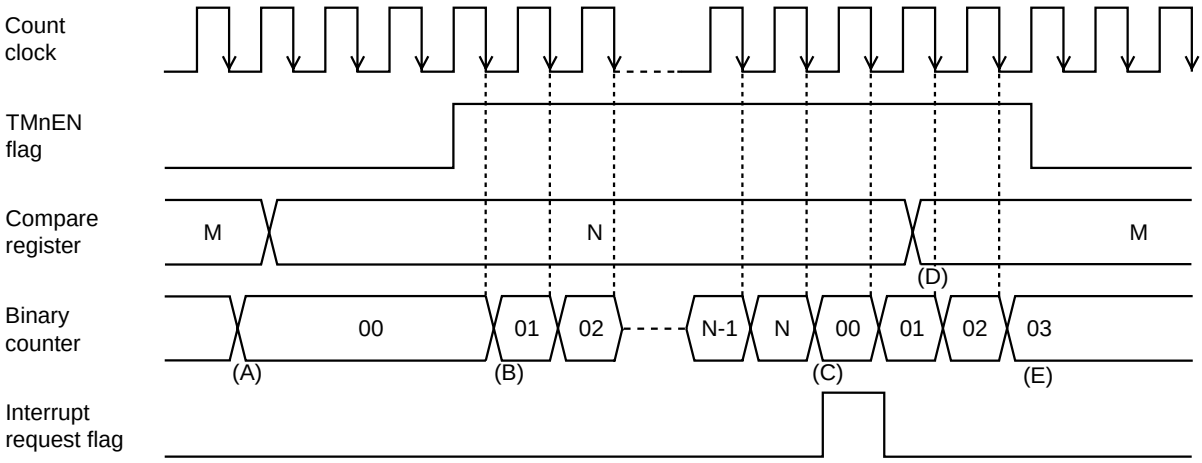


Figure:5.4.1 Count Timing of Timer Operation (Timers 0,1,2,3,4 and 5)

- (A)If the value is written to the compare register during the TMnEN flag is stopped ("0"), the binary counter is cleared to 0x00, at the writing cycle.
- (B)If the TMnEN flag is operated ("1"), the binary counter is started to count.

  The counter starts to count up at the falling edge of the count clock.
- (C)If the binary counter reaches the value of the compare register, the interrupt request flag is set at the next count clock, then the binary counter is cleared to 0x00 and the counting is restarted.
- (D)Even if the compare register is rewritten during the TMnEN flag is enabled ("1"), the binary counter is not cleared.
- (E)If the TMnEN flag is stopped ("0"), the binary counter is stopped.

When the binary counter reaches the value in the compare register, the interrupt request flag is set and the binary counter is cleared, at the next count clock. So set the compare register as:

Compare register setting = (count till the interrupt request -1)

If the compare register is set the smaller than the binary counter during the count operation, the binary counter counts up to the overflow, at first.

If the interrupt is enabled, the timer interrupt request flag should be cleared before timer is started.

The timer n interrupt request generation (at TMnOC = 0x00) has the same waveform at TMnOC = 0x01.

At NORMAL operation, when fx is selected as the clock source, even the value is written to the compare register with stopped the binary counter, it might not be cleared.
To clear the binary counter definitely, any value should be written to the compare register after the clock source which is synchronized to fosc or fs is selected.

When fx is used as the clock source, clear the binary counter before starting the timer operation. Also, when 0x00 is set to the compare register, use the synchronous fx.

5.4.2 Setup Example

■ Timer Operation Setup Example (Timers 0,1,2,3,4 and 5)

Timer function can be set by using timer 0 that generates the constant interrupt. Interrupt is generated every 250 cycles (100 μs) by selecting fs/2 (at fs=2.5 MHz operation) as a clock source.

A setup procedure example, with a description of each step is shown below.

Setup Procedure	Description
(1) Stop the counter TM0MD(0x03F54) bp3 :TM0EN =0	(1) Set the TM0EN flag of the timer 0 mode register (TM0MD) to "0" to stop the counting of the timer 0.
(2) Disable the interrupt TM0ICR(0x03FE8) bp1 :TM0IE =0	(2) Set the TM0IE flag of the TM0ICR register to "0" to disable the interrupt.
(3) Select the normal timer operation TM0MD(0x03F54) bp4 :TM0PWM =0 bp5 :TM0MOD =0	(3) Set the TM0PWM flag and the TM0MOD flag of the TM0MD register to "0" to select the normal timer operation.
(4) Select the count clock source TM0MD(0x03F54) bp2-0 :TM0CK2-0 =001	(4) Select the prescaler output to the clock source by the TM0CK2 to 0 flag of the TM0MD register.
(5) Select and enable the prescaler output CK0MD(0x03F56) bp2-1 :TM0PSC1-0 =X0 bp0 :TM0BAS =1	(5) Select fs/2 to the prescaler output by the TM0PSC 1 to 0 flag and TM0BAS flag of the timer 0 prescaler selection register (CK0MD).
(6) Set the cycle of the interrupt generation TM0OC (0x03F52) =0xF9	(6) Set the value of the interrupt generation cycle to the timer 0 compare register (TM0OC). The cycle is 250, so that the setting value is set to 249 (0xF9). At that time, the timer 0 binary counter (TM0BC) is initialized to 0x00.
(7) Set the interrupt level TM0ICR(0x03FE8) bp7-6 :TM0LV1-0 =10	(7) Set the interrupt level by the TM0LV1 to 0 flag of the timer 0 interrupt control register (TM0ICR). If the interrupt request flag may be already set, clear the request flag. [Chapter 3 3.1.4. Interrupt Flag Setting]
(8) Enable the interrupt TM0ICR (0x03FE8) bp1 :TM0IE =1	(8) Set the TM0IE flag of the TM0ICR register to "1" to enable the interrupt.
(9) Start the timer operation TM0MD(0x03F54) bp3 :TM0EN =1	(9) Set the TM0EN flag of the TM0MD register to "1" to operate the timer 0.

The TM0BC starts to count up from 0x00. When the TM0BC reaches the setting value of the TM0OC register, the timer 0 interrupt request flag is set at the next count clock, then the value of the TM0BC becomes 0x00 and restart to count up.

When the TMnEN flag of the TMnMD register is changed at the same time to other bit, binary counter may start to count up by the switching operation.

When the fx is selected for the count clock source and the value of the binary counter is read out during the operation, incorrect value at count up may be read out. To prevent this, select the synchronous fs for the count clock source. In this case, the binary counter is count up by the signal which is synchronized to the timer n system clock, therefore the correct value is always read out.

When the fosc is selected to the count clock source, the value of the binary counter may be not read out correctly.

Do not operate the TMnEN flag and the TMnCK 2 to 0 flag of the TMnMD register at the same time. That may lead the mulfunction.

When the count clock source is changed, set the timer interrupt enable.

5.5 8-bit Event Count

5.5.1 Operation

Event count operation has 2 types;TMnIO input and synchrocous TMnIO input, according to the clock source selection.

■ 8-bit Event Count Operation (Timers 0,1,2,3,4 and 5)

Event count operation means that the binary counter (TMnBC) counts the input signal from external to the TMnIO pin. If the value of the binary counter reaches the setting value of the compare register (TMnOC), interrupts can be generated at the next count clock.

Table:5.5.1 Event Count Input Clock

	Timer 0	Timer 1	Timer 2	Timer 3	Timer 4	Timer 5
Event input	TM0IO input (P10)	TM1IO input (P11)	TM2IO input (P12)	TM3IO input (P13)	TM4IO input (P14/PD2)	TM5IO input (P15/PD3)
	Synchronous TM0IO input	Synchronous TM1IO input	Synchronous TM2IO input	Synchronous TM3IO input	Synchronous TM4IO input	Synchronous TM5IO input

■ Count Timing of TMnIO Input (iTimers 0,1,2,3,4 and 5)

When TMnIO input is selected, TMnIO is input to the count clock of the timer n.

The binary counter is started to count up at the falling edge of the TMnIO input signal.

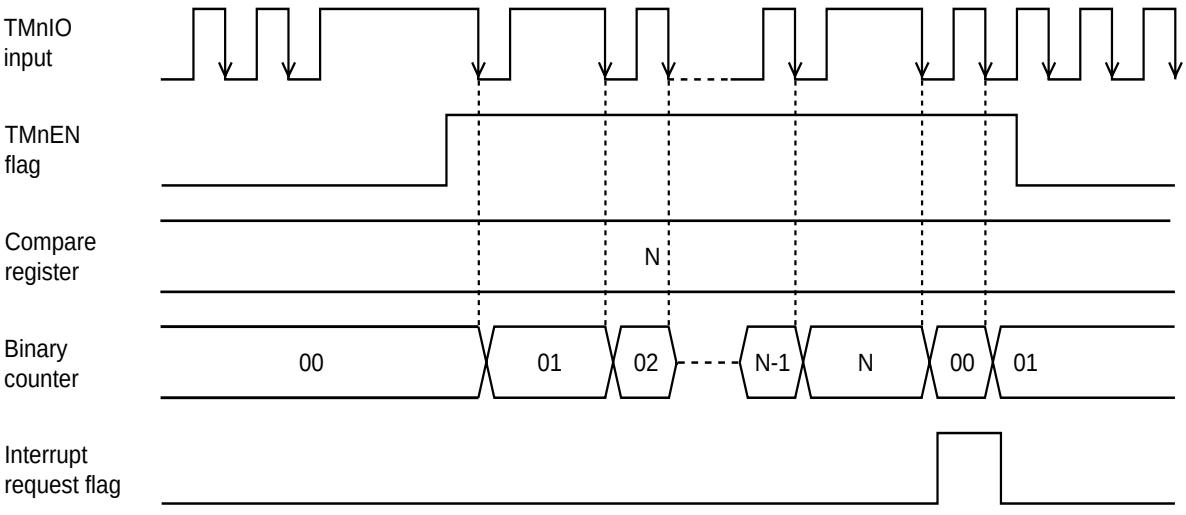


Figure:5.5.1 Count Timing of TMnIO Input (Timers 0,1,2,3,4 and 5)

When the binary counter is stopped, even any value is written to the compare register, it might not be cleared.
To clear the binary counter definitely, any value should be written to the compare register after the synchronous TMnIO input is selected.

When the TMnIO input is selected for count clock source and the value of the timer n binary counter is read out during operation, incorrect value at count up may be read out. To prevent this, use the event count by synchronous TMnIO input, as the following page.

When the event input (TMnIO input) is used, clear the binary count before the timer operation. Also, when 0x00 is set to the compare register, use the event count by the synchronous TMnIO input, as the following page.

CPU can be recovered from STOP mode by the timer interrupt only at the TMnIO input selection. When TMnIO input is used at STOP mode, fs should be selected for the count clock and set the value to TMnOC, then select TMnIO input.

■ Count Timing of Synchronous TMnIO Input (Timers 0,1,2,3,4 and 5)

If the synchronous TMnIO input is selected, the synchronous circuit output signal is inputted to the timer n count clock. The synchronous circuit output signal is synchronization with the falling edge of the system clock derived the TMnIO input signal.

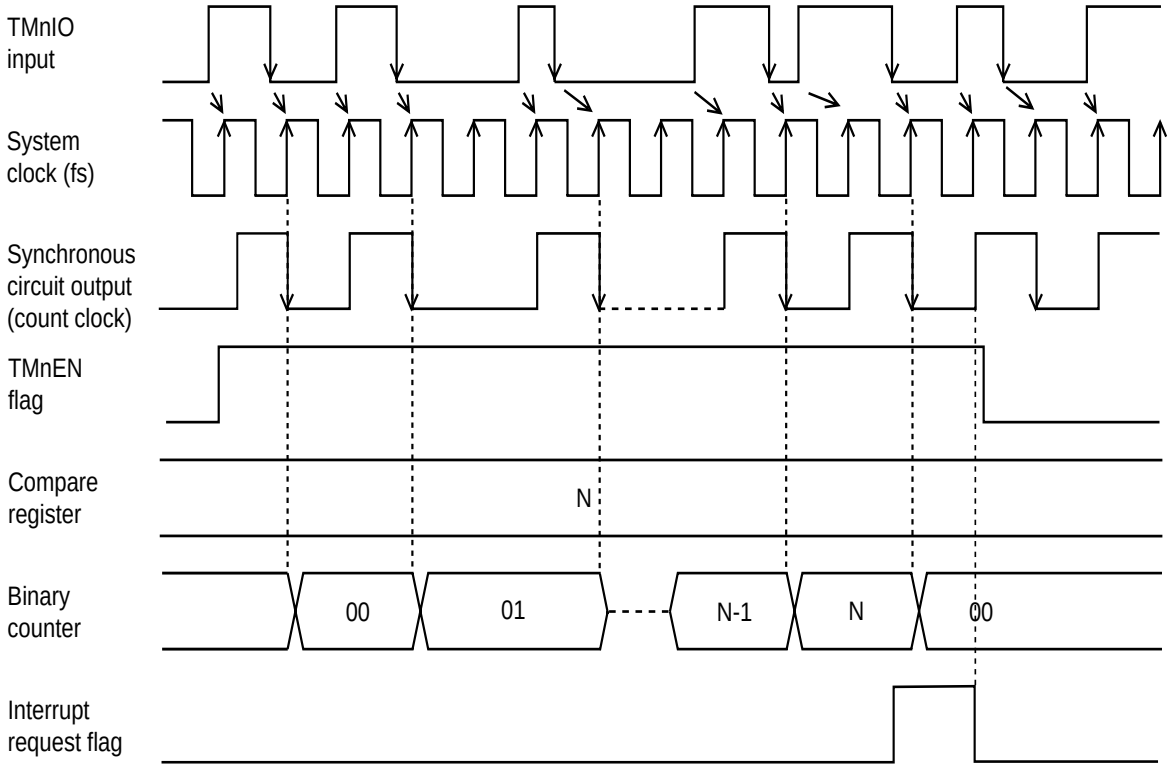


Figure:5.5.2 Count Timing of Synhronous TMnIO Input (Timers 0,1,2,3,4 and 5)

When the synchronous TMnIO input is selected as the count clock source, thetimer ncounter counts up in synchronization with system clock, therefore the correct value is always read out.

5.5.2 Setup Example

■ Event Count Setup Example (Timers 0,1,2,3,4 and 5)

If the falling edge of the TMnIO input pin signal is detected 5 times, an interrupt is generated.

A setup procedure example, with a description of each step is shown below.

Setup Procedure	Description
(1) Stop the counter TM0MD(0x03F54) bp3 :TM0EN =0	(1) Set the TM0EN flag of the timer 0 mode register to "0" to stop timer 0 counting.
(2) Disable the interrupt TM0ICR(0x03FE8) bp1 :TM0IE =0	(2) Set the TM0IE flag of the TM0ICR register to "0" to disable the interrupt.
(3) Set the special function pin to input P1DIR(0x03F31) bp0 :P1DIR0 =0	(3) Set the P1DIR0 flag of the port 1 direction control register (P1DIR) to "0" to set P10 pin to input mode. [Chapter 4. I/O Port Function]
(4) Select the count clock source TM0MD(0x03F54) bp2-0 :TM0CK2-0 =X01	(4) Select the prescaler output to the clock source by the TM0CK2 to 0 flag of the TM0MD register.
(5) Select and enable the prescaler output CK0MD(0x03F56) bp2-1 :TM0PSC1-0 =X0 bp0 :TM0BAS =1	(5) Select the fs/2 to the prescaler output by the TM0PSC1 to 0 flag and the TM0BAS flag of the timer 0 prescaler selection register (CK0MD).
(6) Set the interrupt generation cycle TM0OC (0x03F52) =0x04	(6) Set the interrupt generation cycle to the timer 0 compare register (TM0OC). Counting is 5, so the setting value should be 4. At the time, the timer 0 binary counter (TM0BC) is initializes to 0x00.
(7) Select the normal timer operation TM0MD(0x03F54) bp4 :TM0PWM =0 bp5 :TM0MOD =0	(7) Set the TM0PWM flag and the TM0MOD flag of the TM0MD register to "0" to select the normal timer operation.
(8) Select the count clock source TM0MD(0x03F54) bp2-0 :TM0CK2-0 =110	(8) Select the TM0IO input to the clock source by the TM0CK2 to 0 flag of the TM0MD register.
(9) Set the interrupt level TM0ICR(0x03FE8) bp7-6 :TM0LV1-0 =10	(9) Set the interrupt level by the TM0LV1 to 0 flag of the timer 0 interrupt control register (TM0ICR). If the interrupt request flag may be already set, clear the request flag. [Chapter 3 3.1.4. Interrupt Flag Setting]

Setup Procedure	Description
(10) Enable the interrupt TM0ICR(0x03FE8) bp1 :TM0IE =1	(10) Set the TM0IE flag of the TM0ICR register to "1" to enable the interrupt.
(11) Start the event count TM0MD(0x03F54) bp3 :TM0EN =1	(11) Set the TM0EN flag of the TM0MD register to "1" to operate the timer 0.

Every time TM0BC detects the falling edge of TM0IO input, TM0BC counts up from 0x00. When TM0BC reaches the setting value of TM0OC register, the timer 0 interrupt request flag is set at the next count clock, then the value of TM0BC becomes 0x00 and counting up is restarted.

5.6 8-bit Timer Pulse Output

5.6.1 Operation

The TMnIO pin can output a pulse signal at any frequency.

■ Operation of Timer Pulse Output (Timers 0,1,2,3,4 and 5)

The timers can output signals of 2 × cycle of the setup value in the compare register (TMnOC). Output pins are as follows;

Table:5.6.1 Timer Pusle Output Pin

	Timer 0	Timer 1	Timer 2	Timer 3	Timer 4	Timer 5
Pulse output pin	TM0IO output (P10)	TM1IO output (P11)	TM2IO output (P12)	TM3IO output (P13)	TM4IO output (P14, PD2)	TM5IO output (P15, PD3)

■ Count Timing of Timer Pulse Output (Timers 0,1,2,3,4 and 5)

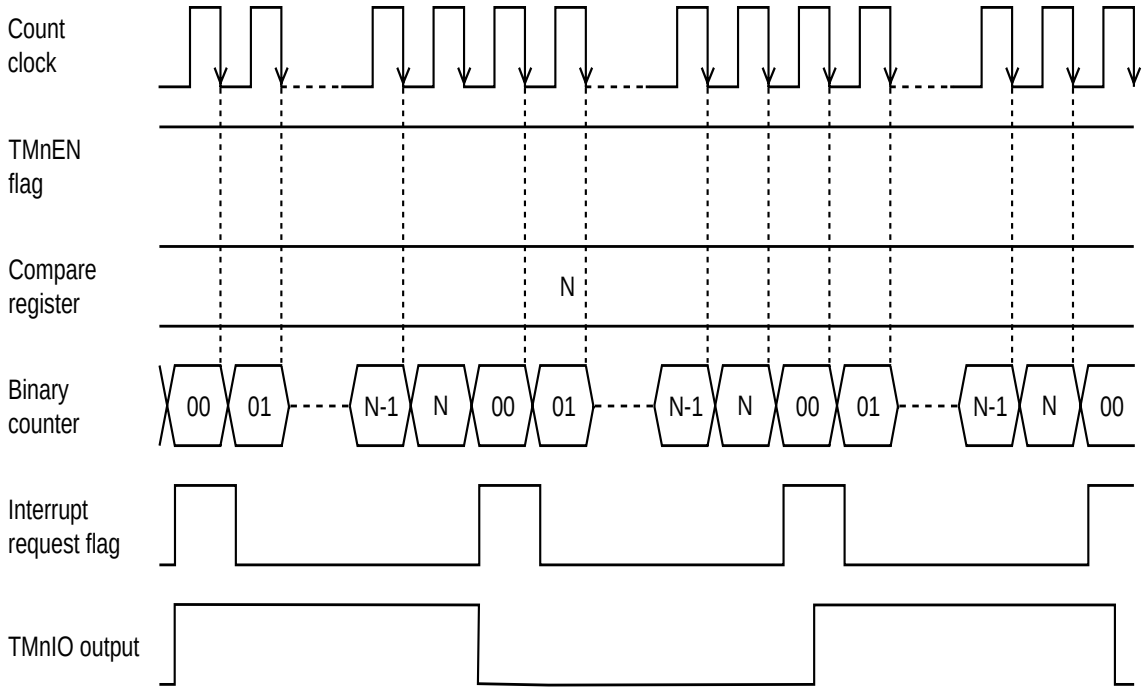


Figure:5.6.1 Count Timing of Timer Pulse Output (Timers 0,1,2,3,4 and 5)

- The TMnIO pin outputs signals of 2 × cycle of the setup value in the compare register. If the binary counter reaches the compare register, and the binary counter is cleared to 0x00, TMnIO output (timer output) is inverted. The invension of the timer output is changed at the rising edge of the count clock. This is happened to form waveform inside to correct the output cycle.

5.6.2 Setup Example

■ Timer Pulse Output Setup Example (Timers 0,1,2,3,4 and 5)

TM0IO pin outputs 50 kHz pulse by using timer 0. For this, select fs/2 for clock source, and set a 1/2 cycle (100 kHz) for the timer 0 compare register (at fs = 10 MHz).

An example setup procedure, with a description of each step is shown below.

Setup Procedure	Description
(1) Stop the counter TM0MD(0x03F54) bp3 :TM0EN =0	(1) Set the TM0EN flag of the timer 0 mode register (TM0MD) to "0" to stop timer 0 counting.
(2) Set the special function pin to the output mode P1OMD(0x03F2B) bp0 :P1OMD0 =1 P1DIR (0x03F31) bp0 :P1DIR0 =1	(2) Set the P1OMD0 flag of the port 1 output mode register (P1OMD) to "1" to set P10 pin to the special function pin. Set the TM0MOD flag of the port 1 direction control register (P1DIR) to "1" to set the output mode. [Chapter 4. I/O Port Function]
(3) Select the normal timer operation TM0MD(0x03F54) bp4 :TM0PWM =0 bp5 :TM0MOD =0	(3) Set the TM0MOD flag of the TM0MD register to "0" to select the normal timer operation.
(4) Select the count clock source TM0MD(0x03F54) bp2-0 :TM0CK2-0 =X01	(4) Select the prescaler output to the clock source by the TM0CK2 to 0 flag of the TM0MD register.
(5) Select and enable the prescaler output CK0MD(0x03F56) bp2-1 :TM0PSC1-0 =X0 bp0 :TM0BAS =1	(5) Select fs/2 to the prescaler output by the TM0PSC 1 to 0 flag and TM0BAS flag of the timer 0 prescaler selection register (CK0MD).
(6) Set the timer pulse output cycle TM0OC (0x03F52) =0x31	(6) Set the timer 0 compare register (TM0OC) to the 1/2 of the timer pulse output cycle. The setting value should be 50-1=49 (0x31), for 100 kHz to be divided by 5 MHz. At that time, the timer 0 binary counter (TM0BC) is initialized to 0x00.
(7) Start the timer operation TM0MD(0x03F54) bp3 :TM0EN =1	(7) Set the TM0EN flag of the TM0MD register to "1" to operate the timer 0.

TM0BC counts up from 0x00. If TM0BC reaches the setting value of the TM0OC register, then TM0BC is cleared to 0x00, TM0IO output signal is inverted and TM0BC restarts to count up from 0x00.

If any data is written to compare register when the binary counter is stopped, timer output is reset to "L".

At TMnOC=0x00, timer pulse output has the same waveform to at 0x01.

If any data is written to compare register when the binary counter is stopped, timer output is reset to "L".

[Compare register] Compare register=Timer pulse output / (Selection clock cycle × 2)-1

5.7 8-bit PWM Output

The TMnIO pin outputs the PWM waveform, which is determined by the match timing for the compare register and the overflow timing of the binary counter.

5.7.1 Operation

■ Operation of 8-bit PWM Output (Timers 0, 2 and 4)

The PWM waveform with an arbitrary duty cycle is generated by setting the duty cycle of ‘‘H‘‘ period to the compare register (TMnOC). The cycle is the period from the full count to the overflow of the 8-bit timer.

Table:5.7.1 shows PWM output pins;

Table:5.7.1 Output Pins of PWM Output

	Timer 0	Timer 2	Timer 4
PWM output pin	TM0IO output pin(P10)	TM2IO output pin(P12)	TM4IO output pin(P14, PD2)

■ Count Timing of PWM Output (at Normal) (Timers 0, 2 and 4)

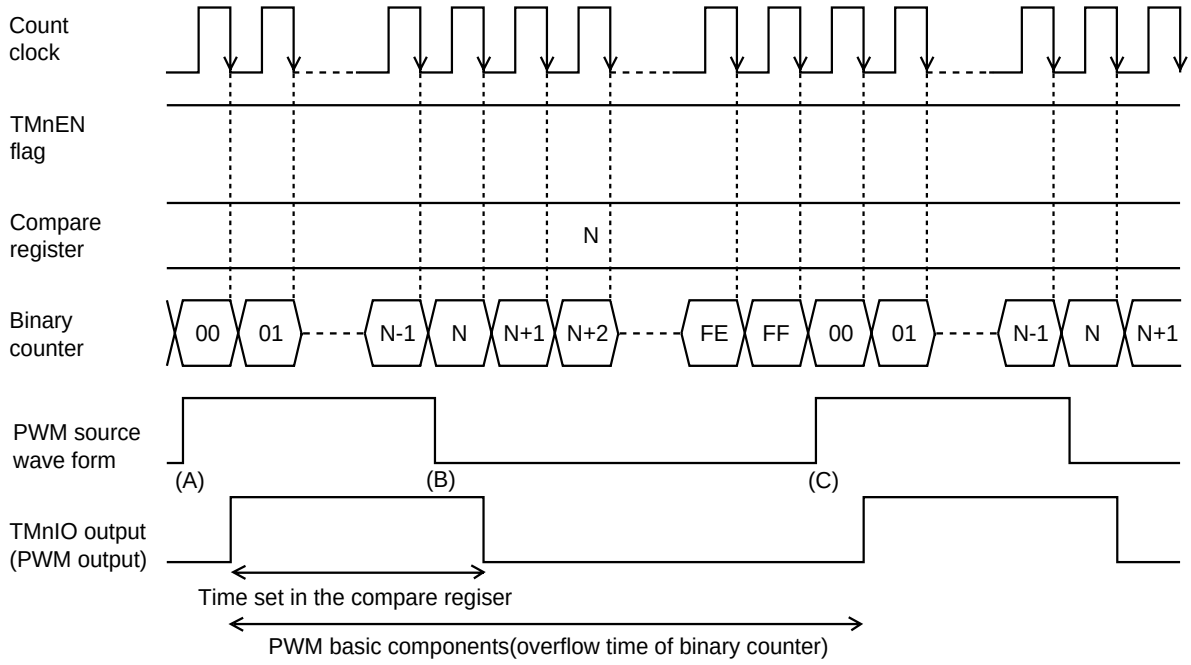


Figure:5.7.1 Count Timing of PWM Output (at Normal) (Timers 0, 2 and 4)

PWM source waveform

- (A) is "H" while counting up from 0x00 to the value stored in the compare register.
- (B) is "L" after the match to the value in the compare register, then the binary counter continues counting up till the overflow.
- (C) is "H" again, if the binary counter is overflown.

The PWM outputs PWM source waveform with 1 count clock delay, because the waveform is created inside to correct the output cycle.

■ Count Timing of PWM Output (when the compare register is 0x00) (Timers 0, 2 and 4)

Here is the count timing when the compare register is set to 0x00.

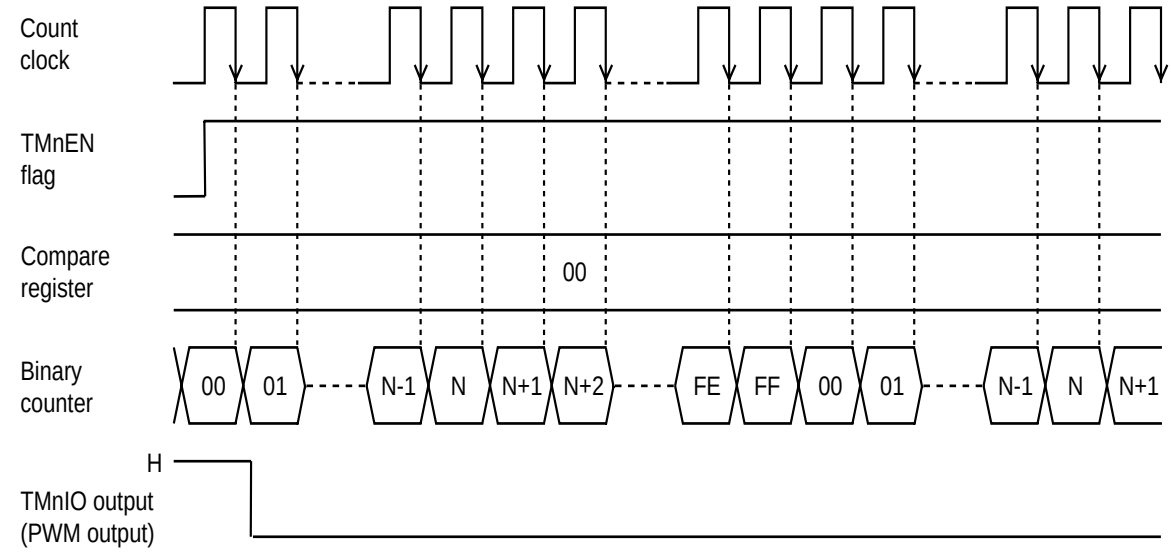


Figure:5.7.2 Count Timing of PWM Output (when compare register is 0x00)

When TMnEN flag is stopped ("0"), PWM output is "H".

■ Count Timing of PWM Output (when the compare register is 0xFF) (Timers 0, 2 and 4)

Here is the count timing when the compare register is set to 0xFF.

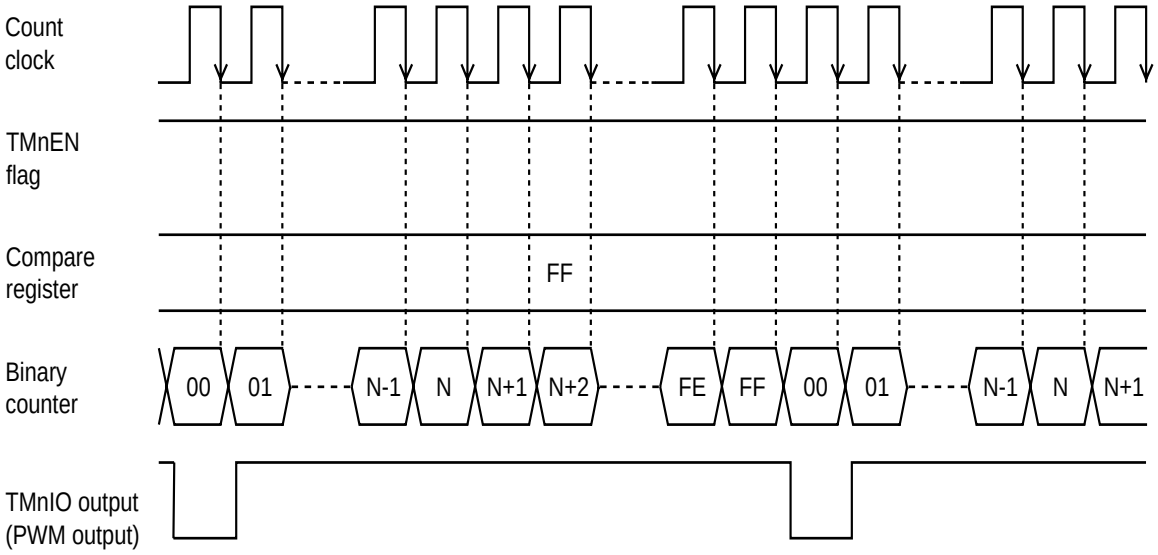


Figure:5.7.3 Count Timing of PWM Output (when the compare register is 0xFF) (Timers 0, 2 and 4)

5.7.2 Setup Example

■ PWM Output Setup Example (Timers 0, 2 and 4)

The 1/4 duty cycle PWM output waveform is output from the TM0IO output pin at 19.53 kHz by using the timer 0. Fs/2 oscillates at 5 MHz. Cycle period of PWM output waveform is decided by the overflow of the binary counter. "H" period of the PWM output waveform is decided by the setting value of the compare register.

An example setup procedure, with a description of each step is shown below.

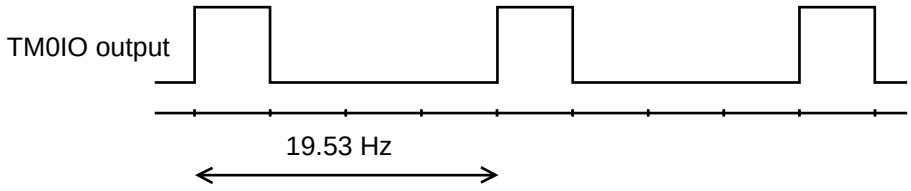


Figure:5.7.4 Output Waveform of TM0IO Output Pin

Setup Procedure	Description
(1) Stop the counter TM0MD(0x03F54) bp3 :TM0EN =0	(1) Set the TM0EN flag of the timer 0 mode register (TM0MD) to "0" to stop the timer 0 counting.
(2) Set the special function pin to the output mode P1OMD(0x03F2B) bp0 :P1OMD0 =1 P1DIR (0x03F31) bp0 :P1DIR0 =1	(2) Set the P1OMD0 flag of the port 1 output mode register (P1OMD) to "1" to set P10 pin to the special function pin. Set the TM0MOD flag of the port 1 direction control register (P1DIR) to "1" to set the output mode. [Chapter 4. I/O Port Function]
(3) Select the PWM operation TM0MD(0x03F54) bp4 :TM0PWM =1 bp5 :TM0MOD =0 bp6 :TM0POP =0	(3) Set the TM0PWM flag of the TM0MD register to "1" and the TM0MOD flag to "0" , and the TMOPOP flag to "0" to select the PWM operation.
(4) Select the count clock source TM0MD(0x03F54) bp2-0 :TM0CK2-0 =001	(4) Select the prescaler output to the clock source by the TM0CK2 to 0 flag of the TM0MD register.
(5) Select and enable the prescaler output CK0MD(0x03F56) bp2-1 :TM0PSC1-0 =X0 bp0 :TM0BAS =1	(5) Select fs/2 to the prescaler output by the TM0PSC1 to 0 and TM0BAS flag of the timer 0 prescaler selection register.

Setup Procedure	Description
(6) Set the period of PWM "H" output TM0OC (0x03F52) =0x40	(6) Set the "H" period of PWM output to the timer 0 compare register (TM0OC). The setting value is set to 256/4=64 (0x40), because it should be the 1/4 duty of the full count (256). At that time, the timer 0 binary counter (TM0BC) is initialized to 0x00.
(7) Start the timer operation TM0MD(0x03F54) bp3 :TM0EN =1	(7) Set the TM0EN flag of the TM0MD register to "1" to operate the timer 0.

TM0BC counts up from 0x00. PWM source waveform outputs "H" till TM0BC reaches the setting value of the TM0OC register, and outputs "L" after that. Then, TM0BC continues counting up, and PWM source waveform outputs "H" again, once overflow is happened, and TM0BC restarts counting up from 0x00. TM0IO pin outputs the PWM source waveform with 1 count clock delay.

The initial setting of PWM output is changed from "L" output to "H" output at the selection of PWM operation by the TMnPWM flag of the TMnMD register.

5.8 Synchronous Output

5.8.1 Operation

When the binary counter of the timer reaches the set value of the compare register, the latch data is output from port 7 at the next count clock.

■ Synchronous Output Operation by 8-bit Timer (Timers 1 and 2)

The port 7 latched data is output from the output pin in synchronization with the interrupt request generation by the match of the binary counter and the compare register.

Only port 7 can perform synchronous output operation, and individual bits can be set. 8-bit timers that have synchronous output operation are the Timers 1 and 2.

Table:5.8.1 Synchronous Output Port (iTimers 1 and 2)j

	Timer 1	Timer 2
Synchronous output port	Port 7	Port 7

■ Timing of Synchronous Output (Timers 1 and 2)

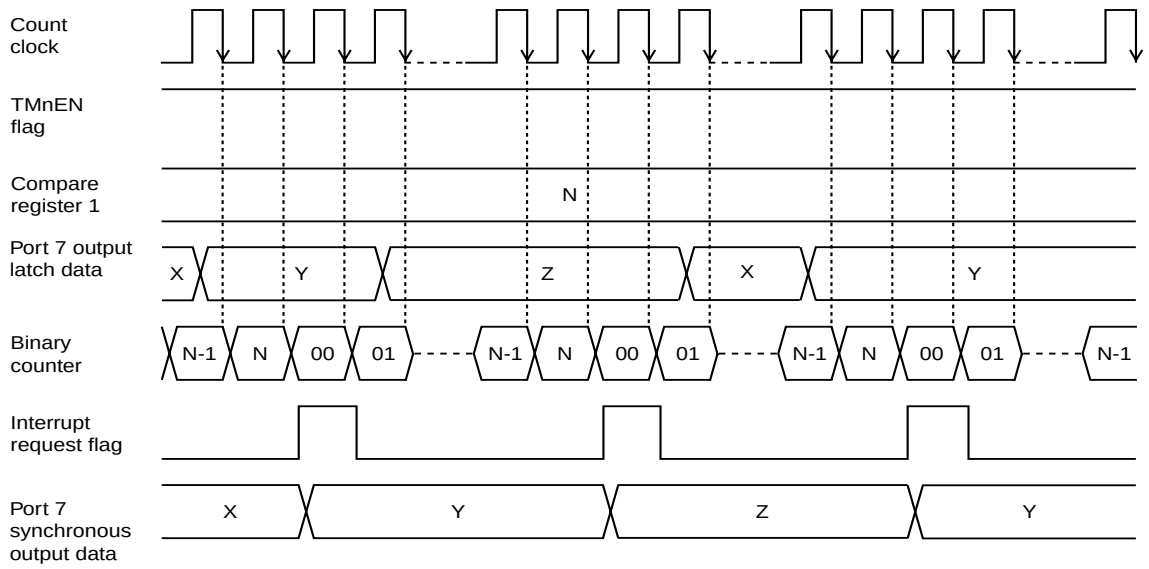


Figure:5.8.1 Timing of Synchronous Output (Timers 1 and 2)

- The port 7 output latched data is output from the output pin in synchronization with the interrupt request generation by the match of binary counter and compare register.

5.8.2 Setup Example

■ Synchronous Output Setup Example (Timers 1 and 2)

Setup example that latch data of port 7 is output constantly (100 µs) by using the timer 1 from the synchronous output pin is shown below. The clock source of the timer 1 is selected fs/2 (fs=2 MHz at operation).

A setup procedure example, with a description of each step is shown below.

Setup Procedure	Description
(1) Stop the counter TM1MD(0x03F55) bp3 :TM1EN =0	(1) Set the TM1EN flag of the timer 1 mode register (TM1MD) to "0" to stop the timer 1 counting.
(2) Select the synchronous output event P7SEV(0x03F2F) bp1-0 :P7SEV1-0 =11	(2) Set the P7SEV1to 0 flag of the pin control register (P7SEV) to "11" to set the synchronous output event to the timer 1 interrupt.
(3) Set the synchronous output pin P7SYO(0x03F1F) =0xFF P7DIR(0x03F37) =0xFF	(3) Set the port 7 synchronous output control register (P7SYO) to 0xFF to set the synchronous output pin. Set the port 7 direction control register (P7DIR) to 0xFF to set port 7 to output mode.
(4) Select the normal timer operation TM1MD(0x03F55) bp4 :TM1CAS =0	(4) Set the TM1CAS flag of the TM1MD register to "0" to select the normal timer operation.
(5) Select and enable the prescaler output TM1MD(0x03F55) bp2-0 :TM1CK2-0 =X01	(5) Select the prescaler output to the clock source by the TM1CK2 to 0 flag of the TM1MD register.
(6) Select and enable the prescaler output CK1MD(0x03F57) bp2-1 :TM1PSC1-0 =X0 bp0 :TM1BAS =1	(6) Select fs/2 to the prescaler output by the TM1PSC1 to 0 and TM1BAS flag of the timer 1 prescaler selection register (CK1MD).
(7) Set the synchronous output event TM1OC (0x03F53) =0x63	(7) Set the synchronous output generation cycle to the timer 1 compare register (TM1OC). The setting value is set to 100-1=99 (0x63), because 1 MHz is divided by 10 KHz. At that time, the timer 1 binary counter (TM1BC) is initialized to 0x00.
(8) Start the timer operation TM1MD(0x03F55) bp3 :TM1EN =1	(8) Set the TM1EN flag of the TM1MD register to "1" to operate the timer 1.

- TM1BC counts up from 0x00. If any data is written to the port 7 output register (P7OUT), the data of port 7 is output from the synchronous output pin in every time an interrupt request is generated by the match of TM1MC and the set value of the TM1OC register.

5.9 Serial Transfer Clock Output

5.9.1 Operation

Serial transfer clock can be created by using the timer output signal.

Serial transfer clock operation by 8-bit timer (Timers 2, 3, 4 and 5)

- Timer 2:Serial interface 0, 2, and 4
- Timer 3:Serial interface 2, and 3
- Timer 4:Serial interface 0,1
- Timer 5:Serial interface 1, 3, and 4

■ Timing of Serial Transfer Clock (Timers 2, 3, 4 and 5)

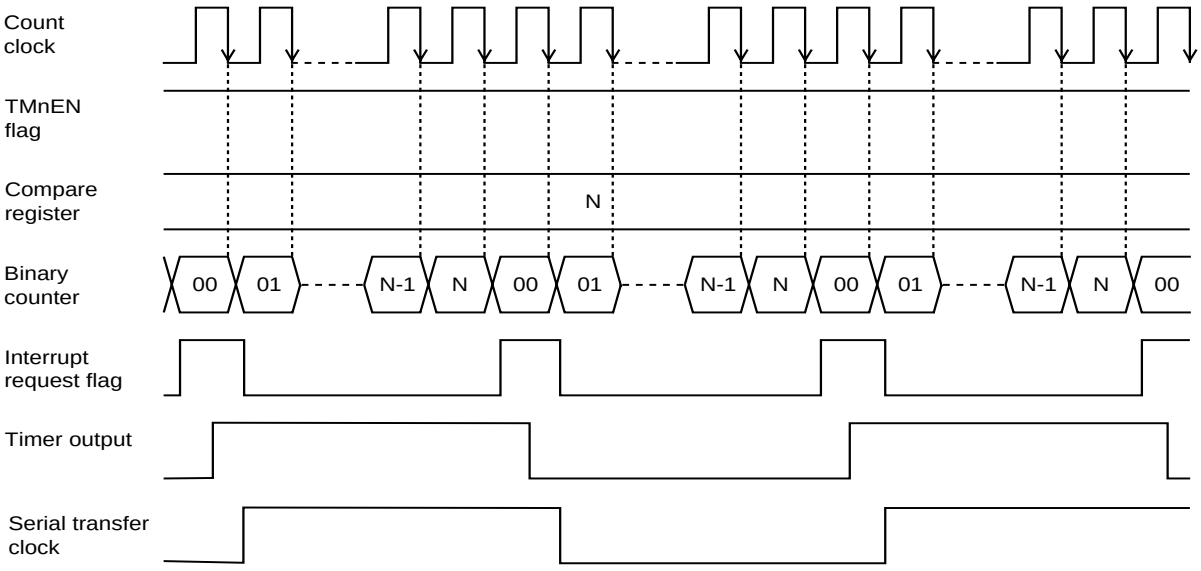


Figure:5.9.1 Timing of Serial Transfer Clock (Timers 2, 3, 4 and 5)

- The timer output is synchronized to the serial transfer clock by the timer count clock, and its frequency is 1/2 of the set frequency set by the compare register.
- Other count timings are the same as the timing of timer operation.
- For the baud rate calculation and the serial interface setup, refer to Serial Interface .

5.9.2 Setup Example

■ Serial Transfer Clock Setup Example (Timer 2)

How to create a transfer clock for full duplex UART (Serial 4) using with the timer 2 is shown below. The baud rate is selected to be 300 bps, the source clock of timer2 is selected to be fs/2 (at fs=2 MHz).

An example setup procedure, with a description of each step is shown below.

Setup Procedure	Description
(1) Stop the counter TM2MD(0x03F5C) bp3 :TM2EN =0	(1) Set the TM2EN flag of the timer 2 mode register (TM2MD) to "0" to stop the timer 2 counting.
(2) Select the normal timer operation TM2MD(0x03F5C) bp4 :TM2PWM =0 bp5 :TM2MOD =0	(2) Set the TM2PWM flag and the TM2MOD flag of the TM2MD register to "0" to select the normal timer operation.
(3) Select the count clock source TM2MD(0x03F5C) bp2-0 :TM2CK2-0 =001	(3) Select the prescaler output to the clock source by the TM2CK2 to 0 flag of the TM2MD register.
(4) Select and enable the prescaler output CK2MD(0x03F5E) bp2-1 :TM2PSC1-0 =X0 bp0 :TM2BAS =1	(4) Select fs/2 to the prescaler output by the TM2PSC1 to 0 flag and the TM2BAS flag of the timer 2 prescaler selection register.
(5) Set the baud rate TM2OC (0x03F5A) =0xCF	(5) Set the timer 2 compare register (TM2OC) such a value that the baud rate comes to 300 bps. At that time, the timer 2 binary counter (TM2BC) is initialized to 0x00.
(6) Start the timer operation TM2MD(0x03F5C) bp3 :TM2EN =1	(6) Set the TM2EN flag of the TM2MD register to "1" to operate the timer 2.

- TM2BC counts up from 0x00. Timer 2 output is the clock of the serial interface 4 at transmission and reception.
- Refer to Chapter 15 about the value of compare register setting and serial operation setting

5.10 Simple Pulse Width Measurement

5.10.1 Operation

Timer measures the "L" duration of the pulse signal input from the external interrupt pin.

■ Simple Pulse Width Measurement Operation by 8-bit Timer (Timers 0, 2 and 4)

When the input signal of the external interrupt pin (simple pulse width) is "L", the binary counter of the timer counts up. Pulse width "L" period can be measured by reading the count of timer. 8-bit timers that have the simple pulse width measurement function are the Timers 0, 2 and 4.

Table:5.10.1 Simple Pulse Width Measurement Able Pins

	Timer 0	Timer 2	Timer 4
Simple pulse width measurement enable pin	External interrupt 2 (P22/ IRQ2A, PD0/IRQ2B)	External interrupt 3 (P23/ IRQ3A, PD1/IRQ3B)	External interrupt 4 (P24/ IRQ4)

■ Count Timing of Simple Pulse Width Measurement (Timers 0, 2 and 4)

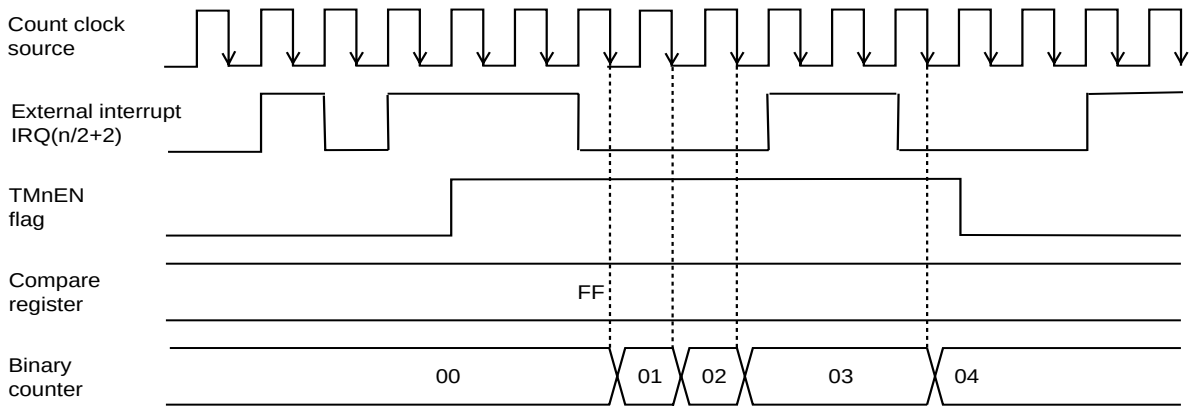


Figure:5.10.1 Count Timing of Simple Pulse Width Measurement (Timers 0, 2 and 4)

- When the input signal of the external interrupt pin for simple pulse width measurement is "L" at TMnEN flag operation is ("1"), the timer counts up.

5.10.2 Setup Example

■ Setup Example of Simple Width Measurement by 8-bit Timer (Timers 0, 2 and 4)

The pulse width of "L" period of the external interrupt 2 (IRQ2) input signal is measured by the timer 0. The clock source of the timer 0 is selected to fs/2.

A setup procedure example, with a description of each step is shown below.

Setup Procedure	Description
(1) Stop the counter TM0MD(0x03F54) bp3 :TM0EN =0	(1) Set the TM0EN flag of the timer 0 mode register (TM0MD) to "0" to stop the timer 0 counting.
(2) Set the pulse width measurement operation TM0MD(0x03F54) bp4 :TM0PWM =0 bp5 :TM0MOD =1	(2) Set the TM0PWM flag of the TM0MD register to "0" and TM0MOD flag to "1" to enable the timer operation during "L" period to be measured.
(3) Select the count clock source TM0MD(0x03F54) bp2-0 :TM0CK2-0 =001	(3) Select the prescaler output to the clock source by the TM0CK2 to 0 flag of the TM0MD register.
(4) Select and enable the prescaler output CK0MD(0x03F56) bp2-1 :TM0PSC1-0 =X0 bp0 :TM0BAS =1	(4) Select fs/2 to the prescaler output by the TM0PSC1 to 0 flag and the TM0BAS flag of the timer 0 prescaler selection register (CK0MD).
(5) Set the compare register TM0OC (0x03F52) =0x'FF'	(5) Set the timer 0 compare register (TM0OC) to the bigger value than "L" period (the cycle of fs/2) of measured pulse width. At that time, the timer 0 binary counter (TM0BC) is initialized to 0x00.
(6) Set the interrupt pin IRQ2ICR(0x03F4E) bp2:IRQ2SEL =0	(6) Set the external interrupt 2 pin to IRQ2A by the IRQ2SEL flag of the external interrupt 2 control register (IRQSEL).
(7) Set the interrupt valid input IRQ2ICR(0x03F6D) bp0 :LVLEN2 =0	(7) Set the IRQ2A valid input to edge by LVLEN2 flag of external interrupt valid input switching control register(LVLMD).
(8) Set the interrupt level IRQ2ICR(0x03FE4) bp7-6 :IRQ2LV1-0 ="XX"	(8) Set the interrupt level by IRQ2LV1-0 flag of external interrupt 2 control register. Reset the request flag when interrupt request flag is already set. [Chapter3. 3.1.4 Interrupt Flag Setup]
(9) Set the interrupt valid edge IRQ2ICR(0x03FE4) bp5 :REDG2 =1	(9) Set the REDG2 flag of the IRQ2ICR register to "1" to specify the interrupt valid edge to the rising edge.

Setup Procedure	Description
(10) Enable the interrupt IRQ2ICR(0x03FE4) bp5 :RED2IE =1	(10) Set the IRQ2IE flag of the IRQ2ICR register to "1" to enable the interrupt.
(11) Enable the timer operation TM0MD(0x03F54) bp3 :TM0EN =1	(11) Set the TMOEN flag of TMOMD register to enable the timer 0 operation.

- TM0BC2 starts to count up from 0x00 with negative edge of the external interrupt 2 (IRQ2A) input as a trigger. Timer 0 continues to count up during "L" period of IRQ2A input, then stop the counting with positive edge of IRQ2A input as a trigger. At the same time, reading the value of TM2BC by interrupt handling can detects "L" period of IRQ2 input.

5.11 Cascade Connection

5.11.1 Operation

Cascading Timers 0 and 1 or Timers 2 and 3 or Timers 4 and 5 forms a 16-bit timer.

■ 8-bit Timer Cascade Connection Operation (Timer 0 + Timer 1, Timer 2 + Timer 3, Timer 4 + Timer 5)

Timers 0 and 1 or Timers 2 and 3 or Timers 4 and 5 are combined to be a 16-bit timer. Cascading timer is operated at the clock source of Timers 0,2 or 4 which are lower 8 bits.

Table:5.11.1 Timer Functions at Cascade Connection

	Timer 0+Timer1 (16-bit)	Timer 2+Timer 3 (16-bit)	Timer 4+Timer 5 (16-bit)
Interrupt source	TM1IRQ	TM3IRQ	TM5IRQ
Timer operation	O	O	O
Event count	O TM0IO input	O TM2IO input	O TM4IO input
PWM output	-	-	-
Synchronous output	O	-	-
Pulse width measurement	-	-	-
Clock source	fosc fosc/4 fosc/16 fosc/32 fosc/64 fs/2 fs/4 synchronous fx synchronous TM0IO input	fosc fosc/4 fosc/16 fosc/32 fosc/64 fs/2 fs/4 synchronous fx synchronous TM2IO input	fosc fosc/4 fosc/16 fosc/32 fosc/64 fs/2 fs/4 synchronous fx synchronous TM4IO input
fosc:Machine clock (High frequency oscillation) fx:Machine clock (Low frequency oscillation) fs:System clock [Chapter 2. 2.5 Clock Switching]			

- At cascade connection, the binary counter and the compare register are operated as a 16-bit register. At operation, set the TMnEN flag of the upper and lower 8-bit timers to "1" to be operated.

  Also, select the clock source by the lower 8-bit timer.

  Other setup and count timing is the same to the 8-bit timer at independently operation.

When timer 0 and timer 1 are used in cascade connection, timer 1 is used as an interrupt request flag. Timer pulse output of timer 0 is "L" fixed output.
An interrupt request of timer 0 is not generated, but the timer 0 interrupt should be disabled.

When timer 2 and timer 3 are used in cascade connection, timer 3 is used as an interrupt request flag. Timer pulse output of timer 2 is "L" fixed output.
An interrupt request of timer 2 is not generated, but the timer 2 interrupt should be disabled.

When timer 4 and timer 5 are used in cascade connection, timer 5 is used as an interrupt request flag. Timer pulse output of timer 4 is "L" fixed output.
An interrupt request of timer 4 is not generated, but the timer 4 interrupt should be disabled.

At cascade connection, when the clear of the binary counter is needed by rewriting the compare register, set the TMnEM flag of both the upper 8-bit timer and the lower 8-bit timer to "0" to stop counting.

5.11.2 Setup Example

■ Cascade Connection Timer Setup Example (Timer 0 + Timer 1, Timer 2 + Timer 3, Timer 4 + Timer 5)

Setting example of timer function that an interrupt is constantly generated by cascade connection of the timer 0 and the timer 1, as a 16-bit timer is shown. An interrupt is generated 2500 times every 1 ms by selecting source clock fs/2 (fs=5 MHz at operation).

An example setup procedure, with a description of each step is shown below.

Setup Procedure	Description
(1) Stop the counter TM0MD(0x03F54) bp3 :TM0EN =0 TM1MD(0x03F55) bp3 :TM1EN =0	(1) Set the TM0EN flag of the timer 0 mode register (TM0MD) to "0", the TM1EN flag of the timer 1 mode register to "0" to stop the timer 0 and the timer 1 counting.
(2) Disable the timer interrupt TM0ICR(0x03FE8) bp1 :TM0IE =0 TM1ICR(0x03FE9) bp1 :TM1IE =0	(2) Set the TM0IE flag of the timer 0 interrupt control register (TM0ICR) and the TM1IE flag of the timer 1 interrupt control register (TM1ICR) to "0" and to disable the interrupt.
(3) Select the normal lower timer operation TM0MD(0x03F54) bp4 :TM0PWM =0 bp5 :TM0MOD =0	(3) Set the TM0PWM flag and the TM0MOD flag of the TM0MD register to "0" to select the normal timer 0 operation.
(4) Set the cascade connection TM1MD(0x03F55) bp4 :TM1CAS =1	(4) Set the TM1CAS flag of the TM1MD register to "1" to connect the timer 1 and the timer 0 to the cascade.
(5) Select the count clock source TM0MD(0x03F54) bp2-0 :TM0CK2-0 =001	(5) Select the prescaler to the clock source by the TM0CK2 to 0 flag of the TM0MD register.
(6) Select and enable the prescaler output CK0MD(0x03F56) bp2-1 :TM0PSC1-0 =X0 bp0 :TM0BAS =1	(6) Select fs/2 to the prescaler output by the TM0PSC1 to 0 flag and the TM0BAS flag of the timer 0 prescaler selection register (CK0MD).
(7) Set the interrupt generation cycle TMnOC(0x03F53,0x03F52) =0x09C3	(7) Set the timer 1 compare register + timer 0 compare register (TM1OC + TM0OC) to the interrupt generation cycle (0x09C3:2500 cycles -1). At that time, timer 1 binary counter + timer 0 binary counter (TM1BC + TM0BC) are initialized to 0x000.
(8) Set the level of the upper timer interrupt TM1ICR(0x03FE9) bp7-6 :TM1LV1-0 =10	(8) Set the interrupt level by the TM1LV1 to 0 flag of the timer 1 interrupt control register (TM1ICR). If any interrupt request flag may be already set, clear all request flags. [Chapter 3. 3.1.4 Interrupt Flag Setup]

Setup Procedure	Description
(9) Enable the upper timer interrupt TM1ICR(0x03FE9) bp1 :TM1IE =1	(9) Set the TM1IE flag of the TM1ICR register to "1" to enable the interrupt.
(10) Start the upper timer operation TM1MD(0x03F55) bp3 :TM1EN =1	(10) Set the TM1EN flag of the TM1MD register to "1" to operate the timer 1.
(11) Start the lower timer operation TM0MD(0x03F54) bp3 :TM0EN =1	(11) Set the TM0EN flag of the TM0MD register to "1" to operate the timer 0.

- TM1BC + TM0BC counts up from 0x0000 as a 16-bit timer.

  When TM1BC + TM0BC reaches the set value of TM1BC + TM0BC register, the timer 1 interrupt request flag is set at the next count clock, and the value of TM1BC + TM0BC becomes 0x0000 and restarts count up.

Use a 16-bit access instruction to set the (TM1OC + TM0OC) register.

Start the upper timer operation before the lower timer operation.

Chapter 6 16-bit Timer

6

6.1 Overview

This LSI contains a general-purpose 16-bit timer (Timer 7). Its compare register is double buffer type. Timer 7 (high function 16-bit timer) has 2 sets of compare registers with double buffering. Also, as an independent interrupt it has a timer 7 interrupt and timer 7 compare register 2 match interrupt.

6.1.1 Functions

Table:6.1.1 shows the functions of each timer.

Table:6.1.1 16-bit Timer functions

	Timer 7 (High precision 16-bit timer)
Input source	TM7IRQ T7OC2IRQ
Timer operation	O
Event count	O TM7IO input/SynchronousTM7IO input
Timer pulse output	O TM7IO output
PWM output (duty is changeable)	O TM7IO output
High precision PWM output (duty/cycle are changeable)	OTM7IO output
Synchronous output	O
Capture function	O
Pulse width measurement	O
Clock source	fosc fosc/2 fosc/4 fosc/16 fs fs/2 fs/4 fs/16 TM7IO input TM7IO input/2 TM7IO input/4 TM7IO input/16 SynchronousTM7IO input SynchronousTM7IO input/2 SynchronousTM7IO input/4 SynchronousTM7IO input/16
fosc:Machine clock (High frequency oscillation) fs:System clock [Chapter 2. 2.6 Clock Switching]	

6.1.2 Block Diagram

■ Timer 7 Block Diagram

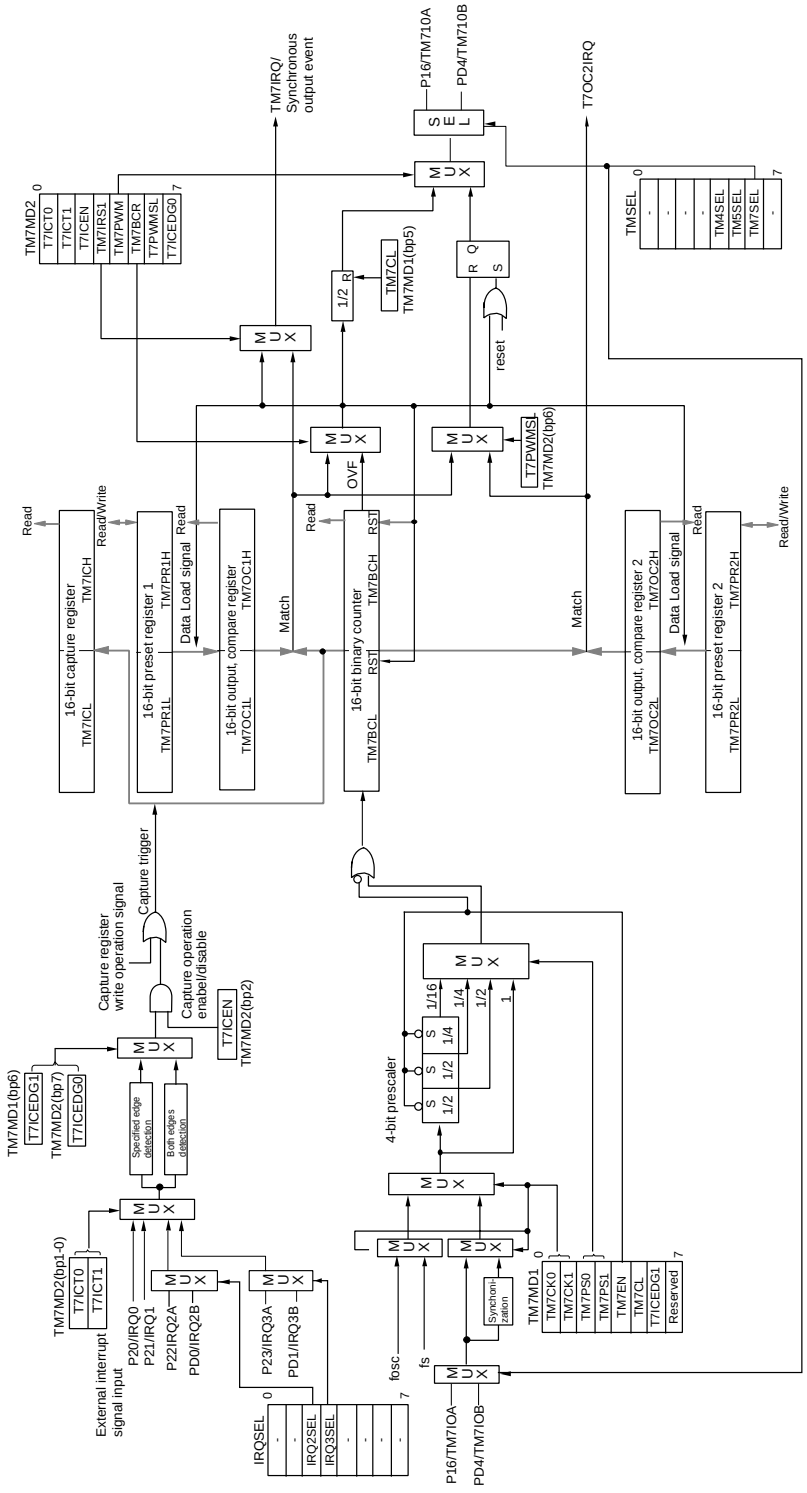


Figure:6.1.1 Timer 7 Block Diagram

6.2 Control Registers

Timer 7 the binary counter (TM7BC), the compare register 1 (TM7OC1), and its double buffer present register (TM7PR1), the compare register 2 (TM7OC2) and its double buffer preset register 2 (TM7PR2) , the capture register (TM7IC).The mode register 1 (TM7MD1) and mode register 2 (TM7MD2) controls timer 7.

6.2.1 Registers

Table:6.2.1 shows the registers that control timer 7.

Table:6.2.1 16-bit Timer Control Registers

Register	Address	R/W	Function	Page
TM7BCL	0x03F70	R	Timer 7 binary counter (lower 8 bits)	VI-7
TM7BCH	0x03F71	R	Timer7 binary counter (upper 8 bits)	VI-7
TM7OC1L	0x03F72	R	Timer 7 compare register 1 (lower 8 bits)	VI-5
TM7OC1H	0x03F73	R	Timer 7 compare register 1 (upper 8 bits)	VI-5
TM7PR1L	0x03F74	R/W	Timer 7 preset register 1 (lower 8 bits)	VI-6
TM7PR1H	0x03F75	R/W	Timer 7 preset register 1 (upper 8 bits)	VI-6
TM7ICL	0x03F76	R	Timer 7 capture register 1 (lower 8 bits)	VI-7
TM7ICH	0x03F77	R	Timer 7 capture register 1 (upper 8 bits)	VI-7
TM7MD1	0x03F78	R/W	Timer 7 mode register 1	VI-8
TM7MD2	0x03F79	R/W	Timer 7 mode register 2	VI-10
TM7OC2L	0x03F7A	R	Timer 7 compare register 2 (lower 8 bits)	VI-5
TM7OC2H	0x03F7B	R	Timer 7 compare register 2 (upper 8 bits)	VI-5
TM7PR2L	0x03F7C	R/W	Timer 7 preset register 2 (lower 8 bits)	VI-6
TM7PR2H	0x03F7D	R/W	Timer 7 preset register 2 (upper 8 bits)	VI-7
TM7ICR	0x03FF0	R/W	Timer 7 interrupt control register	III-33
T7OC2ICR	0x03FF1	R/W	Timer 7 compare register 2 match interrupt control register	III-35
P1OMD	0x03F2B	R/W	Port 1 output mode register	IV-13
P1DIR	0x03F31	R/W	Port 1 direction control register	IV-13
PDOMD	0x03F1B	R/W	Port D output mode register	IV-109
PDDIR	0x03F3D	R/W	Port D direction control register	IV-108
TMSEL	0x03F3F	R/W	Timer I/O pin switching register	V-23

6.2.2 Programmable Timer Registers

Timer 7 has a set of 16-bit programmable timer registers, which contains a compare register, a preset register, a binary counter and a capture register. Each register has 2 sets of 8-bit register. Operate these registers by 16-bit access.

A compare register is a 16-bit register which stores comparative value of the compare register and the binary counter.

■ Timer 7 Compare Register 1 Lower 8 bits (TM7OC1L:0x03F72)

bp	7	6	5	4	3	2	1	0
Flag	TM7OC1L7	TM7OC1L6	TM7OC1L5	TM7OC1L4	TM7OC1L3	TM7OC1L2	TM7OC1L1	TM7OC1L0
At reset	X	X	X	X	X	X	X	X
Access	R	R	R	R	R	R	R	R

■ Timer 7 Compare Register 1 Upper 8 bits (TM7OC1H:0x03F73)

bp	7	6	5	4	3	2	1	0
Flag	TM7OC1H7	TM7OC1H6	TM7OC1H5	TM7OC1H4	TM7OC1H3	TM7OC1H2	TM7OC1H1	TM7OC1H0
At reset	X	X	X	X	X	X	X	X
Access	R	R	R	R	R	R	R	R

■ Timer 7 Compare Register 2 Lower 8 bits (TM7OC2L:0x03F7A)

bp	7	6	5	4	3	2	1	0
Flag	TM7OC2L7	TM7OC2L6	TM7OC2L5	TM7OC2L4	TM7OC2L3	TM7OC2L2	TM7OC2L1	TM7OC2L0
At reset	X	X	X	X	X	X	X	X
Access	R	R	R	R	R	R	R	R

■ Timer 7 Compare Register 2 Upper 8 bits (TM7OC2H:0x03F7B)

bp	7	6	5	4	3	2	1	0
Flag	TM7OC2H7	TM7OC2H6	TM7OC2H5	TM7OC2H4	TM7OC2H3	TM7OC2H2	TM7OC2H1	TM7OC2H0
At reset	X	X	X	X	X	X	X	X
Access	R	R	R	R	R	R	R	R

Timer 7 preset registers 1,2 are buffer registers of the compare registers 1,2 of timer 7. If the set value is written to the timer 7 preset registers 1,2 when the counting is stopped, the same set value is loaded to the timer 7 compare register. If set value is written to the timer 7 preset registers 1,2 during counting, the set value of the timer 7 preset registers 1,2 is loaded to the timer 7 compare registers 1,2 at the timing that the timer 7 binary counter is cleared.

■ Timer 7 Preset Register 1 Lower 8 bits (TM7PR1L:0x03F74)

bp	7	6	5	4	3	2	1	0
Flag	TM7PR1L7	TM7PR1L6	TM7PR1L5	TM7PR1L4	TM7PR1L3	TM7PR1L2	TM7PR1L1	TM7PR1L0
At reset	X	X	X	X	X	X	X	X
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

■ Timer 7 Preset Register 2 Upper 8 bits (TM7PR1H:0x03F75)

bp	7	6	5	4	3	2	1	0
Flag	TM7PR1H7	TM7PR1H6	TM7PR1H5	TM7PR1H4	TM7PR1H3	TM7PR1H2	TM7PR1H1	TM7PR1H0
At reset	X	X	X	X	X	X	X	X
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

■ Timer 7 Preset Register 2 lower 8 bits (TM7PR2L:0x03F7C)

bp	7	6	5	4	3	2	1	0
Flag	TM7PR2L7	TM7PR2L6	TM7PR2L5	TM7PR2L4	TM7PR2L3	TM7PR2L2	TM7PR2L1	TM7PR2L0
At reset	X	X	X	X	X	X	X	X
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

■ Timer 7 Preset Register 2 Upper 8 bits (TM7PR2H:0x03F7D)

bp	7	6	5	4	3	2	1	0
Flag	TM7PR2H7	TM7PR2H6	TM7PR2H5	TM7PR2H4	TM7PR2H3	TM7PR2H2	TM7PR2H1	TM7PR2H0
At reset	X	X	X	X	X	X	X	X
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Binary counter is a 16-bit up counter. If any data is written to a preset register when the counting is stopped, the binary counter is cleared to 0x0000.

■ Timer 7 Binary Counter Lower 8 bits (TM7BCL:0x03F70)

bp	7	6	5	4	3	2	1	0
Flag	TM7BCL7	TM7BCL6	TM7BCL5	TM7BCL4	TM7BCL3	TM7BCL2	TM7BCL1	TM7BCL0
At reset	X	X	X	X	X	X	X	X
Access	R	R	R	R	R	R	R	R

■ Timer 7 Binary Counter Upper 8 bits (TM7BCH:0x03F71)

bp	7	6	5	4	3	2	1	0
Flag	TM7BCH7	TM7BCH6	TM7BCH5	TM7BCH4	TM7BCH3	TM7BCH2	TM7BCH1	TM7BCH0
At reset	X	X	X	X	X	X	X	X
Access	R	R	R	R	R	R	R	R

Input capture register is a register that holds the value loaded from a binary counter by a capture trigger. A capture trigger is generated by an input signal from an external interrupt pin, and when an arbitrary value is written to an input capture register (Directly writing to the register by program is disabled.).

■ Timer 7 Input Capture Register Lower 8 bits (TM7ICL:0x03F76)

bp	7	6	5	4	3	2	1	0
Flag	TM7ICL7	TM7ICL6	TM7ICL5	TM7ICL4	TM7ICL3	TM7ICL2	TM7ICL1	TM7ICL0
At reset	X	X	X	X	X	X	X	X
Access	R	R	R	R	R	R	R	R

■ Timer 7 Input Capture Register Upper 8 bits (TM7ICH:0x3F77)

bp	7	6	5	4	3	2	1	0
Flag	TM7ICH7	TM7ICH6	TM7ICH5	TM7ICH4	TM7ICH3	TM7ICH2	TM7ICH1	TM7ICH0
At reset	X	X	X	X	X	X	X	X
Access	R	R	R	R	R	R	R	R

6.2.3 Timer Mode Registers

This is a readable/writable register that controls timer 7.

■ Timer 7 Mode Register 1(TM7MD1:0x03F78)

bp	7	6	5	4	3	2	1	0
Flag	Reserved	T7ICEDG1	TM7CL	TM7EN	TM7PS1	TM7PS0	TM7CK1	TM7CK0
At reset	0	0	1	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bp	Flag	Description
7	Reserved	Set always "0".
6	T7ICEDG1	Capture trigger edge selection 0:Falling edge 1:Rising edge
5	TM7CL	Timer output reset signal 0:Operate timer output 1:Disable timer output
4	TM7EN	Timer 7 count control 0:Halt the count 1:Operate the count
3-2	TM7PS1 TM7PS0	Count clock selection 00:1/1 of clock 01:1/2 of clock 10:1/4 of clock 11:1/16 of clock
1-0	TM7CK1 TM7CK0	Clock source selection 00:fosc 01:fs 10:TM7IO input 11:Synchronous TM7IO input

■ Timer 7 Mode Register 2(TM7MD2:0x03F79)

bp	7	6	5	4	3	2	1	0
Flag	T7ICEDG0	T7PWMSL	TM7BCR	TM7PWM	TM7IRS1	T7ICEN	T7ICT1	T7ICT0
At reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bp	Flag	Description
7	T7ICEDG0	Capture trigger edge selection 0:Select the both edges 1:Select the specified edge
6	T7PWMSL	PWM mode selection 0:Set duty by OC1 1:Set duty by OC2
5	TM7BCR	Timer 7 count clear factor selection 0:Full count OVF 1:Match of BC and OC1
4	TM7PWM	Timer output waveform selection 0:Output timer 1:Output PWM
3	TM7IRS1	Timer 7 interrupt factor selection 0:Counter clear 1:Match of BC and OC1
2	T7ICEN	Input capture operation enable flag 0:Disable capture operation 1:Enable capture operation
1-0	T7ICT1 T7ICT0	Capture trigger selection 00:External interrupt 0 input signal P20/IRQ0 input signal 01:External interrupt 1 input signal P21/IRQ1 input signal 10:External interrupt 2 input signal P22/IRQ2A (PD0/IRQ2B) input signal 11:External interrupt 3 input signal P23/IRQ3A (PD1/IRQ3B) input signal

■ Timer I/O Pin Switching Control Register (TMSEL:0x03F3F)

bp	7	6	5	4	3	2	1	0
Flag	-	TM7SEL	TM5SEL	TM4SEL	-	-	-	-
At reset	-	0	0	0	-	-	-	-
Access	-	R/W	R/W	R/W	-	-	-	-

bp	Flag	Description
7	-	-
6	TM7SEL	Timer 7 I/O pin switching 0:P16/TM7IOA 1:PD4/TM7IOB
5	TM5SEL	Timer 5 I/O pin switching 0:P15/TM5IOA 1:PD3/TM5IOB
4	TM4SEL	Timer 4 I/O pin switching 0:P14/TM4IOA 1:PD2/TM4IOB
3-0	-	-

■ External Interrupt Pin Switching Control Register (IRQSEL:0x03F4E)

bp	7	6	5	4	3	2	1	0
Flag	-	-	-	-	IRQ3SEL	IRQ2SEL	-	-
At reset	-	-	-	-	0	0	-	-
Access	-	-	-	-	R/W	R/W	-	-

bp	Flag	Description
7-4	-	-
3	IRQ3SEL	External interrupt 3 input pin switching 0:P23 1:PD1
2	IRQ2SEL	External interrupt 2 input pin switching 0:P22 1:PD0
1-0	-	-

6.3 Operation

6.3.1 Operation

The timer operation can constantly generate interrupts.

■ 16-bit Timer Operation (Timer 7)

The generation cycle of an timer interrupt is set by the clock source selection and the set value of the compare register 1 (TM7OC1), in advance. When the binary counter (TM7BC) reaches the set value of the compare register 1, the timer 7 interrupt request is generated at the next count clock. There are 2 sources ; the TM7OC1 compare match or the full count over flow, to be selected to clear the binary counter. After the binary counter is cleared to 0x0000, the counting up is restarted from 0x0000.

Table:6.3.1 16-bit Timer Interrupt Source and Binary Counter Clear Source (Timer 7)

TM7MD2 register		Interrupt source	Binary counter clear source
TM7IRS1 flag	TM7BCR flag		
1	1	TM7OC1 compare match	TM7OC1 compare match
0	1	TM7OC1 compare match	TM7OC1 compare match
1	0	TM7OC1 compare match	Full count overflow
0	0	Full count overflow	Full count overflow

Timer 7 can generate another set of an independent interrupt (Timer 7 compare register 2 match interrupt) by the set value of the Timer 7 compare register (TM7OC2).At that timer, the binary counter is cleared as the above setup.

The compare register is double buffer type. So, when the value of the preset registers is changed during the counting, the changed value is stored to the compare register when the binary counter is cleared. This function can change the compare register value constantly, without disturbing the cycle during timer operation (Reload function).

When the CPU reads the 16-bit binary counter (TM7BC), the read data is handled in 8-bits units even if it is a 16-bit MOVW instruction. As a result, it will read the data incorrectly if a carry from the lower 8 bits to the upper 8 bits occurs during counting operation. To read the correct value of the 16-bit counting (TM7BC), use the writing program function to the input capture register (TM7IC). By writing to the TM7IC, the counting data of TM7BC can be stored to TM7IC to read out the correct counting value during timer operation.
[chapter 6.9.1. Operation]

To count properly, do not switch the count clock on the timer operation. To switch the count clock, stop the timer operation.

Table:6.3.2 shows the clock source that can be selected.

Table:6.3.2 Clock Source at Timer Operation (Timer 7)

Clock source	1count time
fosc	50 ns
fosc/2	100 ns
fosc/4	200 ns
fosc/16	800 ns
fs	100 ns
fs/2	200 ns
fs/4	400 ns
fs/16	1.6 µs
fosc=20 MHz,fs=fosc/2=10 MHz	

■ Count Timing of Timer Operation (Timer 7)

The binary counter counts up with the selected clock source as the count clock. The basic operation of whole 16-bit timer functions is as below.

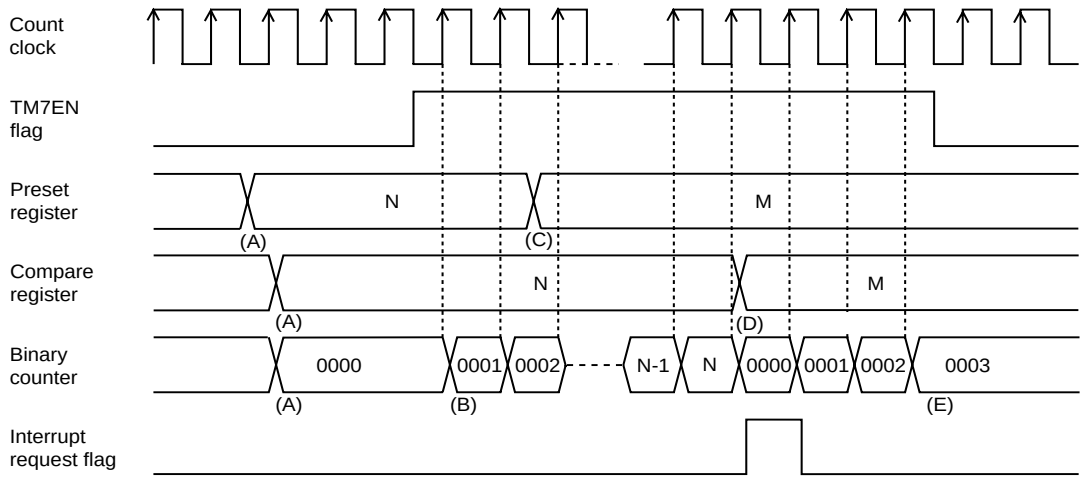


Figure:6.3.1 Count Timing of Timer Operation (Timer 7)

- (A)When a data is written to the preset register while the TM7EN flag is stopped ("0"), the same value is loaded during the writing cycle and the binary counter is cleared to 0x0000.
- (B)When TM7EN flag is ("1"), the binary counter starts counting. The counting starts at the rising edge of the count clock.
- (C)Even if the preset register is rewritten when the TM7EN flag is ("1"), the binary counter is not changed.
- (D)When the binary counter reaches value of compare register 1, the set value of the preset register is loaded to the compare register at the next count clock. And the interrupt request flag is set at the next count clock, and the binary counter is cleared to 0x0000 to restart counting up.
- (E)When the TM7EN flag is ("1"), the binary counter is stopped.

When the binary counter reaches the value of the compare register, the interrupt request flag is set at the next count clock, and the binary counter is cleared. So, set the compare register as:
(the set value of the compare register) = (the counts till the interrupt generation - 1)

When the timer 7 compare register 2 match interrupt is generated and the TM7OC1 compare match is selected as a binary counter clear source, the set value of the compare register 2 should be smaller than the set value of the compare register 1.

On the interrupt service routine, clear the timer interrupt request flag before the timer is started.

When the binary counter is used as a free-counter that counts 0x0000 to 0xFFFF, set 0xFFFF to the compare register or set the TM7BCR flag of the TM7MD2 register to "0".

Setup of 16-bit timer count clock should be done when the timer interrupt is disabled.

6.3.2 Setup Example

■ Timer Operation Setup Example

Timer 7 generates an interrupt constantly for timer function. Fosc/2 (fosc=20 MHz at operation) is selected as a clock source to generate an interrupt every 1000 cycles (100 ms).

An example setup procedure, with a description of each step is shown below.

Setup Procedure	Description
(1) Stop the counter TM7MD1(0x03F78) bp4 :TM7EN =0	(1) Set the TM7EN flag of the timer 7 mode register 1 (TM7MD) to "0" to stop the timer 7 counting.
(2) Disable the interrupt TM7ICR(0x03FF0) bp1 :TM7IE =0	(2) Set the TM7IE flag of the TM7CIR register to "0" to disable the interrupt.
(3) Select the timer clear source TM7MD2(0x03F79) bp5 :TM7BCR =1	(3) Set the TM7BCR flag of the timer 7 mode register 2 (TM7MD2) to "1" to select the compare match to the binary counter clear source.
(4) Select the count clock source TM7MD1 (0x03F78) bp1-0 :TM7CK1-0 =00 bp3-2 :TM7PS1-0 =01	(4) Select fosc to the clock source by the TM7CK1 to 0 flag of the TM7MD1 register. Besides, select 1/2 fosc to the count clock source by the TM7PS1 to 0 flag.
(5) Set the interrupt generation cycle TM7PR1(0x03F75,0x03F74) =0x03E7	(5) Set the interrupt generation cycle to the timer 7 preset register 1 (TM7PR1). The cycle is 1000. The set value should be 1000-1=999 (0x03E7). At the time, the same value is loaded to the timer 7 compare register 1 (TM7OC1), and the timer 7 binary counter (TM7BC) is initialized to 0x0000.
(6) Set the interrupt level TM7ICR(0x03FF0) bp7-6 :TM7LV1-0 =10	(6) Set the interrupt level by the TM7LV1 to 0 flag of the timer 7 interrupt control register (TM7ICR). If the interrupt request flag is already set, clear the request flag. [Chapter 3 3.1.4. Interrupt Flag Setup]
(7) Enable the interrupt TM7ICR (0x03FF0) bp1 :TM7IE =1	(7) Set the TM7IC flag of the TM7ICR register to "1" to enable the interrupt.
(8) Start the timer operation TM7MD1 (0x03F78) bp4 :TM7EN =1	(8) Set the TM7EN flag of the TM7MD1 register to "1" to operate the timer 7.

TM7BC counts up from 0x0000. When TM7BC reaches the set value of the TM7OC1 register, the timer 7 interrupt request flag is set at the next count clock and the TM7BC becomes 0x0000 and counts up again.

When the TM7EN flag of the TM7MD register is changed with other bits, the binary counter may count up by switching operation.

6.4 16-bit Event Count

6.4.1 Operation

Event count operation has 2 types;TM7IO input and synchronous TM7IO input. These can be selected as the count clock. Each type can select 1/1, 1/2, 1/4, 1/16 or 1/128 as a count clock source. Also, it is possible to select the count edge. (the falling edge and the both edge at the normal operation are selectable)

■ 16-bit Event Count Operation (Timer 7)

The binary counter (TM7BC) counts the external signal input to the TM7IO pin. If the binary counter reaches the set value of the compare register (TM7OC), an interrupt can be generated at the next count clock.

Table:6.4.1 Event Count Input Clock

	Timer 7
Event input	TM7IO input (P16, PD4)
	Synchronous TM7IO input

■ Count Timing of TM7IO Input

When TM7IO input is selected, TM7IO input signal is input to the timer 7 count clock. The binary counter counts up at the falling edge of the TM7IO input signal or TM7IO input signal that passed the divider.

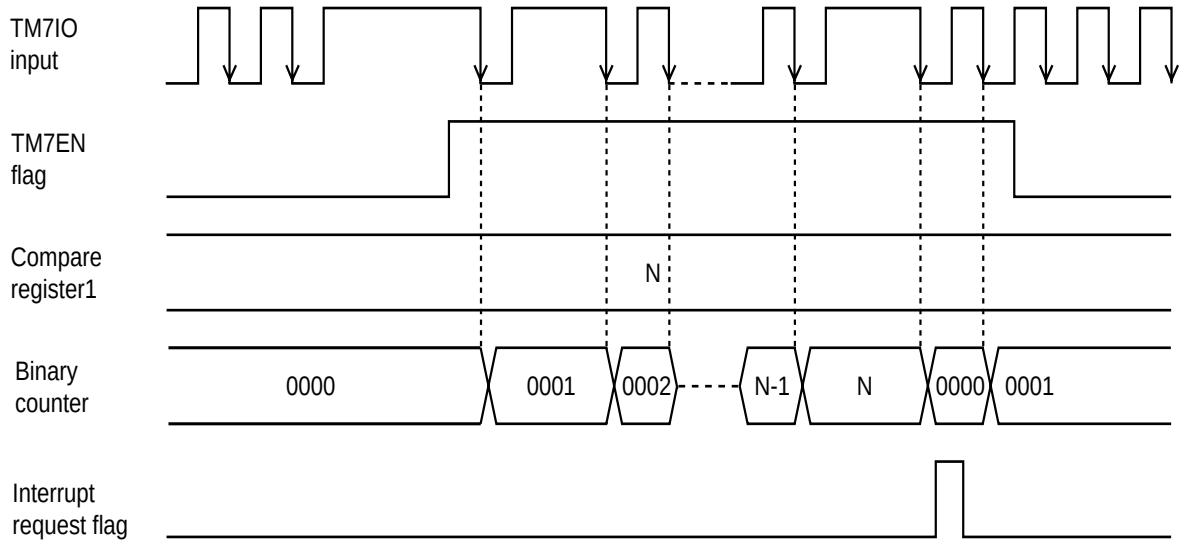


Figure:6.4.1 Count Timing TM7IO Input (Timer 7)

If the binary counter is read out during operation, incorrect data at counting up may be read. And when the timer stops, unexpected data may be read at the binary counter. To prevent this, use the event count by the synchronous TM7IO input, which is shown in the following page.

When the event input (TM7IO input) is used, clear the binary counter before the timer operation. Also, when the compare register is set to 0x0000, use the event count by the synchronous TM7IO input,as shown below.

■ Count Timing of Synchronous TM7IO Input (Timer 7)

If the synchronous TM7IO input is selected, the synchronizing circuit output signal is input to the timer 7 count clock. The synchronizing circuit output signal is changed at the falling edge of the system clock after the TM7IO input signal is changed. The binary counter counts up at the falling edge of the synchronizing circuit output signal or the synchronizing circuit output signal that passed through the division circuit.

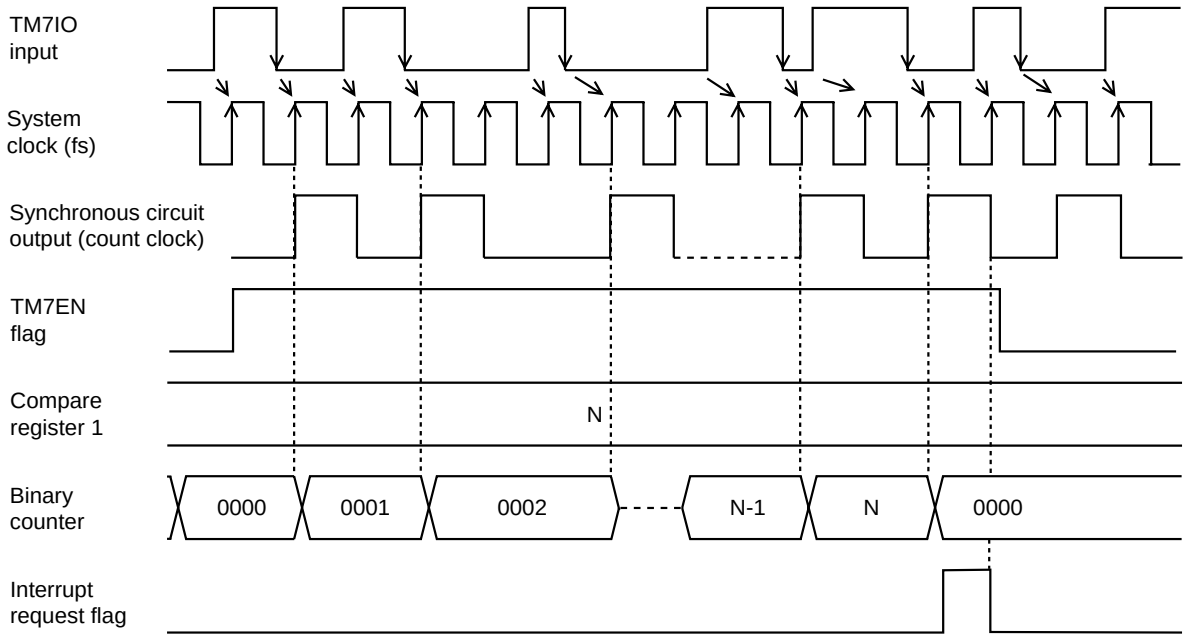


Figure:6.4.2 Count Timing of Synchronous TM7IO Input (Timer 7)

The timer 7 binary counter counts up the binary counter at the signal in synchronization with the system clock so that correct value is read out from the timer 7 binary counter.

When TM7IO input is used, select fs as a count clock, set the value to the TM7PR1 register, then select the TM7IO input. And the value is not writable at the preset register during the operation. At 16 bit timer, only TM7IO input can be returned from STOP mode.

6.4.2 Setup Example

■ Event Count Setup Example

When the falling edge of the TM7IO input pin signal is detected 5 times using Timer 7, an interrupt is generated.

An example setup procedure, with a description of each step is shown below.

Setup Procedure	Description
(1) Stop the counter TM7MD1 (0x03F78) bp4:TM7EN =0	(1) Set the TM7EN flag of the Timer 7 mode register 1 (TM7MD1) to "0" to stop the Timer 7 counting.
(2) Disable the interrupt TM7ICR(0x03FF0) bp1:TM7IE =0	(2) Set the TM7IE flag of the TM7ICR register to "0 "to disable the interrupt.
(3) Select the pin TMSEL(0x03F3F) bp6:TM7SEL =0	(3) Switch the timer I/O pin Set the TM7SEL flag of the TMSEL register to "0 " to select the TM7IOA as the input pin.
(4) Set the special function pin to input P1DIR (0x03F31) bp6 :P1DIR6 =0	(4) Set the P1DIR6 flag of the port 1 direction control register (P1DIR) to "0" to set P16 pin to the input mode. Add pull-up/pull-down resistor, if necessary. [Chapter 4 I/O ports]
(5) Select the count clock source TM7MD1(0x03F78) bp1-0:TM7CK1-0 =01 bp3-2:TM7PS1-0 =00	(5) Select fs to the clock source by the TM7CK1 to 0 flag of the TM7MD1 register. Besides, select 1/1 to the count clock source by the TM7PS1 to 0 flag.
(6) Set the interrupt generation cycle TM7PR1(0x03F75,0x03F74) =0x0004	(6) Set the interrupt generation cycle to the Timer 7 preset register 1 (TM7PR1). The set value should be 4, because the counting is 5 times. At that time, the same value is loaded to the Timer 7 compare register 1 (TM7OC1), and the Timer 7 binary counter (TM7BC) is initialized to 0x0000.
(7) Select the timer clear source TM7MD2 (0x03F79) bp5:TM7BCR =1	(7) Set the TM7BCR flag of the Timer 7 mode register 2 (TM7MD2) to "1" to select the compare match as a binary counter clear source.
(8) Select the count clock source TM7MD1 (0x03F78) bp1-0:TM7CK1-0 =10 bp3-2:TM7PS1-0 =00	(8) Select TM7IO to the clock source by the TM7CK1 to 0 flag of the TM7MD1 register. Besides, select 1/1(no dividing) to the count clock source by the TM7PS1 to 0 flag.
(9) Set the interrupt level TM7ICR (0x03FF0) bp7-6:TM7LV1-0 =10	(9) Set the interrupt level by the TM7LV1 to 0 flag of the Timer 7 interrupt control register (TM7ICR). If the interrupt request flag is already set, clear the request flag. [Chapter 3 3.1.4. Interrupt Flag Setup]

Setup Procedure	Description
(10) Enable the interrupt TM7ICR (0x03FF0) bp1:TM7IE =1	(10) Set the TM7IE flag of the TM7ICR register to "1" to enable the interrupt.
(11) Start the event count TM7MD1 (0x03F78) bp4:TM7EN =1	(11) Set the TM7EN flag of the TM7MD1 register to "1" to operate the Timer 7.

Every time TM7BC reaches the falling edge of the TM7IO input, it counts up from 0x0000. When the TM7BC reaches the set value of the TM7OC1 register, the Timer 7 interrupt request flag is set at the next count clock, and the value of TM7BC becomes 0x0000 to restart counting up.

In case the procedure of the step (5) to (8), the timer may be operated imperfectly.

6.5 16-bit Timer Pulse Output

6.5.1 Operation

TM7IO pin can output a pulse signal with a arbitrary frequency.

■ 16-bit Timer Pulse Output Operation (Timer 7)

These timers can output 2 × cycle signal, compared with the set value of the compare register 1 (TM7OC1) and the 16-bit full count. Output pins are as follows.

Table:6.5.1 Timer Pulse Output Pin

	Timer 7
Pulse output pin	TM7IO output (P16, PD4)

Table:6.5.2 shows the timer interrupt generation sources and the flags that control the timer pulse output cycle.

Table:6.5.2 16-bit Timer Interrupt Generation Source and Timer Pulse Output Cycle (Timer 7)

TM7MD2 register		Interrupt source	Timer pulse output cycle
TM7IRS1 flag	TM7BCR flag		
1	1	TM7OC1 compare match	Set value of TM7OC1 × 2
0	1	TM7OC1 compare match	Set value of TM7OC1 × 2
1	0	TM7OC1 compare match	Full count of TM7BC × 2
0	0	Full count over flow	Full count of TM7BC × 2

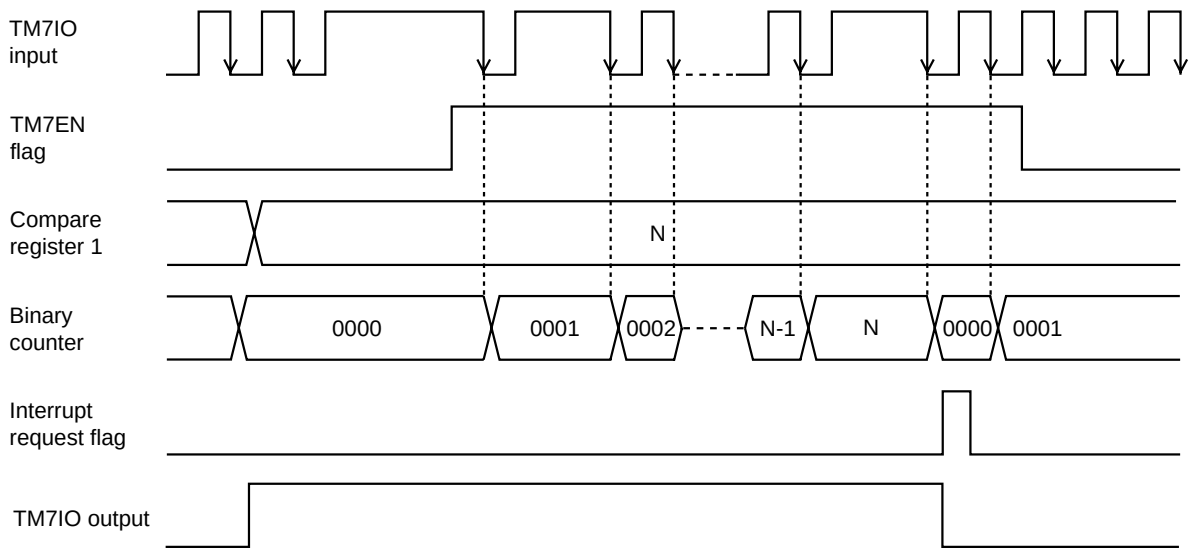


Figure:6.5.1 Count Timing of Timer Pulse Output (Timer 7)

TM7IO output pin outputs 2 × cycle, compared with the value of the compare register 1. If the binary counter reaches the compare value or full count overflow is occurred, the binary counter is cleared to 0x0000, and the TM7IO output (timer output) is inverted.

In the initial state after releasing reset, the timer pulse output is reset, and low output is fixed. Therefore, release the reset of the timer pulse output by setting the TM7CL flag of the TM7MD1 register to "0".

Reset release of the timer pulse output should be done when the timer count is stopped.

When the prescaler is operated by the timer pulse output, set the prescaler dividing rate after the reset release of the timer pulse output.

6.5.2 Setup Example

■ Timer Pulse Output Setup Example

TM7IO output pin outputs a 50 kHz pulse using Timer 7. For this, select fosc as the clock source and set 2x cycle (100 kHz) to the Timer 7 compare register (at fosc=20 MHz).

An example setup procedure, with a description of each step is shown below.

Setup Procedure	Description
(1) Stop the counting TM7MD1 (0x03F78) bp4:TM7EN =0	(1) Set the TM7EN flag of the Timer 7 mode register 1 (TM7MD1) to "0" to stop the Timer 7 counting.
(2) Select the pin TMSEL (0x03F3F) bp6:TM7SEL =0	(2) Switch the timer I/O pin Set the TM7SEL flag of the TMSEL register to "0 " to select the TM7I0A as the input pin.
(3) Set the special function pin P1OMD (0x03F2B) bp6 :P1OMD6 =1 P1DIR (0x03F31) bp6 :P1DIR6 =1	(3) Set the P1OMD6 flag of the port 1 output mode register (P1OMD) to "1" to set P16 as the special function pin. Set the P1DIR6 flag of the port 1 direction control register (P1DIR) to "1" to set the output mode. [Chapter 4 I/O Ports]
(4) Set the timer pulse output TM7MD2 (0x03F79) bp4:TM7PWM =0	(4) Set TM7PWM flag of TM7MD2 register to "0" to select the timer pulse output.
(5) Release the reset of the timer pulse TM7MD1 (0x03F78) bp5:TM7CL =0	(5) Set the TM7CL flag of the TM7MD1 register to "0" to enable the pulse output.
(6) Select the timer clear source TM7MD2 (0x03F79) bp5:TM7BCR =1	(6) Set the TM7BCR flag of the TM7MD2 register to "1" to select the compare match as the binary counter clear source.
(7) Select the count clock source TM7MD1 (0x03F78) bp1-0:TM7CK1-0 =00 bp3-2:TM7PS1-0 =00	(7) Select fosc as the clock source by the TM7CK1 to 0 flag of the TM7MD1 register. Also, select 1/1 dividing as the clock source by the TM7PS1 to 0 flag.
(8) Set the timer pulse output generation cycle TM7PR1(0x03F75,0x03F74) =x00C7	(8) Set 1/2 of the timer pulse output cycle to the Timer 7 preset register 1 (TM7PR1). To set 100 kHz by dividing 20 MHz, set as; 200-1=199 (0xC7) At the same time, the same value is loaded to the Timer 7 compare register 1 (TM7BC) and the Timer 7 binary counter (TM7BC) is initialized to 0x0000.
(9) Start the timer operation TM7MD1 (0x03F78) bp4:TM7EN =1	(9) Set the TM7EN flag of the TM7MD1 register to "1" to operate the Timer 7.

TM7BC counts up from 0x0000. If TM7BC reaches the set value of the TM7OC1 register and TM7BC is cleared to 0x0000, the signal of the TM7IO output is inverted and TM7BC counts up from 0x0000 again.

Regardless of whether the binary counter is stopped or operated, the timer output is "L", when the TM7CL flag of the TM7MD1 register is set to "1".

6.6 16-bit Standard PWM Output (Only duty can be changed consecutively)

TM7IO pin outputs the standard PWM output, which is determined by the overflow timing of the binary counter, and the match timing of the timer binary counter and the compare register.

6.6.1 Operation

■ 16-bit Standard PWM Output (Timer 7)

PWM waveform with an arbitrary duty is generated by setting a duty of PWM "H" period to the compare register 1 (TMnOC1). Its cycle is the time of the 16-bit timer full count overflow.

Table:6.6.1 shows the PWM output pin.

Table:6.6.1 PWM output pin

	Timer 7
Pulse output pin	TM7IO output (P16, PD4)

■ Count Timing of Standard PWM Output (at Normal) (Timer 7)

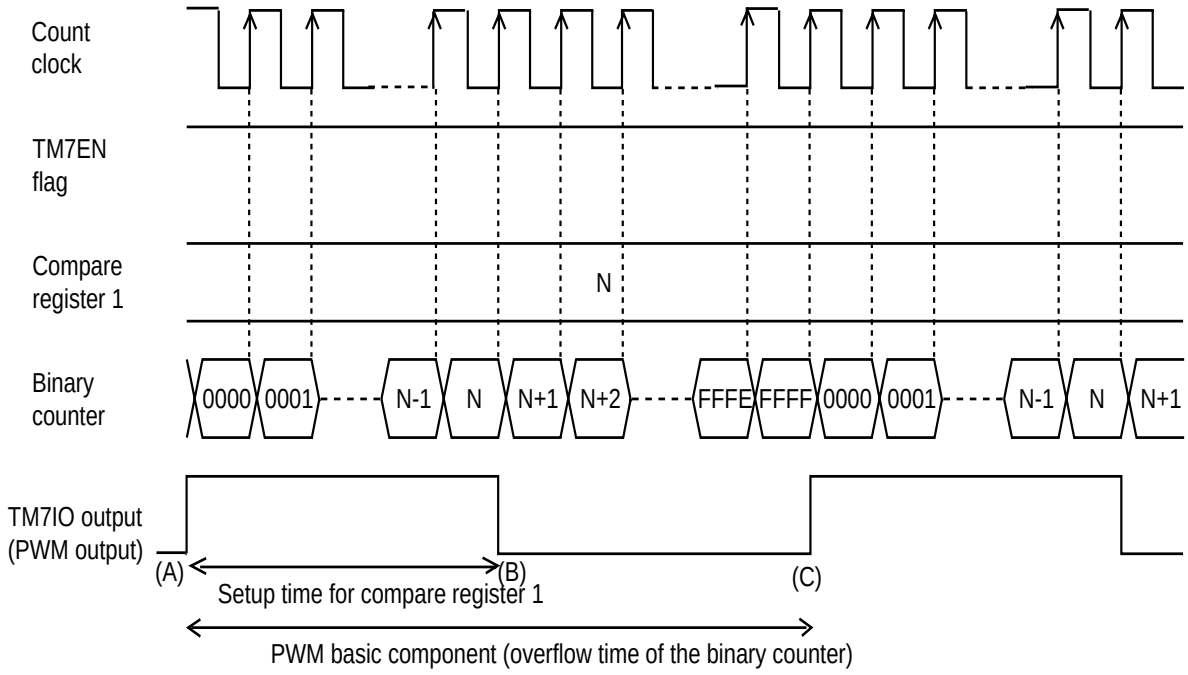


Figure:6.6.1 Count Timing of Standard PWM Output (at Normal)

PWM source waveform,

- (A)shows "H" until the binary counter reaches the compare register value from 0x0000.
- (B)shows "L" after the compare match, then the binary counter counts up till the overflow.
- (C)shows "H" again if the binary counter overflow.

■ Count Timing of Standard PWM Output (when compare register 1 is 0x0000) (Timer 7)

Here is the count timing at setting 0x0000 to the compare register 1.

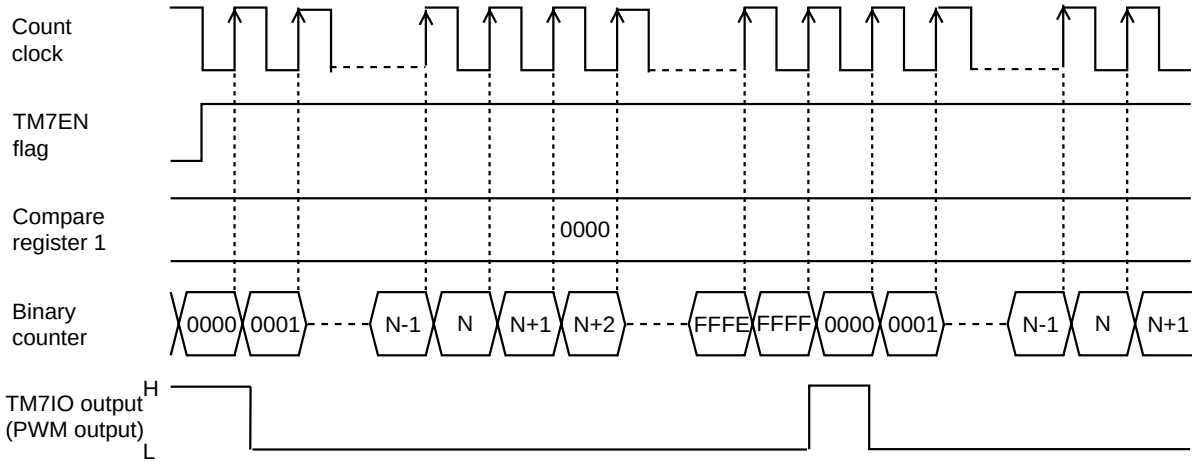


Figure:6.6.2 Count Timing of Standard PWM Output (when compare register 1 is 0x0000)

PWM output shows "H", when TM7EN flag is stopped (at "0").

■ Count Timing of Standard PWM Output (when compare register 1 is 0xFFFF) (Timer 7)

Here is the count timing at setting 0xFFFF to the compare register 1.

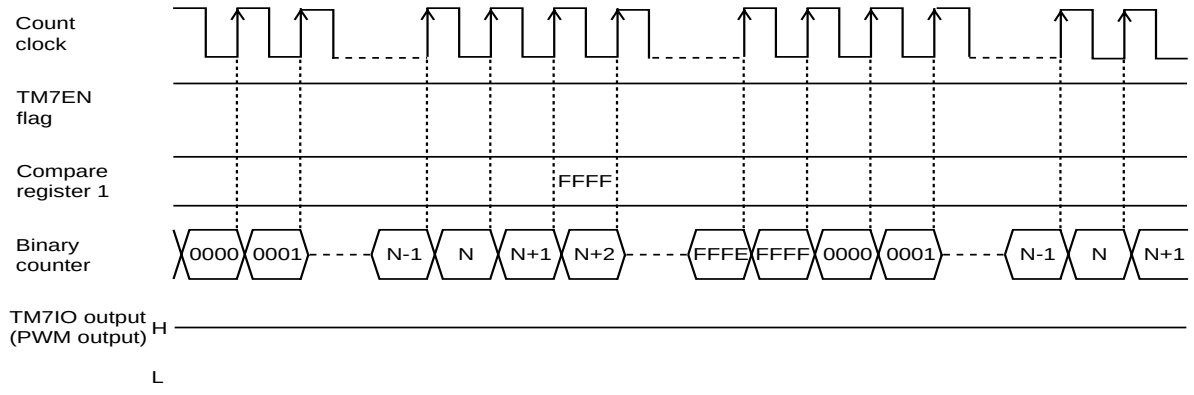


Figure:6.6.3 Count Timing of Standard PWM Output (when compare register 1 is 0xFFFF)

To output the standard PWM output, set the TM7BCR flag of the TM7MD2 register to "0" to select the full count overflow as the binary counter clear source and the PWM output set ("H" output) source.

The TM7OC1 compare match or the TM7OC2 compare match can be selected as a PWM output reset ("L" output) source with the T7PWMSL flag of the TM7MD2 register.

6.6.2 Setup Example

■ Standard PWM Output Setup Example

The TM7IO output pin outputs the 1/4 duty PWM output waveform at 305.18 Hz with the timer 7 (at the high frequency oscillation, fosc=20 MHz). One cycle of the PWM output waveform is decided by the overflow of the binary counter. "H" period of the PWM output waveform is decided by the set value of the compare register 1.

An example setup procedure, with a description of each step is shown below.

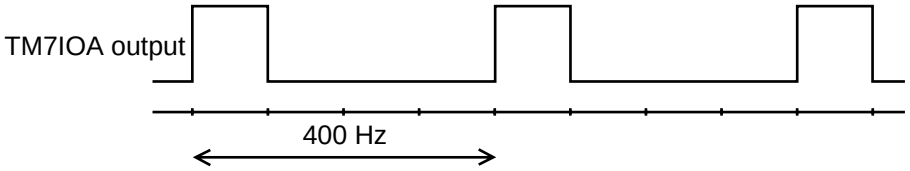


Figure:6.6.4 Waveform of TM7IOA output pin

Setup Procedure	Description
(1) Stop the counter TM7MD1 (0x3F78) bp4 :TM7EN =0	(1) Set the TM7EN flag of the timer 7 mode register 1(TM7MD1) to "0" to stop the timer 7 counting.
(2) Select the pin TMSEL (0x03F3F) bp6:TM7SEL =0	(2) Switch the timer I/O pin Set the TM7SEL flag of the TMSEL register to "0 " toselect the TM7I0A as the input pin.
(3) Set the special function pin to output P1OMD (0x03F2B) bp6 :P1OMD6 =1 P1DIR (0x03F31) bp6 :P1DIR6 =1	(3) Set the P1OMD6 flag of the port 1 output mode register(P1OMD) to "1" to set the P16 pin as aspecial function pin. Set the P1DIR6 flag of the port 1 direction control register(P1DIR) to "1" to set the output mode. [Chapter 4 I/O Ports]
(4) Set the PWM output TM7MD2 (0x3F79) bp4 :TM7PWM =1	(4) Set the TM7PWM flag of the timer 7 mode register 2 (TM7MD2) to "1" to select the PWM output.
(5) Set the standard PWM output TM7MD2 (0x3F79) bp5 :TM7BCR =0	(5) Set the TM7BCR flag of the TM7MD2 register to "0" to select the full count overflow as the binary counter clear source.
(6) Select the count clock source TM7MD1 (0x3F78) bp1-0 :TM7CK1-0 =00 bp3-2 :TM7PS1-0 =00	(6) Select fosc as the clock source by the TM7CK1 to 0 flag of the TM7MD1 register. Also, select 1/1 dividing as the count clock source by the TM7PS1 to 0 flag.

Setup Procedure	Description
(7) Set "H" period of the PWM output TM7PR1(0x3F75,0x3F74)=0x4000	(7) Set "H" period of the PWM output to the timer 7 preset register 1 (TM7PR1). To set 1/4 duty of the full count 65536,set as; 65536/4-1=16383(0x03FFF) At the same time, the same value is loaded to the timer 7 compare register 1(TM7OC1) and the timer 7 binary counter(TM7BC) is initialized to 0x0000.
(8) Start the timer operation TM7MD1 (0x3F78) bp4 :TM7EN =1	(8) Set the TM7EN flag of the TM7MD1 register to "1" to operate the timer 7.

TM7BC counts up from 0x0000. The PWM source waveform outputs "H" until TM7BC reaches the set value of the TM7OC1 register, then after the match it outputs "L". After that, TM7BC continues to count up. Once a overflow occurs, the PWM source waveform outputs "H" again, and TM7BC counts up from 0x0000, again.

In the initial state of the PWM output, it is changed to "H" output from "L" output at the timing that the PWM operation is selected with the TM7PWM flag of the TM7MD register.

6.7 16-bit High Precision PWM Output (Cycle/Duty can be changed consecutively)

The TM7IO pin outputs high precision PWM output, which is determined by the match timing of the timer binary counter and the compare register 1, and match timing of the binary counter and the compare register 2.

6.7.1 Operation

■ 16-bit High Precision PWM Output Operation (Timer 7)

The PWM waveform of any cycle/duty is generated by setting the cycle of PWM to the compare register 1 (TM7OC1) and setting the duty of the "H" period to the compare register 2 (TM7OC2).

■ Count Timing of High Precision PWM Output (at Normal) (Timer 7)

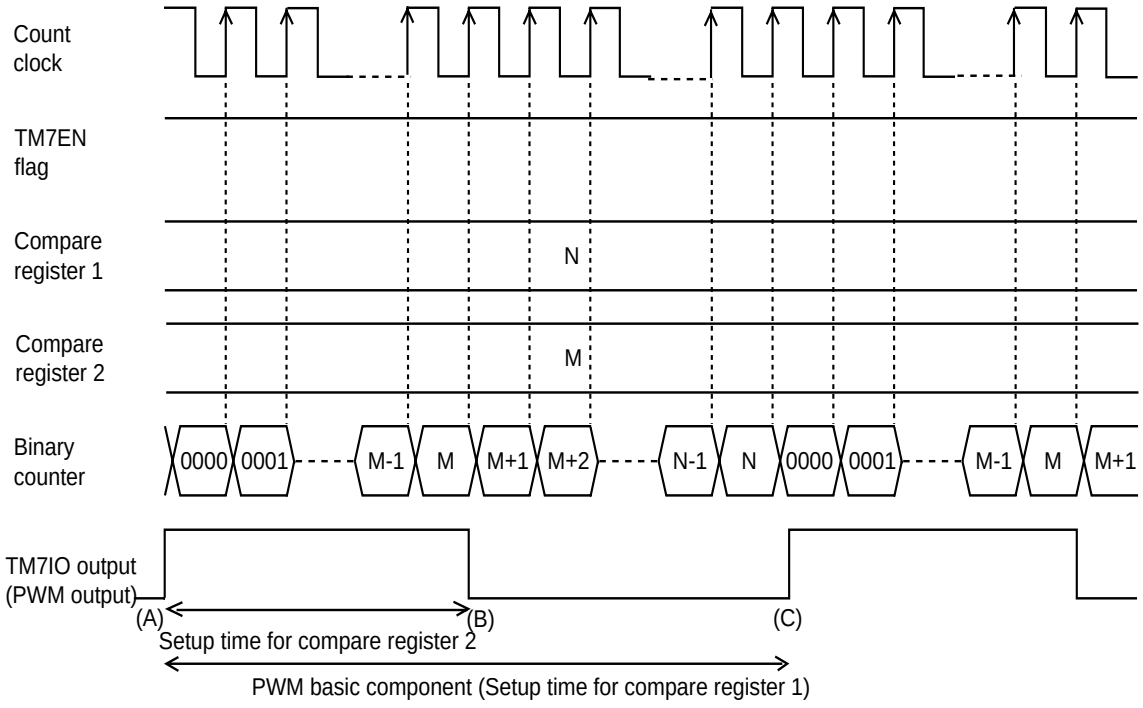


Figure:6.7.1 Count Timing of High Precision PWM Output (at Normal)

PWM source waveform,

- (A)shows "H" until the binary counter reaches the compare register from 0x0000.
- (B)shows "L" after the TM7OC2 compare match, the binary counter then counts up until the binary counter reaches the TM7OC1 compare register is cleared.
- (C)shows "H" again, when the binary counter is cleared.

■ Count Timing of High Precision PWM Output (When the compare register 2 is 0x0000) (Timer 7)

Here is the count timing as the compare register 2 is set to 0x0000.

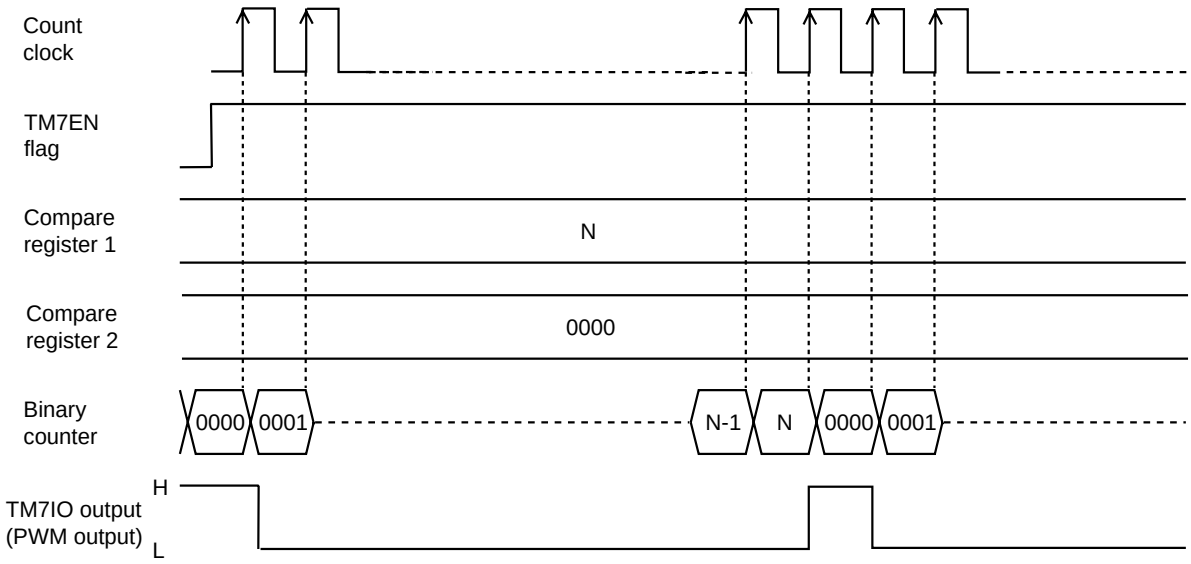


Figure:6.7.2 Count Timing of High Precision PWM Output (When the compare register 2 is 0x0000)

When the TM7EN flag is stopped (at "0"), the PWM output shows "H".

■ Count Timing of High Precision PWM Output (At the compare register 2 = the compere register 1-1) (Timer 7)

Count timng: Compare register 2 = Compare register 1 - 1 is shown below.

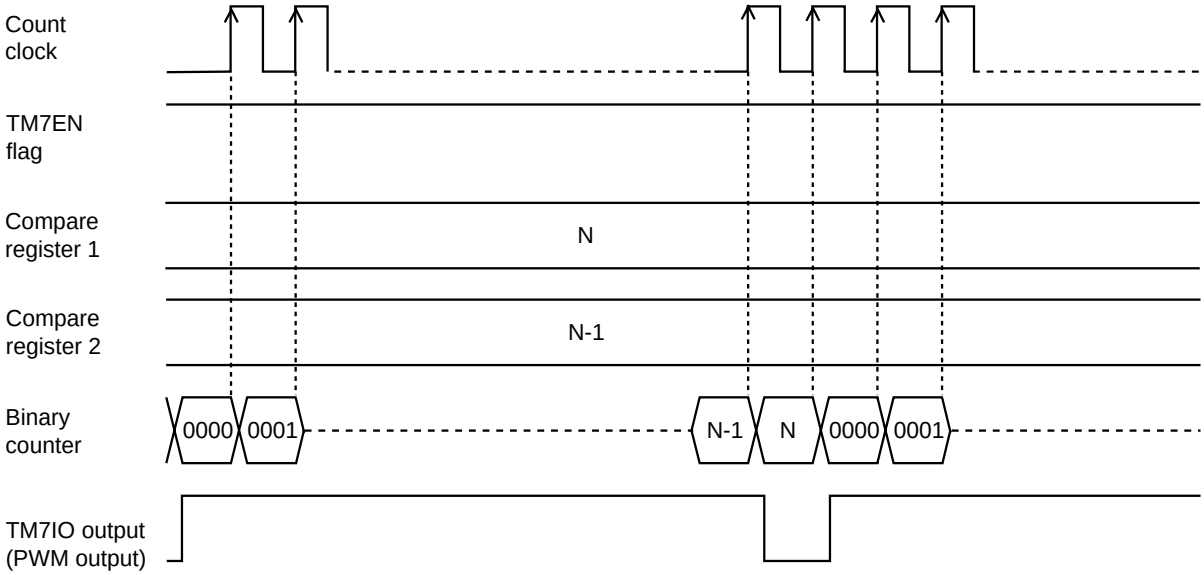


Figure:6.7.3 Count Timing of High Precision PWM Output (At the compare register 2 = the compere register 1-1)

To output the high precision PWM output, set the TM7BCR flag of the TM7MD2 register to "1" to select the TM7OC1 compare match as the clear source for the binary counter, and the set ("H" output) source of the PWM output.
Also, set the T7PWMLS flag to "1" to select the TM7OC2 compare match as the reset ("L" output) source of the PWM output.

6.7.2 Setup Example

■ High Precision PWM Output Setup Example (Timer 7)

The TM7IO output pin outputs the 1/4 duty PWM output waveform at 400 Hz with the timer 7. Select fosc/2 (at fosc=10 MHz) as the clock source. One cycle of the PWM output waveform is decided by the set value of the compare register 1. "H" period of the PWM output waveform is decided by the set value of the compare register 2. An example setup procedure, with a description of each step is shown below.

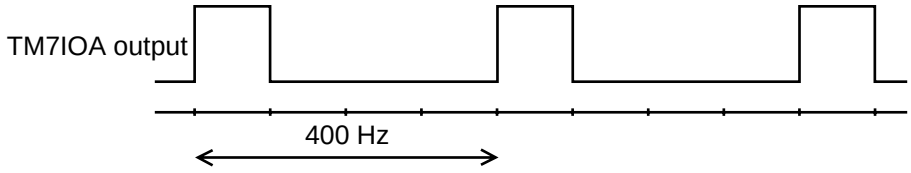


Figure:6.7.4 Waveform of TM7IOA Output Pin

Setup Procedure	Description
(1) Stop the counter TM7MD1(0x03F78) bp4 :TM7EN =0	(1) Set the TM7EN flag of the timer 7 mode register 1 (TM7MD1) to "0" to stop the timer 7 counting.
(2) Select the pin TMSEL(0x03F3F) bp6 :TM7SEL=0	(2) Timer I/O pin switching Set TM7SEL flag of the register(TMSEL) to “0“ and select TM7IOA as the output pin.
(3) Set the special function pin to output P1OMD (0x03F2B) bp6 :P1OMD6 =1 P1DIR (0x03F31) bp6 :P1DIR6 =1	(3) Set the P1OMD6 flag of the port P1 output mode register (P1OMD) to "1" to set P16 pin as the special function pin. Set the P1DIR6 flag of the port P1 direction control register (P1DIR) to "1" to set the output mode. [Chapter 4 I/O Ports]
(4) Set the PWM output TM7MD2(0x03F79) bp4 :TM7PWM =1	(4) Set the TM7PWM flag of the timer 7 mode register 2 (TM7MD2) to "1" to select the PWM output.
(5) Set the high precision PWM output TM7MD2(0x03F79) bp5 :TM7BCR =1 bp6 :T7PWMSL =1	(5) Set the TM7BCR flag of the TM7MD2 register to "1" to select the TM7OC1 compare match as the binary counter clear decision. And set the T7WMSL flag to "1" to select the TM7OC2 compare match as the duty decision source of the PWM output.
(6) Select the count clock source TM7MD1(0x03F78) bp1-0 :TM7CK1-0 =00 bp3-2 :TM7PS1-0 =01	(6) Select fosc as the clock source by the TM7CK1 to 0 flag of the TM7MD1 register. Also, select 1/2 dividing as the count clock source by TM7PS1 to 0 flag.

Setup Procedure	Description
(7) Set the PWM output cycle TM7PR1(0x03F75,0x03F74) =0x61a7	(7) Set the value of PWM out put cycle to timer 7 preset register 1 (TM7PR1). To set 400 Hz by dividing 10 MHz, set as; 25000-1=24999 (0x61a7) At the same time, the same value is loaded to the timer 7 compare register 1 (TM7OC1), the timer 7 binary counter is initialized to 0x0000.
(8) Set the "H" period of the PWM output TM7PR2(0x03F7D,0x03F7C) =0x1869	(8) Set "H" period of the PWM output to the timer 7 preset register 2 (TM7PR2). To set 1/4 duty of 25000 dividing, set as; 25000/4=6249 (0x1869) At the same time, the same value is loaded the timer 7 compare register 2 (TM7OC2).
(9) Start the timer operation TM7MD1(0x03F78) bp4 :TM7EN =1	(9) Set the TM7EN flag of the TM7MD1 register to "1" to operate the timer 7.

TM7BC counts up from 0x0000. The PWM source waveform outputs "H" until TM7BC matches the set value of the TM7OC2 register. Once they matches, it outputs "L". After that, TM7BC continues to count up. Once TM7BC matches the TM7OC1 register to be cleared, the PWM output waveform outputs "H" again and TM7BC counts up from 0x0000 again.

In the initial state of the PWM output, it is changed to "H" output from "L" output at the timing that the PWM operation is selected with the TM7PWM flag of the TM7MD register.

Set as the set value of TM7OC2 < the set value of TM7OC1.
If it is set as the set value of TM7OC2 ≥ the set value of TMnOC1, the PWM output is a "H" fixed output.

6.8 16-bit Timer Synchronous Output

6.8.1 Operation

If the binary counter of the timer reaches the set value of the compare register, port 7 outputs the port 7 output latched data at the next count clock.

■ 16-bit Timer Synchronous Output Operation (Timer 7)

Port 7 outputs the port 7 latched data at a TM7OC1 compare register reaches the binary counter or at the interrupt request generation by the full count overflow. Only port 7 can be used in this operation, and each bit can be set individually.

■ Count Timing of Synchronous Output (Timer 7)

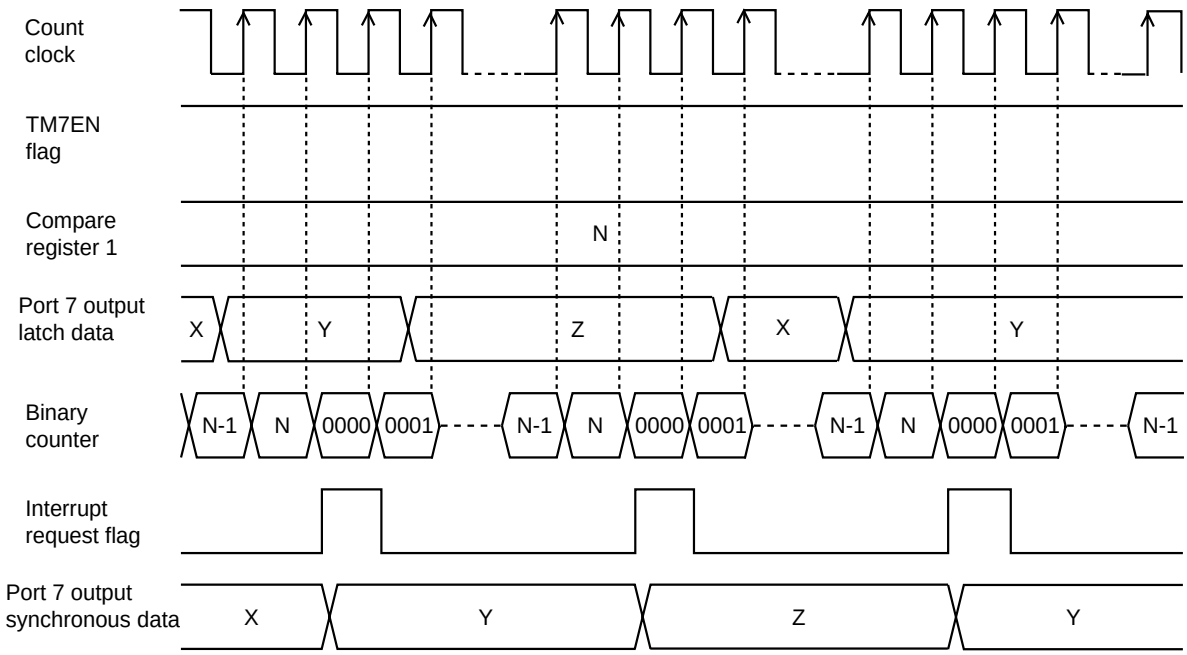


Figure:6.8.1 Count Timing of Synchronous Output (Timer 7)

Output pin outputs the port 7 output latch data at the interrupt request generation by the match of a binary counter and a compare register 1.

6.8.2 Setup Example

■ Synchronous Output Setup Example (Timer 7)

Here is an example to output the port 7 latch data from the synchronous output pin constantly (in every 100 µs) with the timer 7. As the clock source of the timer 7, fs/4 (fosc=4 MHz) is selected. An example setup procedure, with a description of each step is shown below;

Setup Procedure	Description
(1) Stop the counter TM7MD1(0x03F78) bp4 :TM7EN =0	(1) Set the TM7EN flag of the timer 7 mode register 1 (TM7MD1) to "0" to stop the timer 7 counting.
(2) Select the synchronous output event P7SEV(0x03F2F) bp1-0 :P7SEV1-0 =01	(2) Set the P7SEV1 to 0 flag of the pin control register (P7SYO) to "01" to set the synchronous output event to the timer 7 interrupt.
(3) Set the synchronous output pin P7SYO(0x03F1F) =0xFF P7DIR(0x03F37) =0xFF	(3) Set the port 7 synchronous output control register (P7SYO) to 0xFF to set the synchronous output pin. (P77 to P70:Synchronous output pin) Set the port 7 direction control register (P7DIR) to 0xFF to set the port 7 to the output pin. [Chapter 4 I/O Ports]
(4) Select the timer clear factor TM7MD2(0x03F79) bp5 :TM7BCR =1	(4) TSet the TM7BCR flag of the TM7MD2 register to "1" to select the compare match as the binary counter clear source.
(5) Select the count clock source TM7MD1(0x03F78) bp1-0 :TM7CK1-0 =01 bp3-2 :TM7PS1-0 =10	(5) Select fs as the clock source by the TM7CK1 to 0 flag of theTM7MD1 register. Also, select 1/4 dividing as the count clock source by the TM7PS1 to 0 flag.
(6) Set the synchronous output event generation cycle TM7PR1(0x03F75,0x03F74) =0x0063	(6) Set the synchronous output event generation cycle to the timer 7 preset register 1 (TM7PR1). To set 10 kHz by dividing 1 MHz, set as; 100-1=99 (0x0063) At the same time, the same value is loaded to the timer 7 compare register 1 (TM7OC1), the timer 7 binary counter (TM7BC) is initialized to 0x0000.
(7) Start the timer operation TM7MD1 (0x03F78) bp4 :TM7EN =1	(7) Set the TM7EN flag of the TM7MD1 register to "1" to operate the timer.

TM7BC counts up from 0x0000. If any data is written to the port 7 output register (P7OUT), TM7BC is set to the set value of TM7OC1 register and the synchronous output pin outputs data of the port 7 in every time the interrupt request is generated.

6.9 16-bit Timer Capture

6.9.1 Operation

The value of the binary counter is read out at the timing of the external interrupt input signal which is synchronized to fosc, fs or the external event signal, or at the timing of the writing operation with any value to the capture register.

■ Capture Operation with External Interrupt Signal as the Trigger (Timer 7)

Input capture trigger is generated at the external interrupt signal. The capture trigger is selected by the Timer 7 mode register 1 (TM7MD1) and the timer mode register 2 (TM7MD2).Selectable capture triggers and the interrupt flag setup are shown below.

Table:6.9.1 Capture Trigger

Capture trigger source	Timer 7 mode register 2		Timer 7 mode register 1	External interrupt pin switching control register	
	T7ICT1-0	T7ICEDG0	T7ICEDG1	IRQ2SEL	IRQ3SEL
P20/IRQ0 falling edge	00	1	0	×	×
P20/IRQ0 rising edge	00	1	1	×	×
P20/IRQ0 both edges	00	0	×	×	×
P21/IRQ1 falling edge	01	1	0	×	×
P21/IRQ1 rising edge	01	1	1	×	×
P21/IRQ1 both edges	01	0	×	×	×
P22/IRQ2A falling edge	10	1	0	0	×
P22/IRQ2A rising edge	10	1	1	0	×
P22/IRQ2A both edges	10	0	×	0	×
P23/IRQ3A falling edge	11	1	0	×	0
P23/IRQ3A rising edge	11	1	1	×	0
P23IRQ3A both edges	11	0	×	×	0
PD0/IRQ2B falling edge	10	1	0	1	×
PD0/IRQ2B rising edge	10	1	1	1	×
PD0/IRQ2B both edge	10	0	×	1	×
PD1/IRQ3B falling edge	11	1	0	×	1
PD1/IRQ3B rising edge	11	1	1	×	1
PD1/IRQ3B both edge	11	0	×	×	1

In the external interrupt input pin (P20, P21), both edge input capture and both edge interrupt can not used at the same time as there is no both edge interrupt in external interrupt (IRQ0, IRQ1).

When the capture trigger is started at both edges of the external interrupt input signal, if it is engaged with data automatic transfer (ATC1), it is possible to measure the precision width which can measure the input signal between H and L continuously. Set the address of the input capture register TM7ICL to the memory pointer 1. Transferring the value of the input capture register (TM7ICL, TM7ICH) to the memory sequentially with every generation of the capture trigger make it possible to Measure the input signal between H and L continuously.

■ Capture Count Timing as Both Edges of External Interrupt Signal is selected as Trigger (Timer 7)

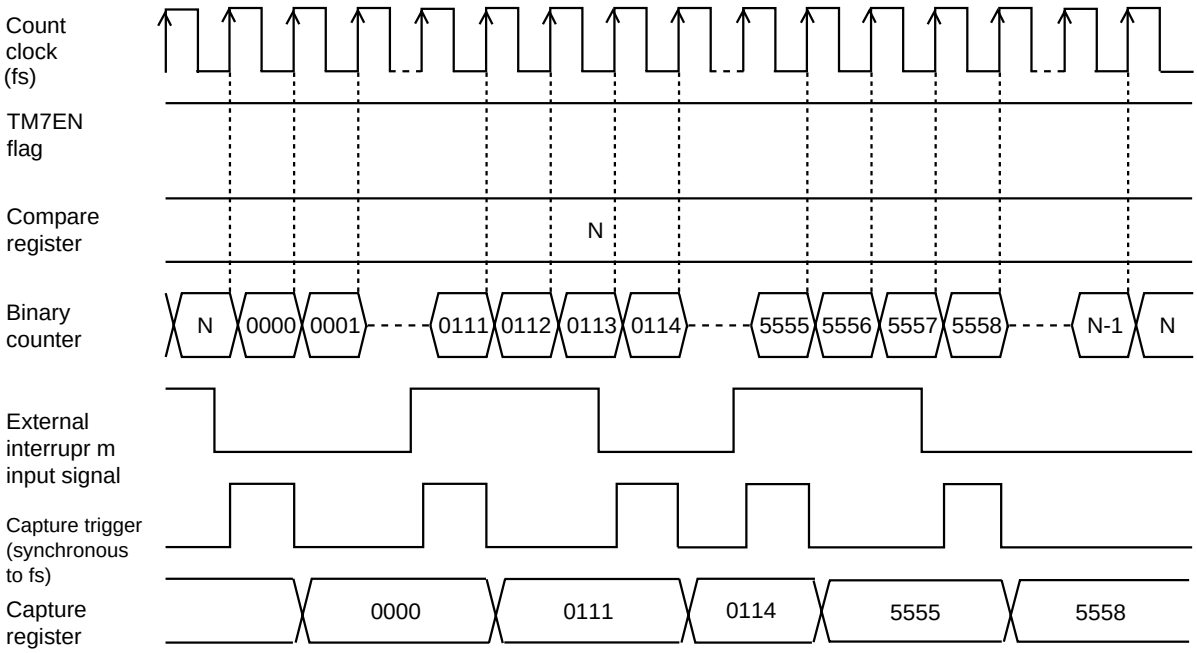


Figure:6.9.1 Capture Count Timing as Both Edges of External Interrupt Signal is selected as Trigger (Timer 7)

A capture trigger is generated at the both edges of the external interrupt m input signal. In synchronized with this capture trigger, the value of binary counter is loaded to the input capture register. The value loaded to the capture register is depending on the value of the binary counter at the falling edge of the capture trigger. When the specified edge is selected as the capture trigger source, the capture trigger is generated only at that edge. The other count timing is the same as the count timing of the timer operation.

When caputer trigger is generated at the both edges of the external interrupt input pin (P20,P21), it is not possible to measure the precision width which can measure continuously the input signal between H and L working with the automatic transfer controller (ATC1) .

When the binary counter is used as a free counter which counts 0x0000 to 0xFFFF set the compare register 1 to 0xFFFF, or set the TM7BCR flag of the TM7MD2 to "0".

Even if an event is generated before the value of the input capture register is read out, the value of the input capture register can be rewritten.

Capture trigger is generated by sampling the external interrupt input singal at the system clock. So, when the interrupt input singal is faster than the system clock cycle, the external interrupt input edge may not be detected. Also, the capture function can not be used during STOP mode because the system clock is stopped.

In the initial state after releasing the reset, the generation of trigger by the external interrupt signal is disabled. Set the T7ICEN flag of the TM7MD2 register to "1" to enable the trigger generation.

■ Capture Operation Triggered by Writing Software (Timer 7)

A capture trigger can be generated by writing an arbitrary value to the input capture register (TM7IC),and at the same timing, the value of the binary counter can be stored to the input capture register.

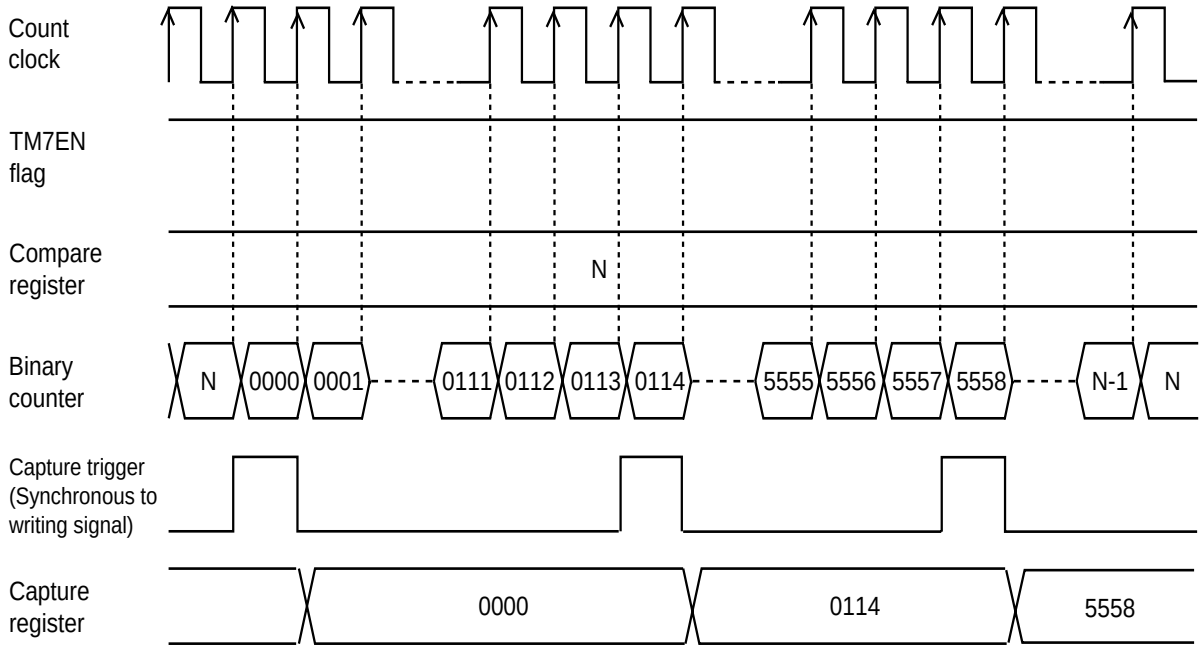


Figure:6.9.2 Capture Count Timing Triggered by Writing Software (Timer 7)

The capture trigger is generated at the writing signal to the input capture register. The writing signal is generated at the last cycle of the writing instruction. In synchronized with this capture trigger, the value of the binary counter is loaded to the input capture register. The value is depending on the value of the binary counter at the falling edge of the capture trigger. The other timing is the same as the timer operation.

The writing to the input capture to generate the capture trigger should be done with 8-bit access instruction of the TM7ICL register or the TM7ICH register.
At this time, data is not actually written to the TM7IC register.

On hardware, there is no flag to disable the capture operation triggered by writing software. Capture operation is enabled regardless of the T7ICEN flag of the TM7MD2 register.

If the capture operation is done during TM7IO input or the operation at fosc, incorrect data at counting up may be written to the input capture register. To prevent this, use the event count by the synchronous TM7IO input.
[Chapter 6 6.4.1. 16-bit Event Count Operation

6.9.2 Setup Example

■ Capture Function Setup Example

Pulse width measurement is enabled by storing the value of the binary counter to the capture register at the interrupt generation edge of the external interrupt 0 input singal with timer 7. The interrupt generation edge is specified to be the rising edge.

An example setup prcedure, with a description of each step is shown below.

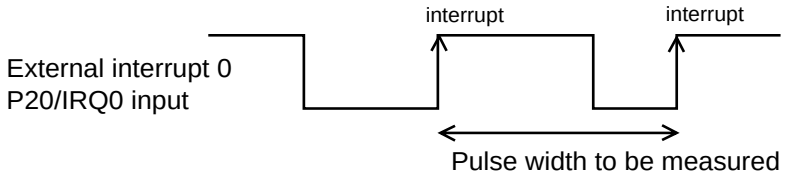


Figure:6.9.3 Pulse Width Measurement of External Interrupt 0

Setup Procedure	Description
(1) Stop the counter TM7MD1(0x03F78) bp4 :TM7EN =0	(1) (1)Set the TM7EN flag of the Timer 7 mode register 1 (TM7MD1) to "0" to stop the Timer 7 counting.
(2) Disable the interrupt IRQ0ICR(0x03FE2) bp1 :IRQ0IE =0	(2) Set the IRQ0IE flag of the IRQ0ICR register to "0" to disable the interrupt.
(3) Select the timer clear source TM7MD2(0x03F79) bp5 :TM7BCR =1	(3) Set the TM7BCR flag of the Timer 7 mode register 2 (TM7MD2) to "1" to select the compare match as the binary counter clear source.
(4) Select the count clock source TM7MD1(0x03F78) bp1-0 :TM7CK1-0 =00 bp3-2 :TM7PS1-0 =00	(4) Select fosc as the clock source by the TM7CK1 to 0 flag of the TM7MD1 register. Also, select 1/1 dividing of fosc as the count clock source by the TM7PS1 to 0 flag.
(5) Set the compare register TM7PR1(0x03F75,0x03F74) =0xFFFF	(5) Set 0xFFFF to the Timer 7 preset register 1(TM7PR1). At that time, the same value is loaded to the Timer 7 compare register 1 (TM7OC1), the Timer 7 binary counter (TM7BC) is initialized to 0x0000.
(6) Select the capture trigger generation interrupt source TM7MD2(0x03F79) bp1-0 :7ICT1-0 =00	(6) Select the external interrupt 0 (IRQ0) input as the capture trigger generation source by the T7ICT1 to 0 flag of the TM7MD2 register.
(7) Select the capture trigger generation edge TM7MD1(0x03F78) bp6 :7ICEDG1 =1 TM7MD2 (0x03F79) bp7 :T7ICEDG0 =1	(7) Set the T7ICEDG1 flag of the TM7MD1 register to "1" to select the rising edge as the capture trigger generation edge. Also, set the T7ICEDG0 flag of the TM7MD2 register to "1" to enable the specify edge as the capture trigger generation source.

Setup Procedure	Description
(8) Select the interrupt generation valid edge IRQ0ICR(0x03FE2) bp5 :REDG0 =1	(8) Set the REDG0 flag of the external interrupt 0 control register (IRQ0ICR) to "1" to select the rising edge as the interrupt generation valid edge.
(9) Set the interrupt level IRQ0ICR(0x03FE2) bp7-6 :IRQ0LV1-0 =10	(9) Set the interrupt level by the IRQ0LV1 to 0 flag of the IRQ0ICR register. If the interrupt request flag is already set, clear the request flag. [Chapter 3 3.1.4. Interrupt Flag Setup]
(10) Enable the interrupt IRQ0ICR(0x033FE2) bp1 :IRQ0IE =1	(10) Set the IRQ0IE flag of the IRQ0ICR register to "1" to enable the interrupt.
(11) Enable the capture trigger generation TM7MD2(0x03F79) bp2:T7ICEN =1	(11) Set the T7ICEN flag of the TM7MD2 register to "1" to enable the capture trigger generation.
(12) Start the timer operation TM7MD1(0x03F78) bp4:TM7EN =1	(12) Set the TM7EN flag of the TM7MD1 register to "1" to operate the Timer 7.

TM7BC counts up from 0x0000. At the timing of the rising edge of the external interrupt 0 input signal, the value of TM7BC is loaded to the TM7IC register. At that time, the pulse width between rising edge of the external interrupt input signal can be measured by reading the value of the TM7IC register through interrupt service routine, and calculating the difference between the capture values.

Chapter 7 Time Base Timer / Free-running Timer

7

7.1 Overview

This LSI has a time base timer and a 8-bit free-running timer (timer 6).

Time base timer is a 15-bit timer counter.

7.1.1 Functions

Table:7.1.1 shows the clock source and the interrupt generation cycle that timer 6 and time base timer can use.

Table:7.1.1 Clock Source and Generation Cycle

	Time base timer	Timer 6 (8-bit free-running)
8-bit timer operation	×	O
Interrupt	TBIRQ	TM6IRQ
Clock source	fosc fx	fosc fx fs fosc × $1/2^{12}$ *1 fosc × $1/2^{13}$ *1 fx × $1/2^{12}$ *2 fx × $1/2^{13}$ *2
Interrupt generation cycle	fosc × $1/2^{7}$ *1 fosc × $1/2^{8}$ *1 fosc × $1/2^{9}$ *1 fosc × $1/2^{10}$ *1 fosc × $1/2^{13}$ *1 fosc × $1/2^{15}$ *1 fx × $1/2^{7}$ *2 fx × $1/2^{8}$ *2 fx × $1/2^{9}$ *2 fx × $1/2^{10}$ *2 fx × $1/2^{13}$ *2 fx × $1/2^{15}$ *2	The interrupt generation cycle is decided by the arbitrary value written to TM6OC.
fosc: Machine clock (High speed oscillation) fx: Machine clock (Low speed oscillation) fs: System clock [Chapter 2 2.5 Clock Switching] *1 Can be used when a clock source of time base timer is selected to 'fosc'. *2 Can be used when a clock source of time base timer is selected to 'fx'.		

When 'fs' is used as a clock source, it counts at "rising" of the count clock and in other uses, it counts "falling" of the count clock.

Count clock source should be changed with the timer interrupt is prohibited.

7.1.2 Block Diagram

■ Timer 6, Time Base Timer Block Diagram

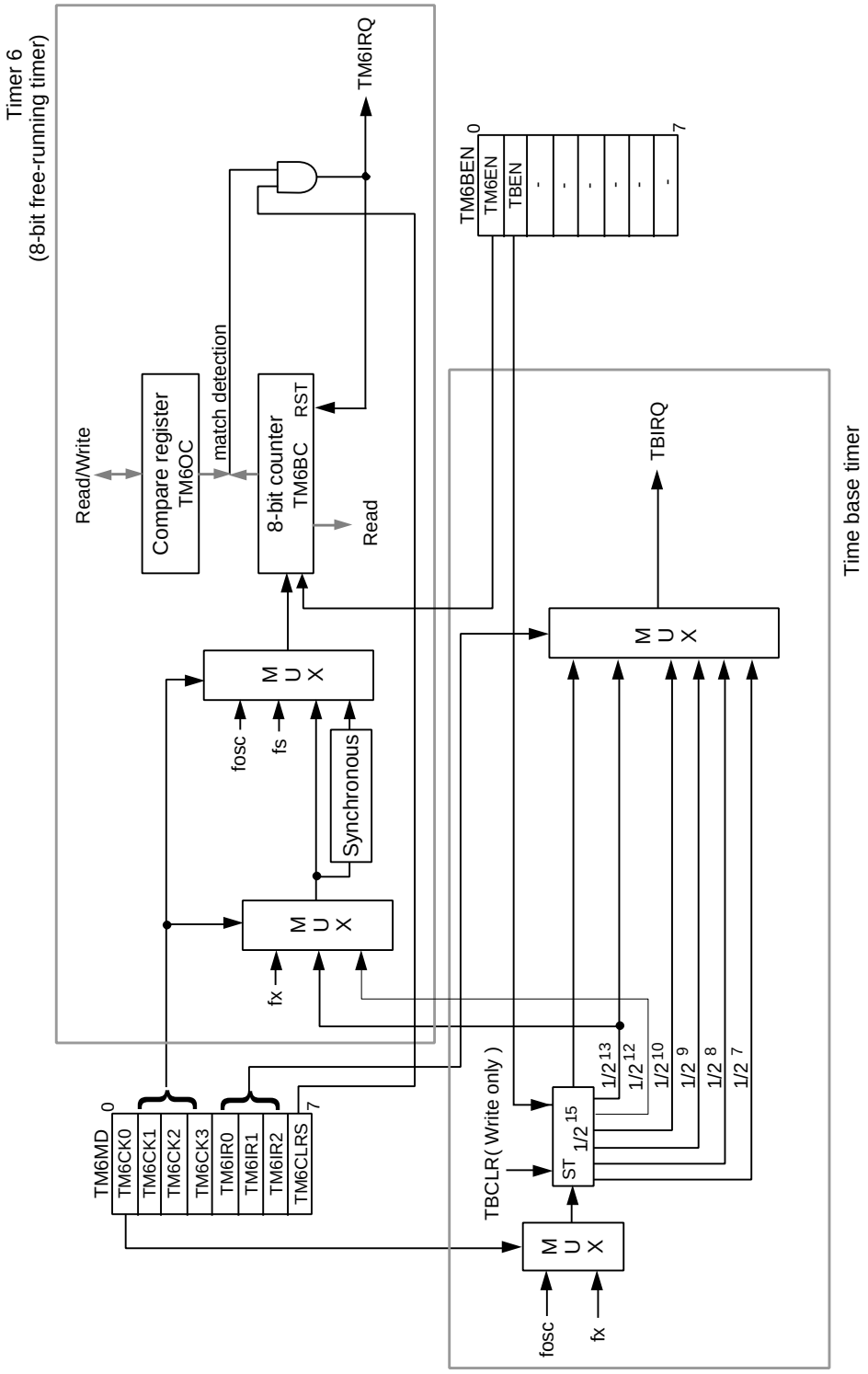


Figure:7.1.1 Block Diagram (Timer 6, Time Base Timer)

7.2 Control Registers

Timer 6 consists of binary counter (TM6BC), compare register (TM6OC), and is controlled by mode register (TM6MD). Time base timer is controlled by mode register (TM6MD) and time base timer clear register (TBCLR). Both timers are operated by the enable signal of the TM6BEN.

7.2.1 Control Registers

Table:7.2.1 shows the registers that control timer 6, time base timer.

Table:7.2.1 Control Registers

	Register	Address	R/W	Function	Page
Timer 6	TM6BC	0x03F68	R	Timer 6 binary counter	VII-6
	TM6OC	0x03F69	R/W	Timer 6 compare register	VII-6
	TM6MD	0x03F6A	R/W	Timer 6 mode register	VII-8
	TM6BEN	0x03F6C	R/W	Timer 6 enable register	VII-7
	TM6ICR	0x03FEE	R/W	Timer 6 interrupt control register	III-32
Time base timer	TM6MD	0x03F6A	R/W	Timer 6 mode register	VII-8
	TBCLR	0x03F6B	W	Time base timer clear control register	VII-6
	TBICR	0x03FEF	R/W	Time base interrupt control register	III-33

7.2.2 Programmable Timer Registers

Timer 6 is a 8-bit programmable counter.

Programmable counter consists of compare register (TM6OC) and binary counter (TM6BC).

Binary counter is a 8-bit up-counter. When the TM6CLRS flag of the timer 6 mode register (TM6MD) is "0" and the interrupt cycle data is written to the compare register (TM6OC), the timer 6 binary counter (TM6BC) is cleared to 0x00.

■ Timer 6 Binary Counter (TM6BC:0x03F68)

bp	7	6	5	4	3	2	1	0
Flag	TM6BC7	TM6BC6	TM6BC5	TM6BC4	TM6BC3	TM6BC2	TM6BC1	TM6BC0
At reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R

■ Timer 6 Compare Register (TM6OC:0x03F69)

bp	7	6	5	4	3	2	1	0
Flag	TM6OC7	TM6OC6	TM6OC5	TM6OC4	TM6OC3	TM6OC2	TM6OC1	TM6OC0
At reset	X	X	X	X	X	X	X	X
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Time base timer can be reset its operation by the software. Time base timer can be cleared by writing an arbitrary value to the time base timer clear control register (TBCLR).

■ Time Base Timer Clear Control Register (TBCLR:0x03F6B)

bp	7	6	5	4	3	2	1	0
Flag	TBCLR7	TBCLR6	TBCLR5	TBCLR4	TBCLR3	TBCLR2	TBCLR1	TBCLR0
At reset	-	-	-	-	-	-	-	-
Access	W	W	W	W	W	W	W	W

7.2.3 Timer 6 Enable Registers

This register controls the starting operation of the timer 6 and the time base timer.

■ Timer 6 Enable Register (TM6BEN:0x03F6C)

bp	7	6	5	4	3	2	1	0
Flag	-	-	-	-	-	Reserved	TBEN	TM6EN
At reset	-	-	-	-	-	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bp	Flag	Description
7-3	-	-
2	Reserved	Set always to “0“
1	TBEN	Time base timer operation control 0:Stop 1:Operation
0	TM6EN	Timer 6 operation control 0:Stop 1:Operation

When the timer 6 is operated, the operation is not started unless the TM6EN flag of the TM6BEN register is set to "1".

When the time base timer is operated, the operation is not started unless the TBEN flag of the TM6BEN register is set to "1".

7.2.4 Timer Mode Registers

This is readable / writable register that controls timer 6 and time base timer.

■ Timer 6 Mode Register (TM6MD:0x03F6A)

bp	7	6	5	4	3	2	1	0
Flag	TM6CLRS	TM6IR2	TM6IR1	TM6IR0	TM6CK3	TM6CK2	TM6CK1	TM6ICK0
At reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bp	Flag	Description
7	TM6CLRS	Timer 6 binary counter clear selection flag 0:Enable the initialization of TM6BC as TM6OC is written. 1:Disable the initialization of TM6BC as TM6OC is written. * TM6IRQ is disable as TM6CLRS = 0, TM6IRQ is enable as TM6CLRS = 1.
6-4	TM6IR2 TM6IR1 TM6IR0	Time base timer interrupt cycle selection 000:Time base selection clock $\times 1/2^{7}$ 001:Time base selection clock $\times 1/2^{8}$ 010:Time base selection clock $\times 1/2^{9}$ 011:Time base selection clock $\times 1/2^{10}$ 10-:Time base selection clock $\times 1/2^{13}$ 11-:Time base selection clock $\times 1/2^{15}$
3-1	TM6CK3 TM6CK2 TM6CK1	Timer 6 clock source selection 000:fosc 001:fs 010:fx 011:Synchronous fx 100:Time base selection clock $\times 1/2^{13}$ 101:Synchronous time base selection clock $\times 1/2^{13}$ 110:Time base selection clock $\times 1/2^{12}$ 111:Synchronous time base selection clock $\times 1/2^{12}$
0	TM6CK0	Time base timer clock source selection 0:fosc 1:fx

7.3 8-bit Free-running Timer

7.3.1 Operation

■ 8-bit Free-running Timer (Timer 6)

The generation cycle of the timer interrupt should be set in advance, by the set value of the compare register (TM6OC) and the clock source selection. When the binary counter (TM6BC) reaches the set value of the compare register, an interrupt request is generated at the next count clock and the binary counter is cleared to restart count up from 0x00.

Table:7.3.1 shows selectable clock source.

Table:7.3.1 Clock Source at Timer Operation (Timer 6)

Clock source	One count time		
	At fosc=20 MHz	At fosc=8.39 MHz	At fosc=2 MHz
fosc	50 ns	119.2 ns	500 ns
fx	30.5 μs		
fs	100 ns	238.4 ns	1000 ns
fosc × $1/2^{12}$	204.8 μs	488.2μs	2048 μs
fosc × $1/2^{13}$	409.6 μs	976.4 μs	4096 μs
fx × $1/2^{12}$	125 ms		
fx × $1/2^{13}$	250 ms		
fosc = 20 MHz, 8.39 MHz, 2 MHz fx = 32.768 KHz fs = fosc/2			

■ 8-bit Free-running Timer as a 1 Minute-timer, a 1 Second-timer

Table:7.3.2 shows the clock source selection and the TM6OC register setup, when a 8-bit free-running timer is used as a 1 minute-timer, a 1 second-timer.

Table:7.3.2 1 Minute-timer, 1 Second-timer (Timer 6) Setup

Interrupt Generation Cycle	Clock source	TM60CE Register
1 min	$fx \times 1/2^{13}$	0xEF
1 s	$fx \times 1/2^{13}$	0x03
fx = 32.768 kHz		

When the 1 minute-timer (1 m.) is set on Table:7.3.2, the bp2 waveform frequency (cycle) of the TM6BC register is 1 Hz (1 s.). So, that can be used for adjusting the seconds.

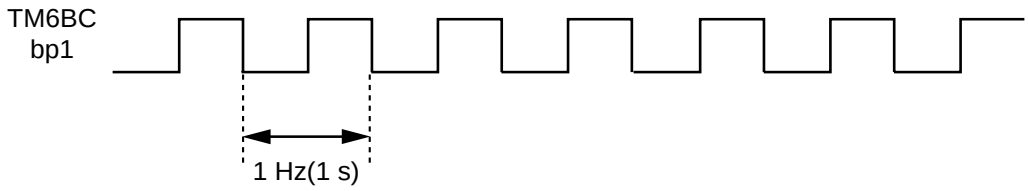


Figure:7.3.1 Waveform of TM6BC Register bp1 (Timer 6)

■ Count Timing of Timer Operation (Timer 6)

Binary counter counts up with the selected clock source as a count clock.

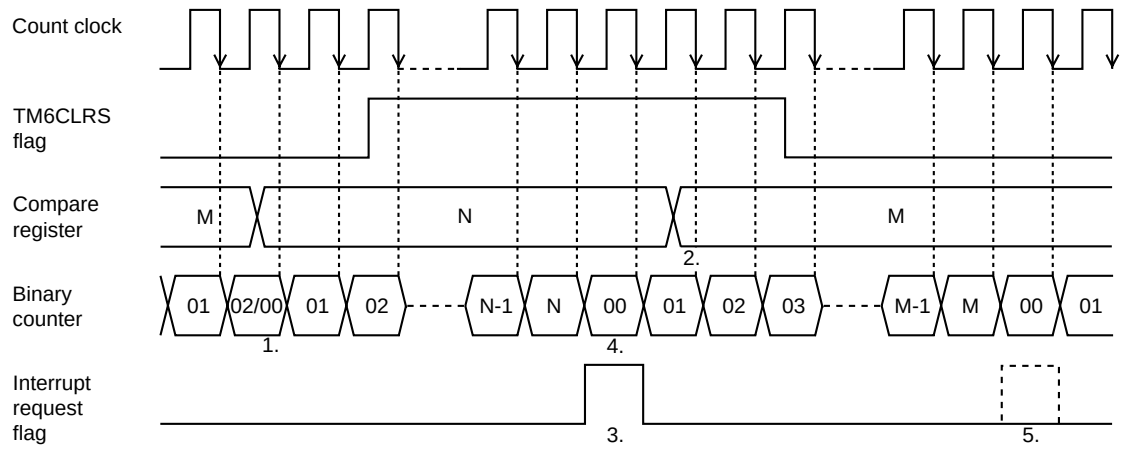


Figure:7.3.2 Count Timing of Timer Operation (Timer 6)

1. When any data is written to the compare register as the TM6CLRS flag is "0", the binary counter is cleared to 0x00.
2. Even if any data is written to the compare register as the TM6CLRS flag is "1", the binary counter is not changed.
3. When the binary counter reaches the value of the compare register as the TM6CLRS flag is "1", an interrupt request flag is set at the next count clock.
4. When an interrupt request flag is set, the binary counter is cleared to 0x00 and restarts the counting.
5. Even if the binary counter reaches the value of the compare register as the TM6CLRS flag is "0", no interrupt request flag is set.

When fx is used to the clock source, the binary counter should be cleared before starting the timer operation. Also, when 0x00 is set to the compare register, the synchronous fx should be used.

When the binary counter reaches the value in the compare register, the interrupt request flag is set and the binary counter is cleared at the next count clock.
So set the compare register as:
Compare register setting = (count till the interrupt request -1)

If the fx input is selected as a clock source and the value of timer 6 binary counter is read out at operation, an incorrect value could be read out. To prevent this, select a synchronous fs as the count clock source.

If the smaller value than the binary counter is set to the compare register at counting operation, the binary counter continues counting till overflow.

7.3.2 Setup Example

■ Timer Operation Setup (Timer 6)

Timer 6 generates interrupts constantly for timer function. Interrupts are generated in every 250 dividing (25 µs) by selecting fs (fosc = 10 MHz at operation) as clock source.

An example setup procedure, with a description of each step is shown below.

Setup Procedure	Description
(1) Enable the binary counter TM6MD(0x03F6A) bp7 :TM6CLRS =0	(1) Set the TM6CLRS flag of the timer 6 mode register (TM6MD) to "0". At the time, the initialization of the timer 6 binary counter (TM6BC) is enabled.
(2) Disable the interrupt TM6ICR(0x03FEE) bp1:TM6IE =0	(2) Set the TM6IE flag of the TM6ICR register to "0" to disable the interrupt.
(3) Select the clock source TM6MD(0x03F6A) bp3-1 :TM6CK3-1 =001	(3) Clock source can be selected by the TM6CK3 to 1 flag of the TM6MD register. Actually, fs is selected.
(4) Set the interrupt generation cycle TM6OC(0x03F69) =0xF9	(4) Set the interrupt generation cycle to the timer 6 compare register (TM6OC). At that time, TM6BC is initialized to 0x00.
(5) Enable the interrupt request TM6MD(0x03F6A) bp7 :TM6CLRS =1	(5) Set the TM6CLRS flag of the TM6MD register to "1" to enable the interrupt request generation.
(6) Set the interrupt level TM6ICR(0x03FEE) bp7-6 :TM6LV1-0 =01	(6) Set the interrupt level by the TM6LV1 to 0 flag of the timer 6 interrupt control register (TM6ICR). If the interrupt request flag may be already set, clear them. [Chapter 3. 3.1.4 Interrupt Flag Setup]
(7) Enable the interrupt TM6ICR(0x03FEE) bp1 :TM6IE =1	(7) Set the TM6IE flag of the TM6ICR register to "1" to enable the interrupt.
(8) Start the TM6 operation TM6BEN(0x03F6C) bp0 :TM6EN =1	(8) Set the TM6EN flag of the TM6BEN register to "1" to start the timer 6.

As TM6OC is set, TM6BC is initialized to 0x00 to count up.

When TM6BC matches TM6OC, the timer 6 interrupt request flag is set at the next count clock and TM6BC is cleared to 0x00 to restart counting.

If the TM6CLRS flag of the TM6MD register is set to "0", TM6BC can be initialized at every rewriting of TM6OC register, but in that state the timer 6 interrupt is disabled. If the timer 6 interrupt should be used, set the TM6CLRS flag to "1" after rewriting the TM6OC register.

On the timer 6 clock source selection, if the time base timer output or the time base timer synchronous output is selected, the clock setup of time base timer is necessary.

7.4 Time Base Timer

7.4.1 Operation

■ Time Base Timer (Time Base Timer)

Interrupt is constantly generated by a selected clock source and a interrupt generation cycle. Table:7.4.1 shows the interrupt cycle is combination with the clock source;

Table:7.4.1 Selection of Time Base Timer Interrupt Generation Cycle

Selected clock source	Interrupt generation cycle	
fosc	fosc × $1/2^7$	6.4 µs
	fosc × $1/2^8$	12.8 µs
	fosc × $1/2^9$	25.6 µs
	fosc × $1/2^{10}$	51.2 µs
	fosc × $1/2^{13}$	409.6 µs
	fosc × $1/2^{15}$	1.64 ms
fx	fx × $1/2^7$	3.9 ms
	fx × $1/2^8$	7.8 ms
	fx × $1/2^9$	15.6 ms
	fx × $1/2^{10}$	31.2 ms
	fx × $1/2^{13}$	250 ms
	fx × $1/2^{15}$	1 s
fosc =20 MHz fx =32.768 kHz		

■ Count Timing Timer Operation (Time Base Timer)

The counter counts up with the selected clock source as a counter clock.

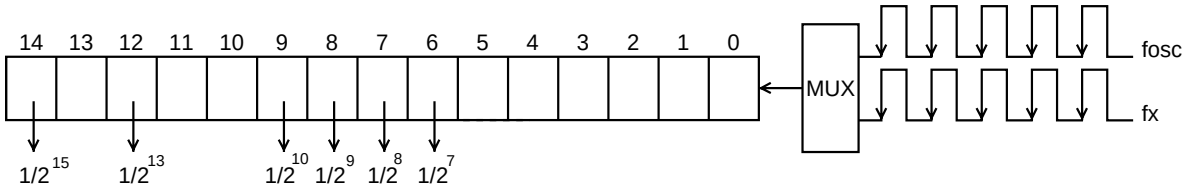


Figure:7.4.1 Count Timing of Timer Operation (Time Base Timer)

- When the selected interrupt cycle is passed, the interrupt request flag of the time base interrupt control register (TBICR) is set.

An interrupt may be generated at switching of the clock source. Enable the interrupt after switching the clock source.

The initialization can be done by writing an arbitrary value to the time base timer clear control register (TBCLR).

7.4.2 Setup Example

■ Timer Operation Setup (Time Base Timer)

An interrupt can be generated constantly with time base timer in the selected interrupt cycle. The interrupt generation cycle is fosc × $1/2^{13}$ (1 ms:fosc = 8.192 MHz) to generate interrupts.

An example setup procedure, with a description of each step is shown below

Setup Procedure	Description
(1) Disable the interrupt TBICR(0x03FEF) bp1 :TBIE =0	(1) Set the TBIE flag of the TBICR register to "0" to disable the interrupt.
(2) Select the clock source TM6MD(0x03F6A) bp0 :TM6CK0 =0	(2) Select fosc as a clock source by the TM6CK0 flag of the timer 6 mode register (TM6MD).
(3) Select the interrupt generation cycle TM6MD(0x03F6A) bp6-4 :TM6IR2-0 =100	(3) Select the selected clock × $1/2^{13}$ as an interrupt generation cycle by the TM6IR2 to 0 flag of the TM6MD register.
(4) Initialize the time base timer TBCLR(0x03F6B) =0x00	(4) Write value to the time base timer clear control register (TBCLR) to initialize time base timer.
(5) Set the interrupt level TBICR(0x03FEF) bp7-6 :TBLV1-0 =01	(5) Set the interrupt level by the TBLV1 to 0 flag of the time base interrupt control register (TBICR). If any interrupt request flag may be already set, clear them. [Chapter 3. 3.1.4 Interrupt Flag Setup]
(6) Enable the interrupt TBICR(0x03FEF) bp1 :TBIE =1	(6) Set the TBIE flag of the TBICR register to "1" to enable the interrupt.
(7) Start the time base timer operation TM6BEN(0x03F6C) bp1 :TBEN =1	(7) Set the TBEN flag of the TM6BEN register to "1" to start the time base timer.

- When the selected interrupt generation cycle is passed, the interrupt request flag of the time base interrupt control register (TBICR) is set to "1".

Chapter 8 Remote Control Functions

8

8.1 Overview

Remote control career output functions can create the career wave for the remote control and output.

8.1.1 Functions

Table:8.1.1 shows the remote control career output functions.

Table:8.1.1 The remote control career output functions.

Remote control career output base timer selection	Timer 0 Timer 3
Duty selection	1/2 1/3 Timer output
Remote control career output enable factor	RMOEN
Remote control career output enable	"L" level output Remote control career output
P10 particular function selection	Timer 0 Remote control career output

8.1.2 Block Diagram

■ Remote Control Career Output Block Diagram

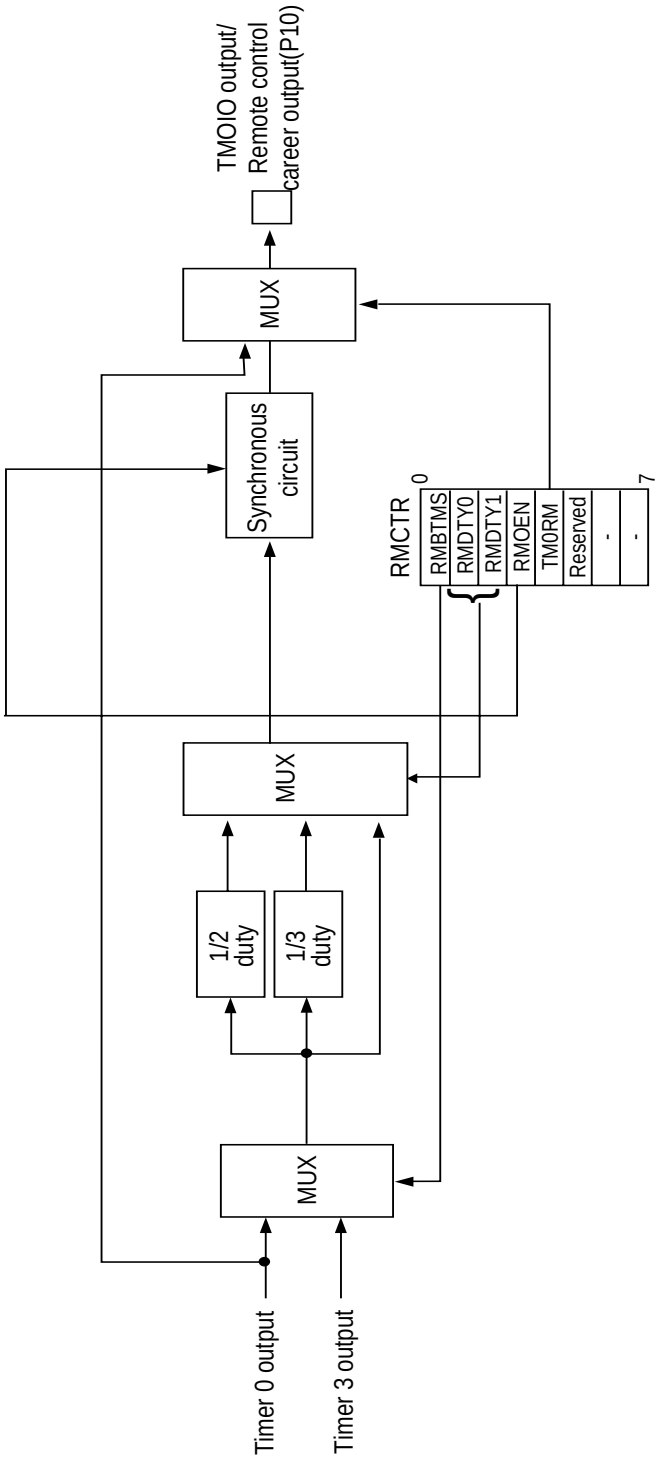


Figure:8.1.1 Remote Control Career Output Block Diagram

8.2 Control Registers

8.2.1 Control Registers

Table:8.2.1 shows the registers that control the remote control career output.

Table:8.2.1 Control Registers

Registers	Address	R/W	Function	Page
RMCTR	0x03F7F	R/W	Remote control career output control register	VIII-5

8.2.2 Remote Control Career Output Control Register

■ Remote Control Career Output Control Register (RMCTR:0x03F7F)

bp	7	6	5	4	3	2	1	0
Flag	-	-	Reserved	TM0RM	RM0EN	RMDTY1	RMDTY0	RMBTMS
At reset	-	-	0	0	0	0	0	0
Access	-	-	R/W	R/W	R/W	R/W	R/W	R/W

bp	Flag	Description
7-6	-	-
5	Reserved	Set always "0".
4	TM0RM	P10 particular functions output selection 0:TM0IO 1:RMOUT
3	RMOEN	Remote control career output enable 0:"L" level output 1:remote control career output
2-1	RMDTY1 RMDTY0	Remote control career duty 00:1/2 duty 01:1/3 duty 1-:Timer output
0	RMBTMS	Remote control career base timer selection 0:Timer 0 output selection 1:Timer 3 output selection

8.3 Operations

8.3.1 Operations

Remote control career output functions can create the career pulse for the remote control.

■ Operation of the remote control career output

Remote control career can be created by using the output signals of timer 0 and timer 3. Duty ratio is selectable from 1/2, 1/3, and timer output. Remote control career output signal is output from the RMOUT pin (P10).

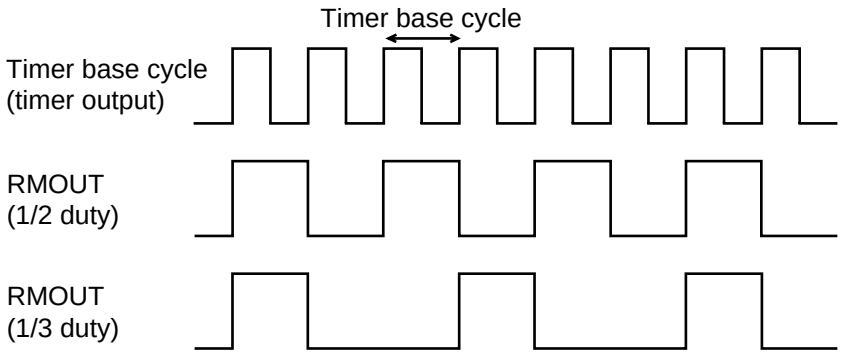


Figure:8.3.1 Remote Control Career Output Signal Duty Ratio

■ Count Timing of Remote Control Career Output Functions (timer0,timer3)

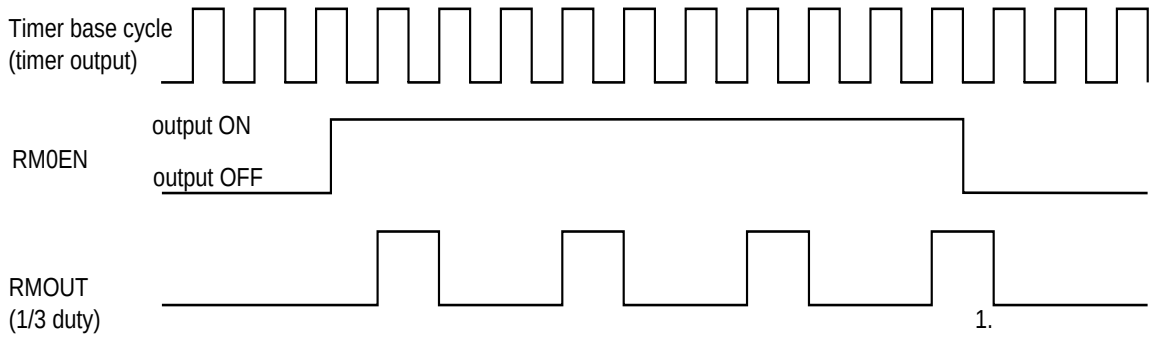


Figure:8.3.2 Count Timing of Remote Control Career Output Functions (timer0, timer3)

Even if the RMOEN flag is switched OFF at the career output "H", the career wave is held by the synchronous circuit.

Set the P1OMD0 flag of the P1OMD register to "1" at switched ON, and "0" at switched OFF.

When the RMOEN flag is changed, the base cycle and the duty cannot be changed at the same time. That affects the career wave.

8.3.2 Setup Examples

■ Remote Control Career Output Functions Setup

The setup examples that 1/3 duty career pulse signal is output as 36.7 kHz for "H" period from the RMOUT pin with the timer 0 are shown below. The clock source of the timer 0 selects fs/2 (at fs = 8 MHz). An example setup procedure, with a description of each step is shown below.

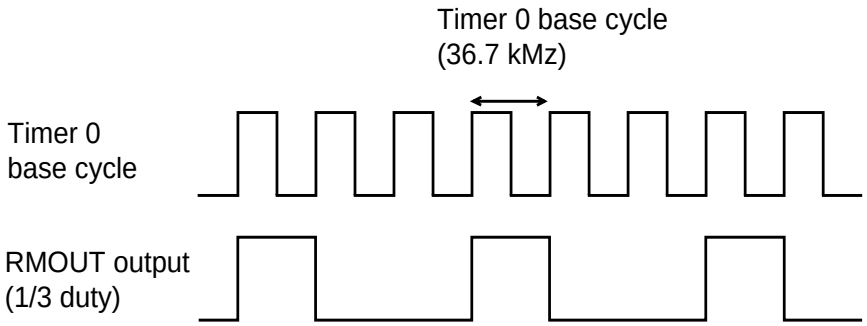


Figure:8.3.3 Output Wave of RMOUT Output Pin

Setup Procedure	Description
(1) Disable the remote control career output RMCTR(0x03F7F) bp3 :RMOEN =0	(1) Set the RMOEN flag of the remote control career output control register (RMCTR) to "0" to disable the remote control career output.
(2) Select the base cycle setup timer RMCTR(0x03F7F) bp0 :RMBTMS =0	(2) Set the RMBTMS flag of the RMCTR register to "0" to select the timer 0 as the setup timer of the base cycle.
(3) Select the career output duty RMCTR(0x03F7F) bp2-1 :RMDTY1-0 =01	(3) Set the RMDTY1, 0 flag of the RMCTR register to "0, 1" to select the duty to 1/3.
(4) Confirm the counter stop TM0MD(0x03F54) bp3 :TM0EN =0	(4) Set the TM0EN flag of the timer 0 mode register (TM0MD) to "0" to stop counting of the timer 0.
(5) Set the remote control career output of the particular function pin P1OMD(0x03F2B) bp0 :P1OMD0 =1 P1DIR(0x03F31) bp0 :P1DIR0 =1 RMCTR(0x03F7F) bp4 :TM0RM =1	(5) Set the P1OMD0 flag of the port 1 output mode register (P1OMD) to "1" to set P1OMD0 pin to the particular function pin. Set the P1DIR0 flag of the port 1 direction control register (PTM0DIR) to "1" to set the output mode. Set the TM0RM flag of the RMCTR register to "1" to select the remote control career output.

Setup Procedure	Description
(6) Select the timer general operation TM0MD(0x03F54) bp4 :TM0PWM =0 bp5 :TM0MOD =0 bp6 :TM0POP =0	(6) Set the TM0PWM flag, the TM0MOD flag, and the TM0POP flag of the TM0MD register to "0" to select the timer general operation.
(7) Select the count clock source TM0MD(0x03F54) bp2-0 :TM0CK2-0 =X01	(7) Select the prescaler output to the clock source by theTM0CK2 to 0 of the TM0MD register.
(8) Select and enable the prescaler output CK0MD(0x03F56) bp2-1 :TM0PSC1-0 =X0 bp0 :TM0BAS =1	(8) Select the fs/2 to the prescaler output by the TM0PSC1 to 0 flag, TM0BAS flag of the timer 0 prescaler selection register.
(9) Set the base cycle of the remote control career TM0OC(0x03F52) =0x36	(9) Set the base cycle of the remote control career by writing 0x36 to the timer 0 compare register (TM0OC). To get 2x cycles of 36.7 kHz (73.4 kHz) that is divided fs = 8 MHz, the setup value is set to (fs/2 MHz/73.4 kHz) - 1 = 54 (0x36).
(10) Start the timer operation TM0MD(0x03F54) bp3 :TM0EN =1	(10) Set the TM0EN flag of the TM0MD register to "1" to start the timer 0.
(11) Enable the remote control career output RMCTR(0x03F7F) bp3 :RMOEN =1	(11) Set the RMOEN flag of the RMCTR register to "1" to enable the remote control career output.

TM0BC starts the count up from 0x00. As The base cycle pulse that is set at the TM0OC is output from the timer 0, 1/3 of the remote control career pulse signal is output. If the RM0EN flag of the RMCTR register is set to "0", the output signal of the remote control career pulse is stopped.

Chapter 9 Watchdog Timer

9

9.1 Overview

This LSI has a watchdog timer. This timer is used to detect software processing errors. It is controlled by the watchdog timer control register (WDCTR). And, once an overflow of watchdog timer is generated, a watchdog interrupt (WDIRQ) is generated. If the watchdog interrupt is generated twice, consecutively, it is regarded to be an indication that the software cannot execute in the intended sequence; thus, a system reset is initiated by the hardware.

9.1.1 Block Diagram

■ Watchdog Timer Block Diagram

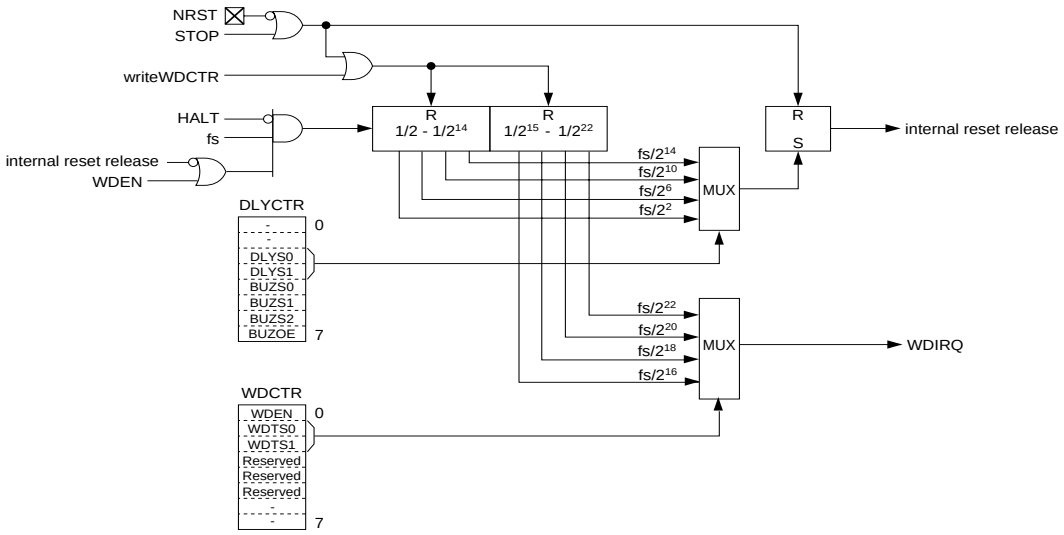


Figure:9.1.1 Block Diagram (Watchdog Timer)

The watchdog timer is also used as a timer to count the oscillation stabilization wait time. this is used as a watchdog timer except at recovering from STOP mode and at reset releasing.

The watchdog timer is initialized at reset or at STOP mode, and counts system clock (fs) as a clock source from the initial value (0x0000). The oscillation stabilization wait time is set by the oscillation stabilization control register (DLYCTR).

[Chapter2 2.8 Reset]

9.2 Control Register

The watchdog timer is formed by the control register (WDCTR).

■ Watchdog Timer Control Register

Table:9.2.1 Watchdog timer control register (WDCTR : 0x03F02)

bp	7	6	5	4	3	2	1	0
Flag	-	-	Reserved	Reserved	Reserved	WDTS1	WDTS0	WDEN
At reset	-	-	0	0	0	1	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bp	Flag	Description
7-6	-	-
5-3	Reserved	Set always "0".
2-1	WDTS1 WDTS0	Watchdog time-out period setup 00:2^{16} of system clock 01:2^{18} of system clock 10:2^{20} of system clock 11:2^{22} of system clock
0	WDEN	Watchdog timer enable 0:Watchdog timer is stopped 1:Watchdog timer is operated

9.3 Operation

9.3.1 Operation

The watchdog timer counts system clock (fs) as a clock source. If the watchdog timer is overflowed, the watchdog interrupt (WDIRQ) is generated as non maskable interrupt (NMI). At reset, the watchdog timer is stopped, but once the operation is enabled, it cannot be stopped except at reset. The watchdog timer control register (WDCTR) sets when the watchdog timer is released or how long the time-out period should be.

If the watchdog interrupt (WDIRQ) is generated twice consecutively, it is regarded to be an indication that the software cannot execute in the intended sequence; thus, a system reset is initiated by the hardware.

The watchdog timer cannot stop, once it starts operation.

■ Usage of Watchdog Timer

When the watchdog timer is used, constant clear in program is needed to prevent an overflow of the watchdog timer. As a result of the software failure, the software cannot execute in the intended sequence, thus the watchdog timer overflows to detect errors.

Programming of the watchdog is generally done in the last step of its programming.

■ How to Detect Incorrect Code Execution

The watchdog timer is executed to be cleared in the certain cycle on the correct code execution. In this LSI, the watchdog timer detects errors when,

1. the watchdog timer overflows.

When the watchdog timer detects any error, the watchdog interrupt (WDIRQ) is generated as a non maskable interrupt (NMI).

■ How to clear Watchdog Timer

The watchdog timer can be cleared by writing to the watchdog timer control register (WDCTR). The watchdog timer can be cleared regardless of the writing data to the register. The bit-set (BSET) that does not change the value is recommended.

■ Watchdog Time-out Period

The watchdog time-out period is decided by the bp2, 1 (WDTS1-0) of the watchdog timer control register (WDCTR) and the system clock (fs). If the watchdog timer is not cleared by this set value, that is regarded as an error and the watchdog interrupt (WDIRQ) of the non maskable interrupt (NMI) is generated.

Table:9.3.1 Watchdog Time-out Period

WDTS1	WDTS0	Watchdog Time-out Period
0	0	2^{16} x system clock
0	1	2^{18} x system clock
1	0	2^{20} x system clock
1	1	2^{22} x system clock

The system clock is decided by the CPU mode control register (CPUM).

[Chapter2 2.6 Clock Switching]

The watchdog time-out period is generally decided from the execution time for main routine of program. That should be set the longer cycle than the value of the execution time or main routine divided by natural number (1, 2,,,). And set the command of the watchdog timer clear to the main routine as that value makes the same cycle.

■ Watchdog Timer and CPU Mode

The relation between this watchdog timer and CPU mode features are as follows;

1. In NORMAL, IDLE, SLOW mode, the system clock is counted.
2. The counting is continued regardless of swithching at NORMAL, IDLE, SLOW mode.
3. In HALT mode, the watchdog timer is stopped.
4. In STOP mode, the watchdog timer is cleared automatically.
5. In STOP mode, the watchdog interrupt cannot be generated.
6. After recovering from STOP, the counting is executed for the period of the oscillation stabilization wait time.
7. After releasing reset, the watchdog timer is cleared automatically and stop counting.

Generally, in the system used STOP mode, if the STOP mode is done or not is divided on the program execution, but, in this case, the counting value of the watchdog timer differs.

9.3.2 Setup Example

The watchdog timer detects errors. On the following example, the time-out period is set to $2^{18} \times$ system clock.

An example setup procedure, with a description of each step is shown below.

■ Initial Setup Program (Watchdog Timer Initial Setup Example)

Setup Procedure	Description
(1) Set the time-out period WDCTR(0x03F02) bp2-1:WDTS1-0 =01	(1) Set the WDTS1-0 flag of the watchdog timer control register (WDCTR) to "01" to select the time-out period to $2^{18} \times$ system clock.
(2) Start the watchdog timer operation WDCTR(0x03F02) bp0:WDEN =1	(2) Set the WDEN flag of the WDCTR register to "1" to start the watchdog timer operation.

■ Main Routine Program (Watchdog Timer Constant Clear Setup Example)

Setup Procedure	Description
(1) Set the watchdog timer for the constant clear Writing to WDCTR(0x03F02) (c.f.)BSET (WDCTR) WDEN (bp0:WDEN=1)	(1) Clear the watchdog timer by the cycle up to $2^{18} \times$ system clock. The watchdog timer clear should be inserted in the main routine, with the same cycle, and to be the set cycle. The recommended instruction is the bit-set (BSET), does not change value, for clear.

■ Interrupt Service Routine Setup

Setup Procedure	Description
(1) Set the watchdog interrupt service routine NMICR(0x03FE1) TBNZ (NMICR),WDIR,WDPR0	(1) If the watchdog timer overflows, the non maskable interrupt is generated. Confirm that the WDIR flag of the non maskable interrupt service routine to manage the suitable execution.

The operation, just before the WDOG interrupt may be executed wrongly. Therefore, if the WDOG interrupt is generated, initialize the system.

Chapter 10 Buzzer

10

10.1 Overview

This LSI has a buzzer. It can output the square wave that multiply by $1/2^9$ to $1/2^{14}$ of the high frequency oscillation clock, or by $1/2^3$ to $1/2^4$ of the low frequency oscillation clock.

10.1.1 Block Diagram

■ Buzzer Block Diagram

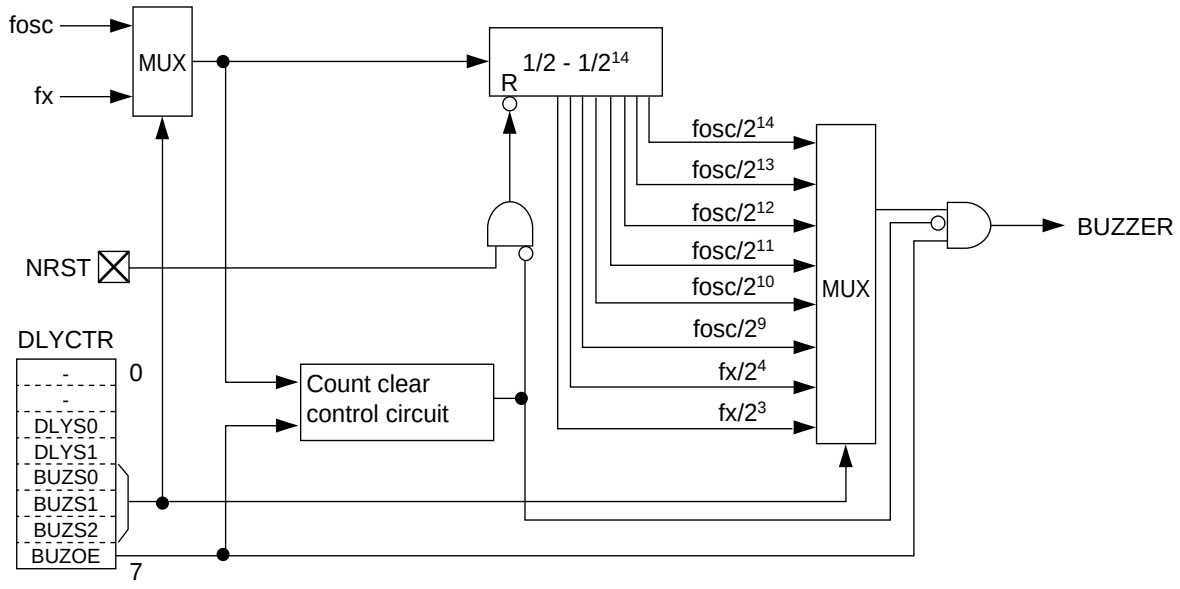


Figure:10.1.1 Buzzer Block Diagram

10.2 Control Register

■ Oscillation Stabilization Wait Time Control Register

Table:10.2.1 Oscilllation Stabilization Wait Time Control Register (DLYCTR:0x03F03)

bp	7	6	5	4	3	2	1	0
Flag	BUZOE	BUZS2	BUZS1	BUZS0	DLYS1	DLYS0	-	-
at reset	0	0	0	0	0	0	-	-
Access	R/W	R/W	R/W	R/W	R/W	R/W	-	-

bp	Flag	Description
7	BUZOE	Output selection 0:Buzzer stop 1:Buzzer operation
6-4	BUZS2 BUZS1 BUZS0	Buzzer output frequency selection 000:fosc/2^{14} 001:fosc/2^{13} 010:fosc/2^{12} 011:fosc/2^{11} 100:fosc/2^{10} 101:fosc/2^{9} 110:fx/2^{4} 111:fx/2^{3}
3-2	DLYS1 DLYS0	Oscillation stabilization wait period selection 00:fs/2^{14} 01:fs/2^{10} 10:fs/2^{6} *1 11:fs/2^{2} *1
1-0	-	-

*1:Do not use at high-speed operation (NORMAL mode).

Use at slow-speed operation (SLOW mode).

10.3 Operation

10.3.1 Operation

■ Buzzer

Buzzer outputs the square wave, having frequency $1/2^9$ to $1/2^{14}$ of the high oscillation clock (fosc), or $1/2^3$ to $1/2^4$ of the low oscillation clock (fx). The BUZS 2, 1, 0 flag of the oscillation stabilization wait control register (DLYCTR) set the frequency of the buzzer output. The BUZOE flag of the oscillation stabilization wait control register (DLYCTR) sets buzzer output ON / OFF.

■ Buzzer Output Frequency

The frequency of buzzer output is decided by the frequency of the high oscillation clock (fosc) or the low oscillation clock (fx) and the bit 6, 5, 4 (BUZS2, BUZS1, BUZS0) of the oscillation stabilization wait control register (DLYCTR).

Table:10.3.1 Buzzer Output Frequency

fosc	fx	BUZS2	BUZS1	BUZSO	Buzzer output frequency
20 MHz	-	0	0	0	1.22 kHz
20 MHz	-	0	0	1	2.44 kHz
20 MHz	-	0	1	0	4.88 kHz
8.39 MHz	-	0	1	0	2.05 kHz
8.39 MHz	-	0	1	1	4.10 kHz
2 MHz	-	1	0	0	1.95 kHz
2 MHz	-	1	0	1	3.91 kHz
-	32 kHz	1	1	0	2 kHz
-	32 kHz	1	1	1	4 kHz

10.3.2 Setup Example

■ Setup Example

Buzzer outputs the square wave of 2 kHz from PD5 pin. It is used 8.39 MHz as the high oscillation clock (fosc).

An example of setup procedure, with a description of each step is shown below.

Setup Procedure	Description
(1) Set the buzzer frequency DLYCTR (0x03F03) bp6-4 :BUZS2-0 =010	(1) Set BUZS2 to BUZS0 flag of the oscillation stabilization wait control register (DLYCTR) to "010" to select fosc/ 2^{12} to the buzzer frequency. When the high oscillation clock fosc is 8.39 MHz, the buzzer output frequency is 2.05 kHz.
(2) Set PD5 pin PDOUT (0x03F1D) bp5 :PDOUT5 =0 PDDIR (0x03F3D) bp5 :PDDIR5 =1	(2) Set the output data PDOUT5 of PD5 pin to "0", and set the direction control PDDIR5 of PD5 pin to "1" to select output mode. Port D5 pin outputs low level.
(3) Buzzer output ON DLYCTR (0x03F03) bp7 :BUZOE =1	(3) Set the BUZSE flag of the oscillation stabilization wait control register (DLYCTR) to "1" to output the square wave of the buzzer output frequency set by PD5 pin.
(4) Buzzer output OFF DLYCTR (0x03F03) bp7 :BUZOE =0	(4) Set the BUZOE flag of the oscillation stabilization wait control register to (DLYCTR) "0" to clear, and PD5 pin outputs low level.

Setup of the buzzer output ON should be done after setup of the buzzer frequency.
When the low oscillation clock (fx) dividing is selected as the buzzer output frequency and the buzzer output is switched ON from OFF, the buzzer dividing counter is not cleared unless more than 1clock of the low oscillation clock is secured.

Chapter 11 Serial interface 0

11

11.1 Overview

This LSI contains a serial interface 0 that can be used for both communication types of clock synchronous and UART (full duplex).

And the pin is changable to A (port0 : P00/SBO0A/TXD0A, P01/SBI0A/RXD0A, P02/SBT0A), or B (port9 : P90/SBO0B/TXD0B, P91/SBI0B/RXD0B, P92/SBT0B)

On this text, if there are not much differences between port A and port B on the operation, port A and B are omitted.

11.1.1 Functions

Table:11.1.1 shows functions of serial interface 0.

Table:11.1.1 Serial Interface 0 functions

Communication style	Clock synchronous	UART (full duplex)
Interrupt	SC0TIRQ	SC0TIRQ(on transmission completion) SC0RIRQ(on reception completion)
Used pins	SBO0,SBI0,SBT0	TXD0, RXD0
3 channels type	O	-
2 channels type	O(SBO0,SBT0)	O
1 channel type	-	TXD0
Specification of transfer bit count/ Frame selection	1 to 8 bits	7 bit +1STOP 7 bit +2STOP 8 bit +1STOP 8 bit +2STOP
Selection of parity bit	-	O
Parity bit control	-	0 parity 1 parity odd parity even parity
Selection of start condition	O	Only "enable start condition" is available
Specification of the first transfer bit	O	O
Specification of input edge/ output edge	O	-

SBO0 output control after final data moved out	H/L/final data hold	-
At the standby mode	Only slave reception is available	-
Continuous operation	O	O
Internal clock 1/8 dividing	O	Only 1/8 dividing is available
Clock source	fosc/2 fosc/4 fosc/16 fosc/64 fs/2 fs/4 External clock Timer 2 output Timer 4 output	fosc/2 fosc/4 fosc/16 fosc/64 fs/2 fs/4 Timer 2 output Timer 4 output
Maximum transfer rate	5.0 MHz	300 kbps
fosc:Machine clock (High speed oscillation) fs:System clock		

Set the transfer rate slower than system clock (fs).

11.1.2 Block Diagram

■ Serial interface 0 Block Diagram

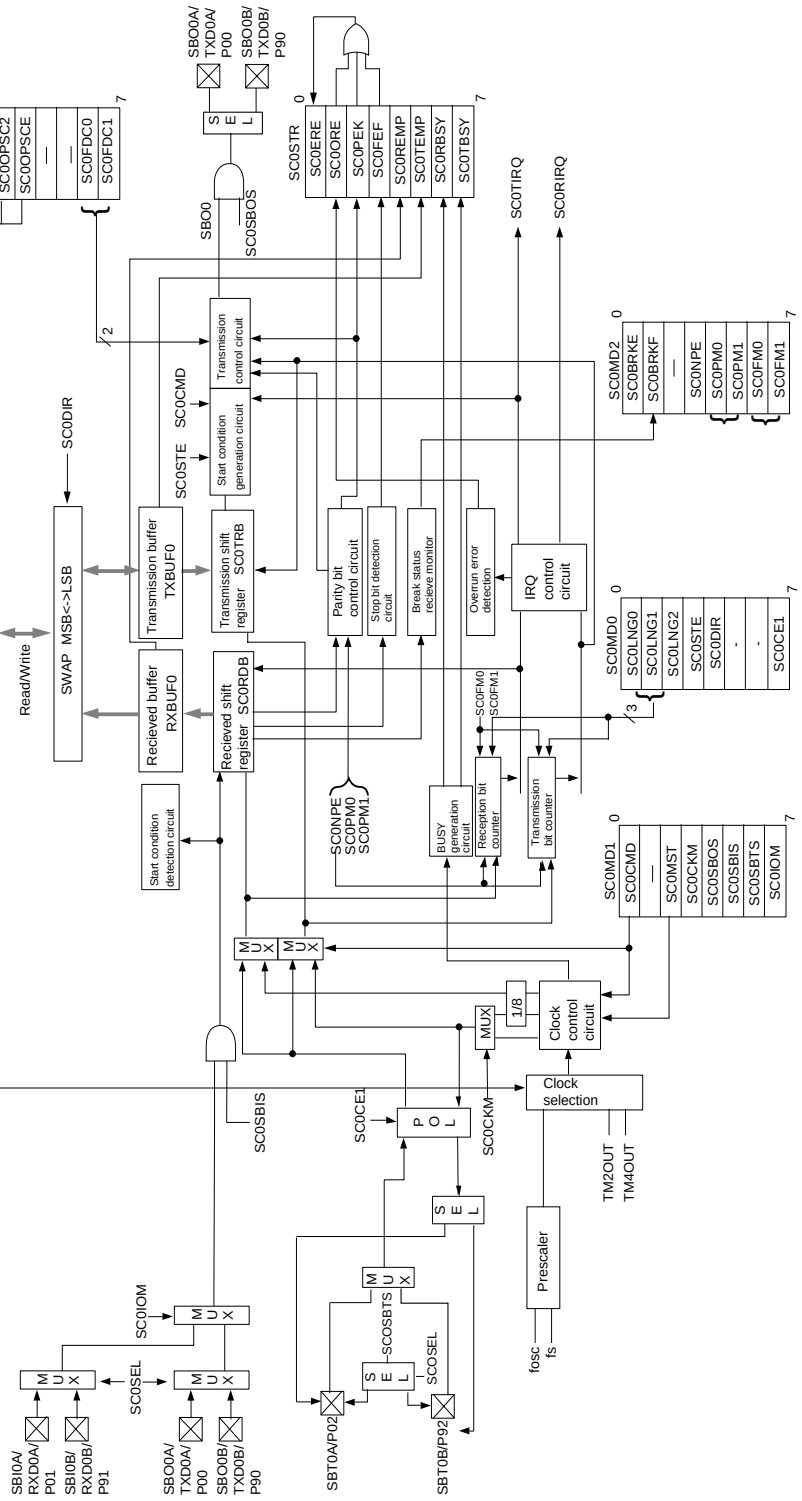


Figure:11.1.1 Serial interface 0 Block Diagram

11.2 Control Registers

11.2.1 Registers

Table:11.2.1 shows registers to control serial interface 0.

Table:11.2.1 Serial interface 0 Control Registers

Register	Address	R/W	Function	Page
SC0MD0	0x03F8F	R/W	Serial interface 0 mode register 0	XI-7
SC0MD1	0x03F90	R/W	Serial interface 0 mode register 1	XI-8
SC0MD2	0x03F91	R/W	Serial interface 0 mode register 2	XI-9
SC0MD3	0x03F92	R/W	Serial interface 0 mode register 3	XI-10
SC0STR	0x03F93	R	Serial interface 0 status register	XI-11
RXBUF0	0x03F94	R	Serial interface 0 received data buffer	XI-6
TXBUF0	0x03F95	R/W	Serial interface 0 transmission data buffer	XI-6
SCSEL	0x03F4F	R/W	Serial I/O pin switching control register	XI-12
P0ODC	0x03F1C	R/W	Port 0 Nch open drain control register	IV-9
P0DIR	0x03F30	R/W	Port 0 direction control register	IV-8
P0PLU	0x03F40	R/W	Port 0 pull-up control register	IV-9
P9ODC	0x03F4C	R/W	Port 9 Nch open drain control register	IV-92
P9DIR	0x03F39	R/W	Port 9 direction control register	IV-91
P9PLU	0x03F49	R/W	Port 9 pull-up control register	IV-92
SC0RICR	0x03FF2	R/W	Serial 0 UART reception interrupt control register	III-38
SC0TICR	0x03FF3	R/W	Serial 0 UART transmission interrupt control register	III-39

R/W:Readable/ Writable

R:Readable only

11.2.2 Data Buffer Registers

Serial interface 0 has each 8-bit data buffer register for transmission, and for reception.

■ Serial interface 0 Received Data Buffer (RXBUF0:0x03F94)

bp	7	6	5	4	3	2	1	0
Flag	RXBUF07	RXBUF06	RXBUF05	RXBUF04	RXBUF03	RXBUF02	RXBUF01	RXBUF00
Reset	X	X	X	X	X	X	X	X
Access	R	R	R	R	R	R	R	R

■ Serial interface 0 Transmission Data Buffer (TXBUF0:0x03F95)

bp	7	6	5	4	3	2	1	0
Flag	TXBUF07	TXBUF06	TXBUF05	TXBUF04	TXBUF03	TXBUF02	TXBUF01	TXBUF00
Reset	X	X	X	X	X	X	X	X
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

11.2.3 Mode Registers

■ Serial interface 0 Mode Register 0 (SC0MD0:0x03F8F)

bp	7	6	5	4	3	2	1	0
Flag	SC0CE1	-	-	SC0DIR	SC0STE	SC0LNG2	SC0LNG1	SC0LNG0
Reset	0	-	-	0	0	1	1	1
Access	R/W	-	-	R/W	R/W	R/W	R/W	R/W

bp	Flag	Description
7	SC0CE1	Transmission data output edge 0:falling 1:rising Reception data input edge 0:rising 1:falling
6-5	-	-
4	SC0DIR	First bit to be transferred 0:MSB first 1:LSB first
3	SC0STE	Start condition selection 0:Disable start condition 1:Enable start condition
2-0	SC0LNG2 SC0LNG1 SC0LNG0	Transfer bit 000:1bit 001:2bit 010:3bit 011:4bit 100:5bit 101:6bit 110:7bit 111:8bit

■ Serial interface 0 Mode Register 1(SC0MD1:0x03F90)

bp	7	6	5	4	3	2	1	0
Flag	SC0IOM	SC0SBTS	SC0SBIS	SC0SBOS	SC0CKM	SC0MST	-	SC0CMD
Reset	0	0	0	0	0	0	-	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	-	R/W

bp	Flag	Description
7	SC0IOM	Serial data input selection 0:Data input from SBI0 (RXD0) 1:Data input from SBO0 (TXD0)
6	SC0SBTS	SBT0 pin function selection 0:Port 1:Transfer clock I/O
5	SC0SBIS	Serial input control selection 0:Input "1" 1:Input serial
4	SC0SBOS	SBO0(TXD0) pin function 0:Port 1:Output serial data
3	SC0CKM	8 cycle of transfer clock selection 0:No 8 cycle 1:8 cycle
2	SC0MST	Clock master/ slave selection 0:Clock slave 1:Clock master
1	-	-
0	SC0CMD	Synchronous serial/ full duplex UART selection 0:Synchronous serial 1:full duplex UART

■ Serial interface 0 Mode Register 2 (SC0MD2:0x03F91)

bp	7	6	5	4	3	2	1	0
Flag	SC0FM1	SC0FM0	SC0PM1	SC0PM0	SC0NPE	-	SC0BRKF	SC0BRKE
Reset	0	0	0	0	0	-	0	0
Access	R/W	R/W	R/W	R/W	R/W	-	R	R/W

bp	Flag	Description
7-6	SC0FM1 SC0FM0	Frame mode specification 00:7 data bit + 1 stop bit 01:7 data bit + 2 stop bit 10:8 data bit + 1 stop bit 11:8 data bit + 2 stop bit
5-4	SC0PM1 SC0PM0	Added bit specification Transmission Reception 00:Add "0" Check for 0 01:Add "1" Check for 1 10:Add odd parity Check for odd parity 11:Add even parity Check for even parity
3	SC0NPE	Parity enable 0:Enable parity bit 1:Disable parity bit
2	-	-
1	SC0BRKF	Break status receive monitor 0:Data reception 1:Break reception
0	SC0BRKE	Break status transmit control 0:Data transmission 1:Break transmission

■ Serial interface 0 Mode Register 3 (SC0MD3:0x03F92)

bp	7	6	5	4	3	2	1	0
Flag	SC0FDC1	SC0FDC0	-	-	SC0PSCE	SC0PSC2	SC0PSC1	SC0PSC0
Reset	0	0	-	-	0	0	0	0
Access	R/W	R/W	-	-	R/W	R/W	R/W	R/W

bp	Flag	Description
7-6	SC0FDC1 SC0FDC0	Output selection after SBO0 final data transmission 00:Fix at "1" (High) output 01:Final data hold 10:Fix at "0" (Low) output 11:Reserved
5-4	-	-
3	SC0PSCE	Prescaler count control 0:Count is forbidden 1:Count is allowed
2-0	SC0PSC2 SC0PSC1 SC0PSC0	Selection clock 000:fosc/2 001:fosc/4 010:fosc/16 011:fosc/64 100:fs/2 101:fs/4 110:Timer 2 output 111:Timer 4 output

■ Serial interface 0 Status Register (SC0STR:0x03F93)

bp	7	6	5	4	3	2	1	0
Flag	SC0TBSY	SC0RBSY	SC0TEMP	SC0REMP	SC0FEF	SC0PEK	SC0ORE	SC0ERE
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R

bp	Flag	Description
7	SC0TBSY	Serial bus status 0:Other use 1:Serial transmission in progress
6	SC0RBSY	Serial bus status 0:Other use 1:Serial reception in progress
5	SC0TEMP	Transfer buffer empty flag 0:Empty 1:Full
4	SC0REMP	Receive buffer empty flag 0:Empty 1:Full
3	SC0FEF	Framing error detection 0:No error 1:Error
2	SC0PEK	Parity error detection 0:No error 1:Error
1	SC0ORE	Overrun error detection 0:No error 1:Error
0	SC0ERE	Error monitor flag 0:No error 1:Error

■ Serial I/O Pin Switching Register (SCSEL:0x03F4F)

bp	7	6	5	4	3	2	1	0
Flag	-	-	-	-	SC3SEL	-	-	SC0SEL
Reset	-	-	-	-	0	-	-	0
Access	-	-	-	-	R/W	-	-	R/W

bp	Flag	Description
7-4	-	-
3	SC3SEL	Serial 3 I/O pin switching 0:P93-P95 1:P33-P35
2-1		
0	SC0SEL	Serial 0 I/O pin switching 0:P90-P92 1:P00-P02

11.3 Operation

Serial interface 0 can be used for both clock synchronous and full duplex UART.

11.3.1 Clock Synchronous Serial Interface

■ Activation Factor for Communication

Table:11.3.1 shows activation factors for communication. At master communication, the transfer clock is generated by setting data to the transmission data buffer TXBUF0, or by receiving a start condition. Except during communication, the input signal from SBT0 pin is masked to prevent errors by noise or so.This mask can be released automatically by setting a data to TXBUF0 (access to the TXBUF0 register), or by inputting a start condition to the data input pin. Therefore, at slave communication, set data to TXBUF0, or input an external clock after a start condition is input.

However, the external clock should be input after more than 3.5 transfer clock interval after the data set to TXBUF0. This wait time is needed to load the data from TXBUF0 to the internal shift register.

Table:11.3.1 Synchronous Serial Interface Activation Factor

	Activation factor	
	Transmission	Reception
At master	Set transmission data	Set dummy data
		Input start condition
At slave	Input clock after transmission data is set	Input clock after dummy data is set
		Input clock after start condition is input

■ Transfer Bit Setup

The transfer bit count is selected from 1 to 8 bits. Set them by the SC0LNG 2 to 0 flag of the SC0MD0 register (at reset:111). The SC0LNG2 to 0 flag holds the former set value until it is set again.

Except during communication, SBT0 pin is masked to prevent errors by noise. At slave communication, set data to TXBUF0 or input a clock to SBT0 pin after a start condition is input.

To communicate properly, more than 3.5 transfer clock after the data set to TXBUF0 is needed to input the external clock.

■ Start Condition Setup

The SC0STE flag of the SC0MD0 register sets if a start condition is enabled or not.

The start condition is regarded that when SC0CE1 flag of SC0MD0 is set to "0" and a clock line (SBT0 pin) is "H", data line (SBI0 pin (with 3 lines) or SBO0 pin (with 2 lines)) is changed from "H" to "L". Also, it is regarded that when SC0CE1 flag is set to "0" and a clock line (SBT0 pin) is "L", data line (SBI0 pin (with 3 lines) or SBO0 pin (with 2 lines)) is changed from "H" to "L".

Both the SC0SBOS flag and the SC0SBIS flag of the SC0MD1 register should be set to "0", before the start condition setup is changed.

At the selection of the start condition "enable" and master transmission / reception, after the start condition output, start condition is input from the slave, then data transmission is generated.

■ First Transfer Bit Setup

The SC0DIR flag of the SC0MD0 register can set the transfer bit. MSB first or LSB first can be selected.

■ Transmission Data Buffer

The transmission data buffer, TXBUF0 is a buffer of reserve that stores data to load the internal shift register. Data to be transferred should be set to the transmission data buffer, TXBUF0, to be loaded to the internal shift register automatically. The data load time of 3.5 transfer clock is needed to load the data. On loading, setting the data to TXBUF0 again may cause error. On loading or not is determined by monitoring the transmission buffer empty flag of the SC0STR. When the data is set to TXBUF0, SC0TEMP flag is set to "1" and when loading is finished, it is cleared "0" automatically.

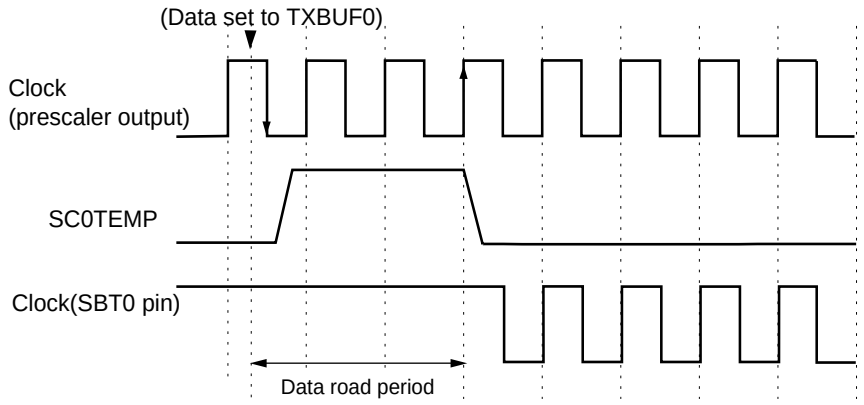


Figure:11.3.1

■ Received Date Buffer

The received data buffer RXBUF0 is a buffer of reserve that pushed the received data in the internal shift register. After the communication complete interrupt SC0TIRQ is generated, all data stored in the internal shift register are stored to the received data buffer RXBUF0 automatically. RXBUF0 can store data up to 1 byte. RXBUF0 is rewritten in every time when communication is completed, so read out data of RXBUF0 till the next receive is completed. The received data buffer empty flag SC0REMP is set to "1" at the same time SC0TIRQ is generated. SC0REMP is cleared to "0" after RXBUF0 is read out.

If a start condition is input to restart during communication, the transmission data is not valid. Set the transmission data to TXBUF0 again to operate the transmission again.

RXBUF0 is rewritten every time when communication is completed. At continuous communication, data of RXBUF0 should be read out until the next reception is completed.

■ Transfer Bit Count and First Transfer Bit

When the transfer bit is 1 bit to 7bit, the data storing method to the transmission data buffer TXBUF0 is different, depending on the first transfer bit selection. At MSB first, use the upper bits of TXBUF0 for storing. When there are 6 bits to be transferred, as shown on Figure:11.3.2, if data "A" to "F" are stored to bp2 to bp7 of TXBUF0, the transmission is operated from "F" to "A". At LSB first, use the lower bits of TXBUF0 for storing. When there are 6 bits to be transferred, as shown on Figure:11.3.3, if data "A" to "F" are stored to bp0 to bp5 of TXBUF0, the transmission is operated from "A" to "F".

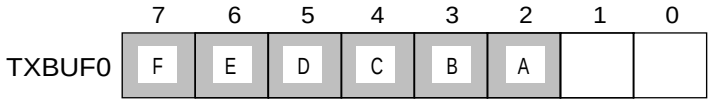


Figure:11.3.2 Transfer Bit Count and First Transfer Bit (starting with MSB)

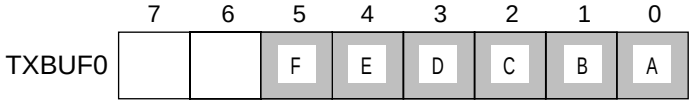


Figure:11.3.3 Transfer Bit Count and First Transfer Bit (starting with LSB)

■ Receive Bit Count and First Transfer Bit

When the transfer bit count is 1 bit to 7 bits, the data storing method to the received data buffer RXBUF0 is different depending on the first transfer bit. At MSB first, data are stored to the lower bits of RXBUF0. When there are 6 bits to be transferred, as shown on figure Figure:11.3.4, if data "A" to "F" are stored to bp0 to bp5 of RXBUF0, the transmission is operated from "F" to "A". At LSB first, data are stored to the upper bits of RXBUF0. When there are 6 bits to be transferred, as shown on Figure:11.3.5, if data "A" to "F" are stored to bp2 to bp7 of RXBUF0, the transmission is operated from "A" to "F".

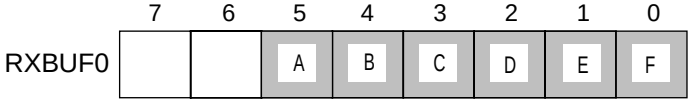


Figure:11.3.4 Receive Bit Count and Transfer First Bit (starting with MSB bit)

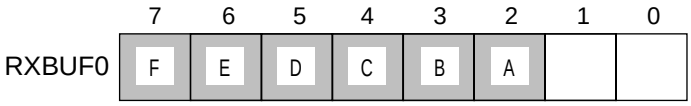


Figure:11.3.5 Receive Bit Count and Transfer First Bit (starting with LSB bit)

When the serial transfer bit is set between 1 to 7, the data except for received data of the specified transfer bit count is unknown. Use the received data after being masked by AND/ OR instruction.

■ Continuous Mode

This serial has a function for continuous communication. If data is set to the transmission data buffer TXBUF0 during communication, the transmission buffer empty flag SC0TEMP is automatically set to interrupt SC0TIRQ is generated after the former data is set. Data setup to TXBUF0 should be done till the communication complete interrupt SC0TIRQ is generated after the data is loaded to the internal shift register. At master communication, there is output after the pension of communication for 4 transfer clocks till the next transmission clock is output after the SC0TIRQ generation.

■ ATC Automatic Continuous Transfer

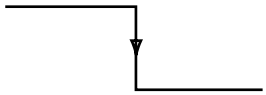
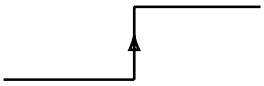
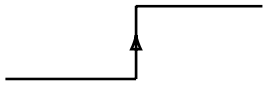
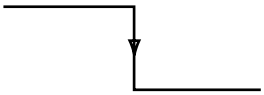
This serial enables the start-up by the data automatic transfer (ATC1). On start-up by ATC1, 255 bytes data transfer can be operated.

Refer to [chapter 18 Automatic Transfer Controller : overview : transfer mode 8 to 9 about the generation of ATC1.]

■ Input Edge/ Output Edge Setup

The SC0CE1 flag of the SC0MD0 register set an output edge of the transmission data, an input edge of the received data. As the SC0CE1 flag = "0", the transmission data is output at the falling edge, and as "1", output at the rising edge. As SC0CE1 = "0", the received data is received at the inversion edge to the output edge of transmission data, and as "1", stored at the same edge.

Table:11.3.2 Transmission Data Output Edge and Received Data Input Edge

SC0CE1	Transmission data output edge	Received data input edge
0		
1		

■ Clock Setup

The SC0PSC2 to 0 of the SC0MD3 register selects the clock source from the special prescaler and timer 2, timer 4 (2 lines) output. The special prescaler starts its operation after the SC0PSCE flag of the SC0MD1 register selects "enable count". The SC0MST flag of the SC0MD1 register can select the internal clock (clock master), or the external clock (clock slave). Even if the external clock is selected, set the internal clock that has the same clock cycle or lower to the external clock, by the SC0MD3 register. Here is the internal clock source that can be set by the SC0MD3 register. Also, the SC0CKM flag of the SC0MD1 register can divide the internal clock by 8.

Table:11.3.3 Synchronous Serial Interface Clock Source

	serial 0
Clock source (internal clock)	fosc/2
	fosc/4
	fosc/16
	fosc/64
	fs/2
	fs/4
	Timer 2 output
	Timer 4 output

When the clock setup is switched, the SC0SBIS flag and SC0SBOS flag of the SC0MD1 register should be set to "0".

When the slave reception is done with enabled start condition, set the speed of the transfer clock slower than the system clock.

■ Switching Unused Pins

Used pin is switched A (SBO0A, SBI0A, SBT0A) or B (SBO0B, SBI0B, SBT0B) at the SC0SL flag of yjr SCSEL register.

■ Data Input Pin Setup

3 channels type (clock pin (SBT0 pin), data output pin (SBO0 pin), data input pin (SBI0 pin)) or 2 channels type (clock pin (SBT0 pin), data I/O pin (SBO0 pin)) can be selected as a communication mode. SBI0 pin can be used for only serial data input. SBO0 pin can select serial data input or output. The SC0IOM flag of the SC0MD1 register can select if the serial data is input to SBI0 pin or SBO0 pin. When "data input from SBO0 pin" is selected to set the 2 lines type, the P0DIR0 flag of the P0DIR register controls direction of SBO0 pin to switch transmission/ reception. At this time, SBI0 pin can be used as a general port, too.

The transfer speed should be up to 5.0MHz.
If the transfer clock is over 5.0 MHz, the transmission data may not be sent correctly.

At reception, if SC0IOM of the SC0MD1 register is set to "1" and "serial data input from SBO0" is selected, SBI0 pin can be used as a general port.

■ Reception Buffer Empty Flag

After reception is completed (communication complete interrupt SC0TIRQ is generated), data is automatically stored to RXBUF0 from the internal shift register. If data is stored to the shift register RXBUF0 when the SC0SBIS of the SC0MD1 register is set to "serial input", the reception buffer empty flag SC0REMP of the SC0STR register is set to "1". This indicates that the received data is going to read out. SC0REMP is cleared to "0" by reading out the data of RXBUF0.

■ Transmission Buffer Empty Flag

During the communication (after setting data to TXBUF0 and before the communication complete interrupt SC0TIRQ is generated) if any data is set to TXBUF0 again, the transmission buffer empty flag SC0REMP of the SC0STR register is set to "1". This indicates that the next transmission data is going to be loaded. Data is loaded to the inside shift register from TXBUF0 by generation of SC0TIRQ, and the next transfer is started as SC0TEMP is cleared to "0".

■ Overrun Error and Error Monitor Flag

After reception complete, if the next data has been already received before reading out of the data of the received data buffer RXBUF0, overrun error is generated and the SC0ORE flag of the SC0STR register is set to "1". At the same time, the error monitor flag SC0ERE is set to indicate that error is occurred on reception. The SC0ERE flag is not cleared till the next communication complete interrupt SC0TIRQ is generated after loading data of the RXBUF0. SC0ERE is cleared as SC0ORE flag is cleared. These error flags have no effect on communication operation.

■ Reception BUSY Flag

If the data is set to the TXBUF0 or recognized the start condition when the SC0SBIS flag of the SC0MD1 register is set to "serial data input", the BUSY flag SC0RBSY of the SC0STR register is set to "1". And, on the generation of the communication complete interrupt SC0TIRQ, the flag is cleared to "0". And, during continuous communication, the SC0RBSY flag is always set. If the transmission buffer empty flag SC0TEMP is cleared to "0" as the communication complete interrupt SC0TIRQ is generated, SC0RBSY is cleared to "0". If the SC0SBIS flag is set to "0" during communication, the SC0RBSY flag is cleared to "0".

■ Transmission BUSY Flag

Data is set to the TXBUF0 or recognized the start condition when the SC0SBOS flag of the SC0MD1 register is set to "serial data output", if the SC0SBOS flag of the SC0MD1 register is "1", SC0TBSY flag of the SC0STR register is set. And, on the generation of the communication complete interrupt SC0TIRQ, the flag is cleared "0". And, during continuous communication, the SC0TBSY flag is always set. If the transmission buffer empty flag SC0TEMP is cleared to "0" as the communication complete interrupt SC0TIRQ is generated,SC0TBSY is cleared to "0". If the SC0SBOS flag is set to "0" during communication, the SC0TBSy flag is cleared to "0".

■ Emergency Reset

This serial interface contains emergency reset for abnormal operation. For emergency reset, the SC0SBOS flag and the SC0SBIOS flag of the SC0MD1 register should be set to "0" (SBO0 pin:port, input data:"1" input).

At emergency reset, the status register (the SC0BRKF flag of the SC0MD2 register, all flags of the SC0STR register) are initialized as they are set at reset, but the control register holds the set value.

■ Last Bit of Transfer Data

Table:11.3.4 shows the data output holding period of the last bit at transmission, and the minimum data input period of the last bit at reception. The internal clock should be set up at slave to keep the data hold time at reception.

Table:11.3.4 Last Bit Data Length of Transfer Data

	The last bit data holding period at transmission	The last data input period at reception
At master	1 bit data length	1 bit data length (Minimum)
At slave	[1 bit data length of external clock × 1/2] + [internal clock cycle × (1/2-3/2)]	

In the case of disabled start condition (at SC0STE flag = 0), the SBO0 output after the data output holding period of the final bit can be set as Table:11.3.5 by the setting value of the SC0FDC1 to 0 flag of the SC0MD3 register.

After released the reset, despite of the setting value of the SC0FDC1 to 0 flag, output before the serial transfer is "H". In the case of the enabled start condition (at SC0STE flag = 1), "H" is output despite of the setting value of the SC0FDC1 to 0.

Table:11.3.5 SBO0 Output after the Data Output Holding Period of the Last Bit (without start condition)

SC0FDC1 flag	SC0FDC0 flag	SBO0 output after the data output holding period of the last bit
0	0	"1"(High) output fix
1	0	"0"(Low) output fix
0	1	Last data holding
1	1	Reserved

■ Other Control Flag Setup

Table:11.3.6 shows flags that are not used at clock synchronous communication. So, they are not needed to set or monitor.

Table:11.3.6 Other Control Flag

Register	Flag	Detail
SC0MD2	SC0BRKE	Break status transmission control
	SC0BRKF	Break status reception monitor
	SC0NPE	Parity enable
	SC0PM1 to 0	Added bit specification
	SC0FM1 to 0	Frame mode specification
SC0STR	SC0PEK	Parity error detection
	SC0FEF	Frame error detection

■ Transmission Timing

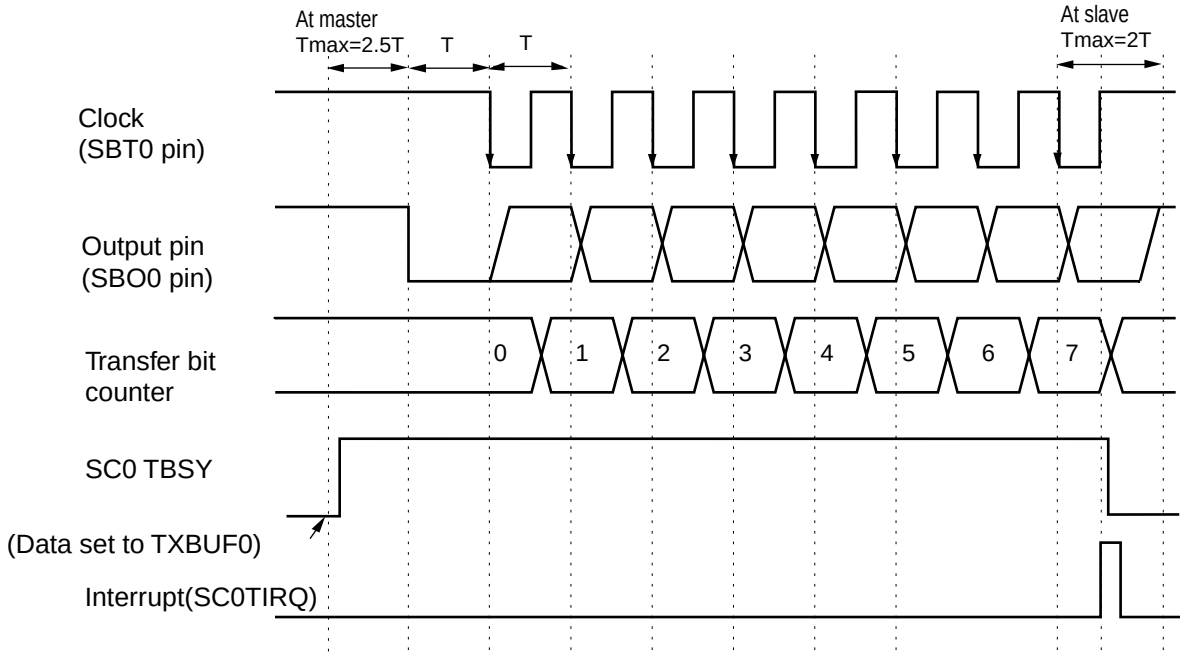


Figure:11.3.6 Transmission Timing (at falling edge, start condition is enabled)

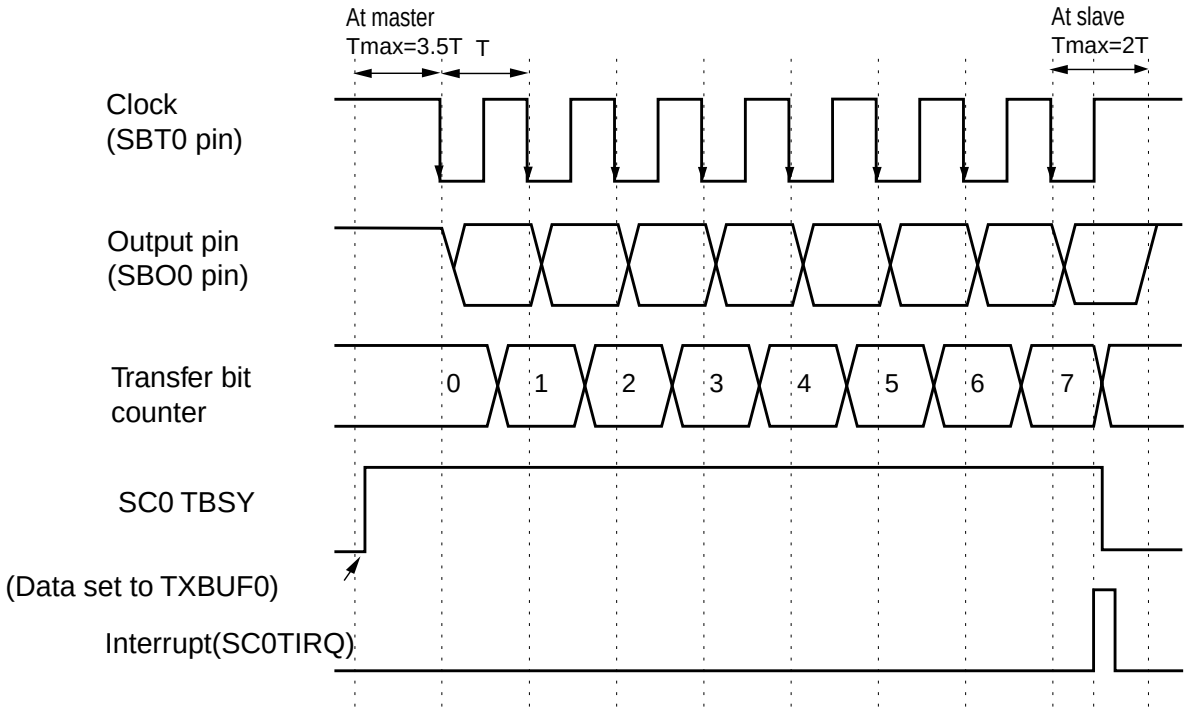


Figure:11.3.7 Transmission Timing (at falling edge, start condition is disabled)

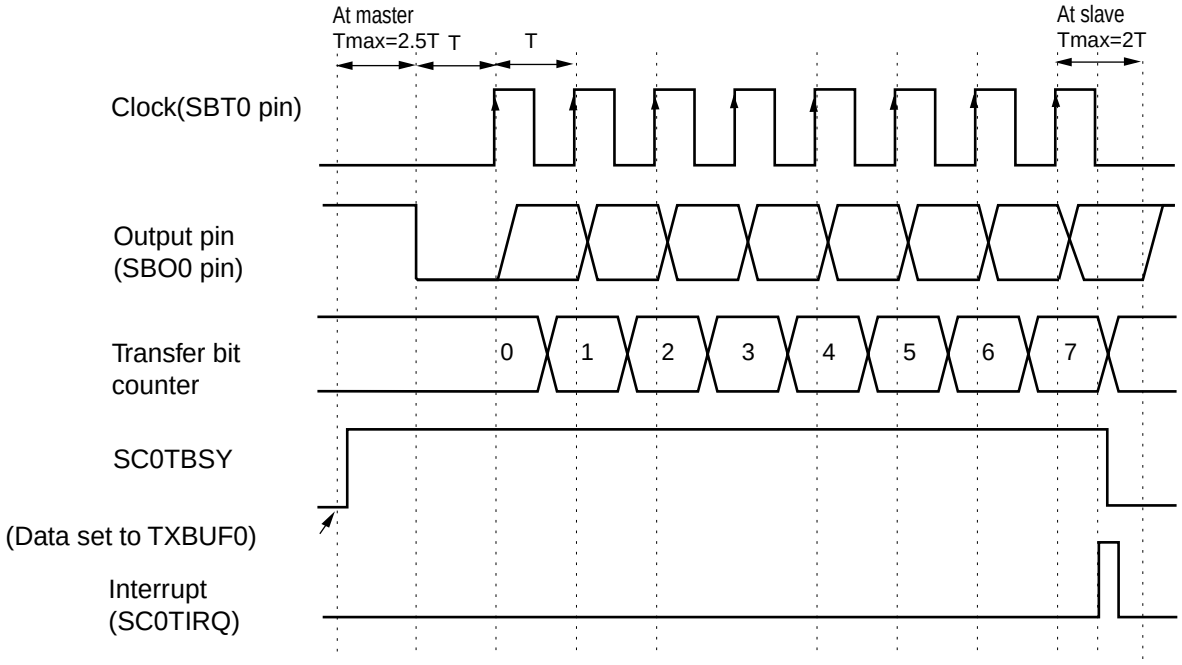


Figure:11.3.8 Transmission Timing (at rising edge, start condition is enabled)

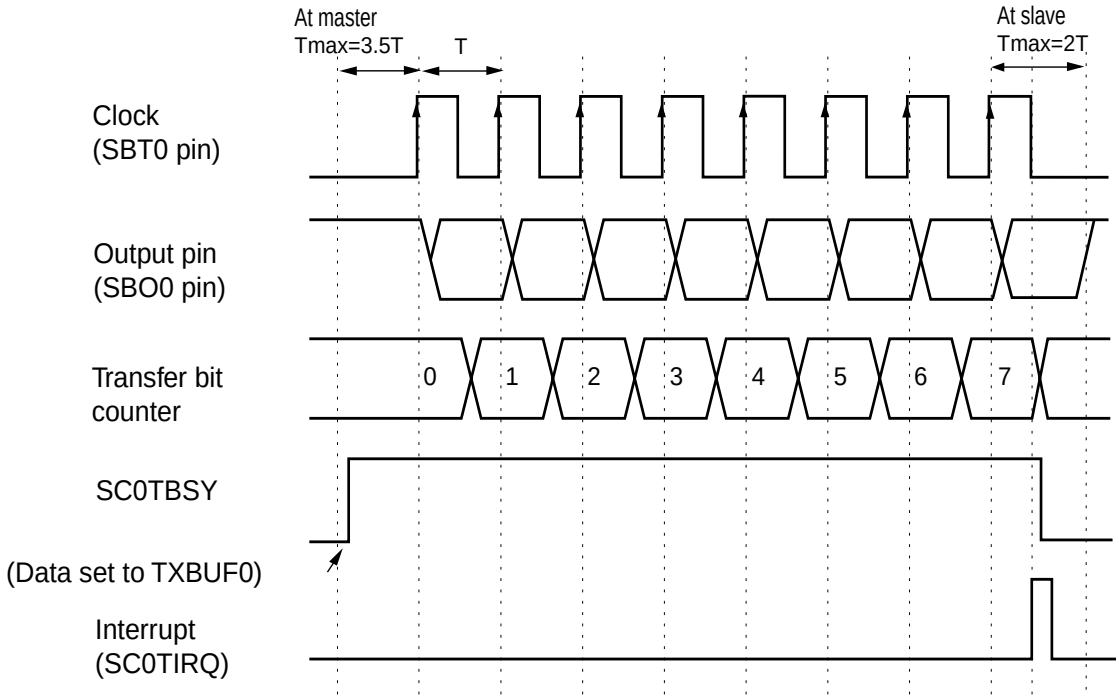


Figure:11.3.9 Transmission Timing (at rising edge, start condition is disabled)

■ Reception Timing

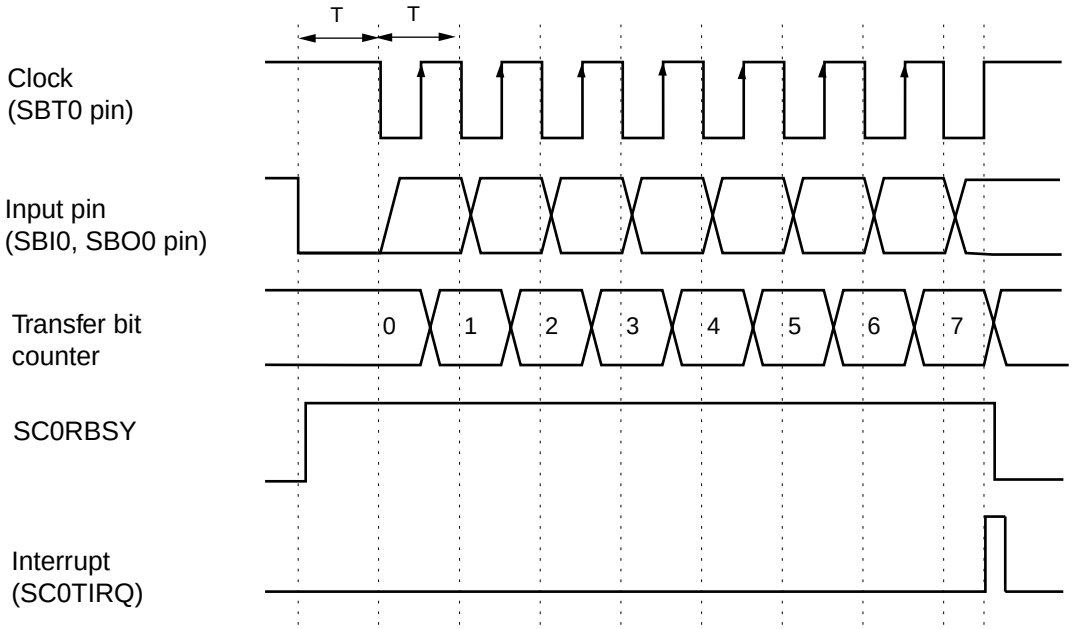


Figure:11.3.10 Reception Timing (at rising edge, start condition is enabled)

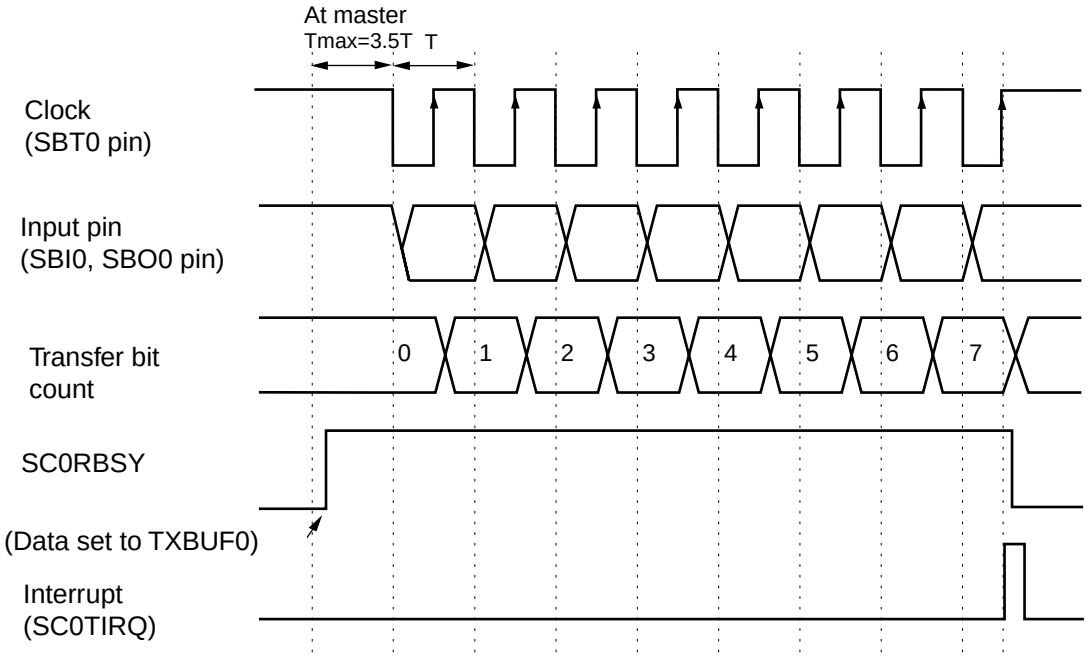


Figure:11.3.11 Reception Timing (at rising edge, start condition is disabled)

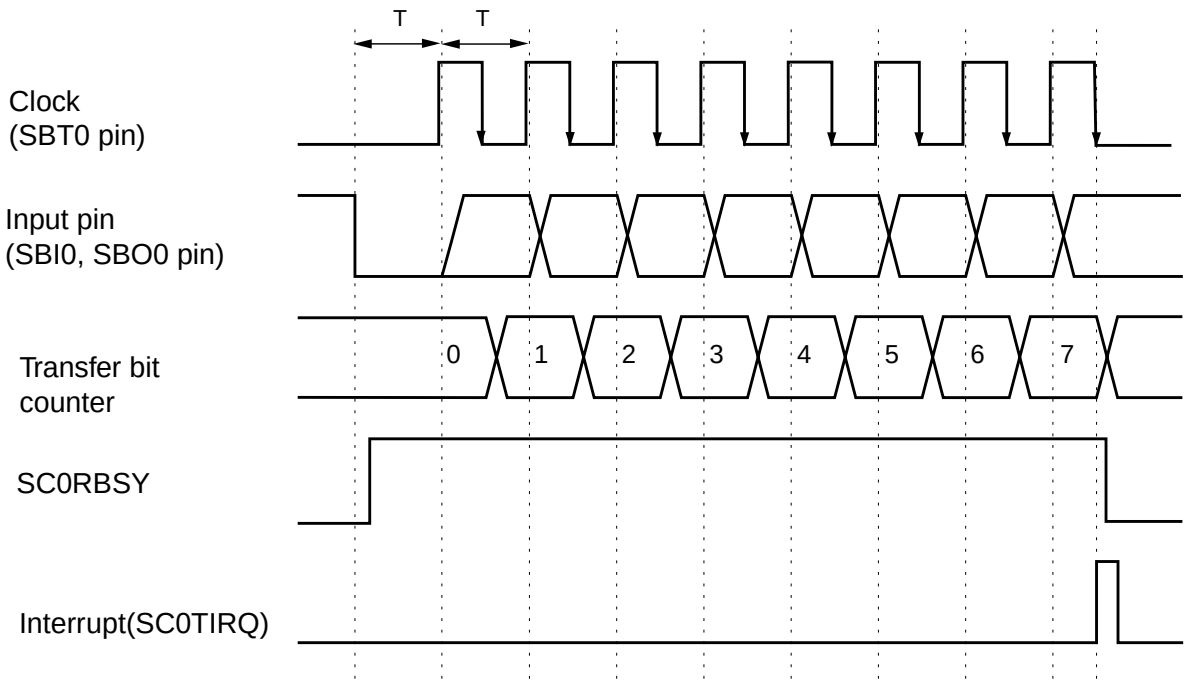


Figure:11.3.12 Reception Timing (at falling edge, start condition is enabled)

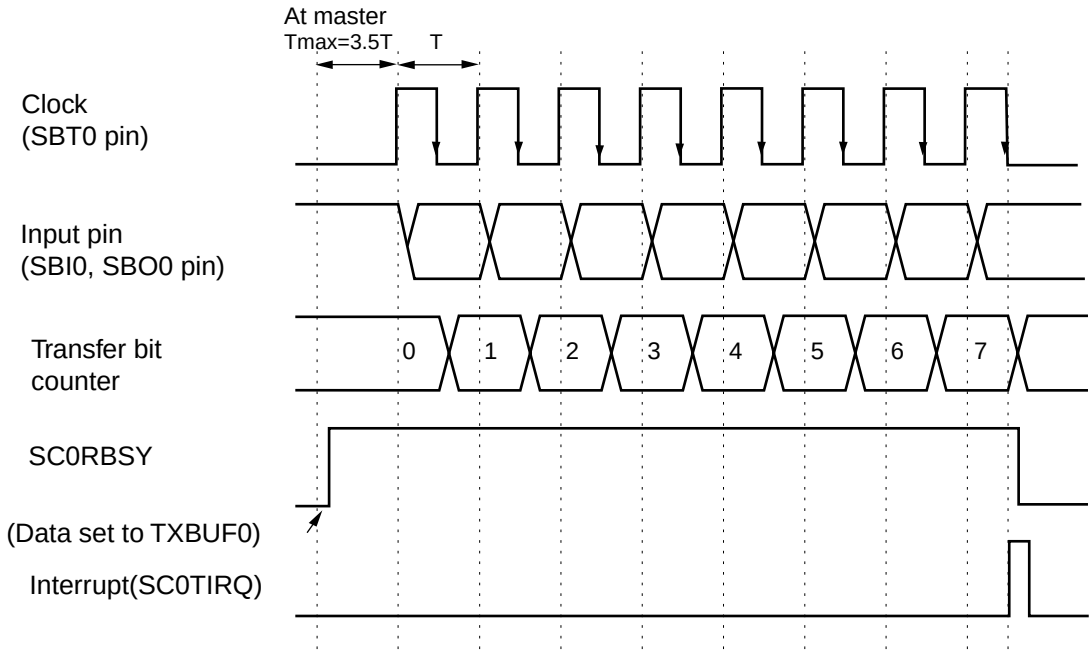


Figure:11.3.13 Reception Timing (at falling edge, start condition is disabled)

■ Transmission/ Reception Timing

When transmission and reception are operated at the same time, set the SC0CE1 flag of the SC0MD0 register to "0" or "1". Data is received at the opposite output edge of the transmission data, so that the input edge of the received data should be the opposite output edge of the transmission data from the other side.

Also, in the case transmission/ reception is done with the start condition, opposite of the communication should be done with the same condition to communicate properly.

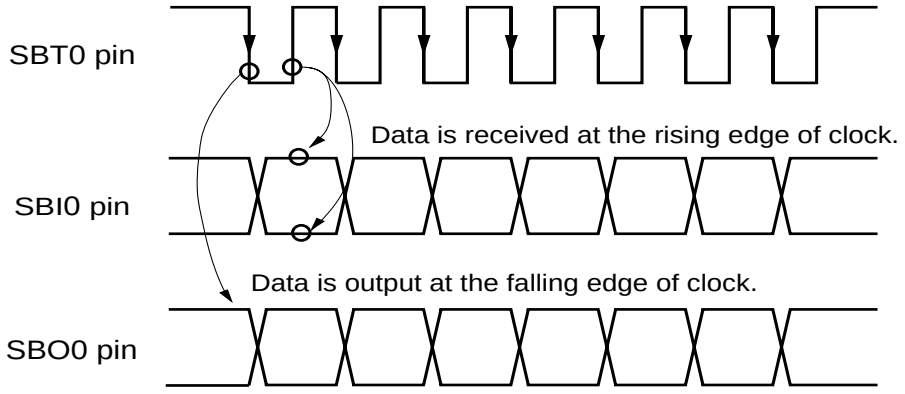


Figure:11.3.14 Transmission/ Reception Timing (Reception:at rising edge, Transmission:at falling edge)

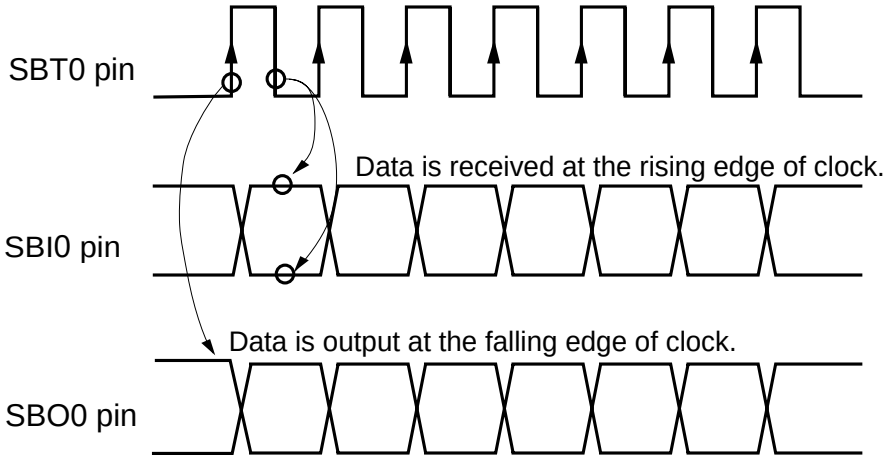


Figure:11.3.15 Transmission/ Reception Timing (Reception:at falling edge, Transmission:at rising edge)

■ Communication Function at Standby Mode

This serial interface has the following way about the return from the standby mode.

This serial interface can do the slave reception at the standby mode. CPU operation status can be recovered from standby to normal by the communication complete interrupt SC0TIRQ that is generated after the slave reception.

(At the standby mode, if the transfer bit count data is received once that is set by the SC0LNG2 to 0 flag of the SC0MD0 register, the continuous reception is not available because the next data is not allowed.) The received data should be read out from the received data buffer RXBUF0 after recovering the normal mode.

In the reception at the standby mode, the communication with enabled start condition is not available. Disable the start condition. The dummy data should be set to the transmission data buffer TXBUF0 before the transition to the standby mode.

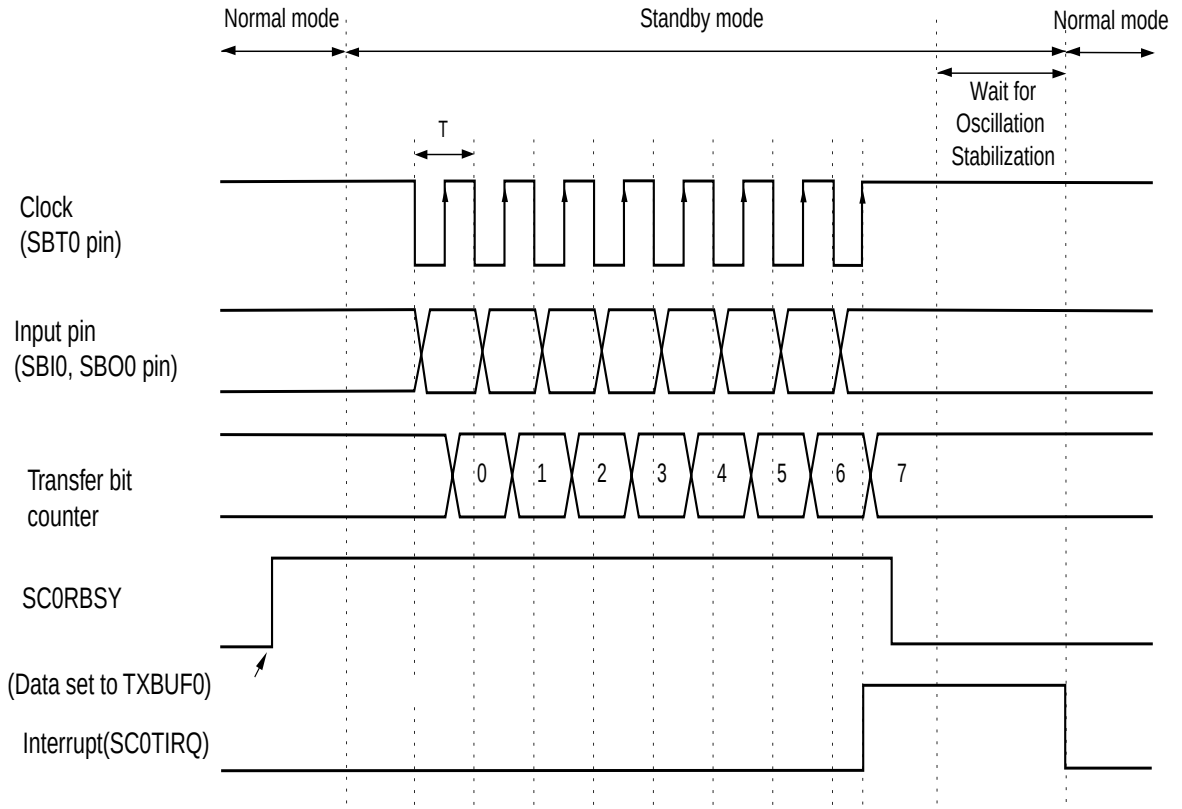


Figure:11.3.16 Reception Timing at Standby Mode (Reception:at rising edge, start condition is disabled)

■ Pins Setup (with 3 channels at transmission)

Table:11.3.7 shows the setup for synchronous serial interface pin with 3 channels (SBO0 pin, SBI0 pin, SBT0 pin) at transmission.

Table:11.3.7 Setup for Synchronous Serial Interface Pin (with 3 channels, at transmission)

<table>
<tr><td rowspan="3">Setup item</td><td>Data output pin</td><td>Data input pin</td><td colspan="2">Clock I/O pin</td></tr>
<tr><td rowspan="2">SBO0A pin/
SBO0B pin</td><td rowspan="2">SBI0A pin/
SBI0B pin</td><td colspan="2">SBT0A pin/SBT0B pin</td></tr>
<tr><td>Clock master</td><td>Clock slave</td></tr>
<tr><td colspan="3">SC0MD1(SC0MST)</td></tr>
<tr><td>Port pin</td><td>P00/P90</td><td>P01/P91</td><td colspan="2">P02/P92</td></tr>
<tr><td rowspan="2">Port pin selection</td><td colspan="4">Select used pin (A, B)</td></tr>
<tr><td colspan="4">SCSEL(SC0SEL)</td></tr>
<tr><td rowspan="2">SBI0/SBO0 selection</td><td colspan="2">SBI0/SBO0 independent</td><td colspan="2" rowspan="2">-</td></tr>
<tr><td colspan="2">SC0MD1(SC0IOM)</td></tr>
<tr><td rowspan="2">Function</td><td>Serial data output</td><td>"1" input</td><td>Serial clock I/O</td><td>Serial clock I/O</td></tr>
<tr><td>SC0MD1(SC0SBOS)</td><td>SC0MD1(SC0SBIS)</td><td colspan="2">SC0MD1(SC0SBTS)</td></tr>
<tr><td rowspan="2">Style</td><td>Push-pull/ Nch open-drain</td><td rowspan="2">-</td><td>Push-pull/ Nch open-drain</td><td>Push-pull/ Nch open-drain</td></tr>
<tr><td>P0ODC(P0ODC0)
/P9ODC(P9ODC0)</td><td colspan="2">P0ODC(P0ODC2)/P9ODC(P9ODC2)</td></tr>
<tr><td rowspan="2">I/O</td><td>Output mode</td><td rowspan="2">-</td><td>Output mode</td><td>Input mode</td></tr>
<tr><td>P0DIR(P0DIR0)
/P9DIR(P9DIR0)</td><td colspan="2">P0DIR(P0DIR2)/P9DIR(P9DIR2)</td></tr>
<tr><td rowspan="2">Pull-up setup</td><td>Added/ Not added</td><td rowspan="2">-</td><td>Added/ Not added</td><td>Added/ Not added</td></tr>
<tr><td>P0PLU(P0PLU0)
/P9PLU(P9PLU0)</td><td colspan="2">P0PLU(P0PLU2)/P9PLU(P9PLU2)</td></tr>
</table>

■ Pins Setup (with 3 channels, at reception)

Table:11.3.8 shows the setup for synchronous serial interface pin with 3 channels (SBO0 pin, SBI0 pin, SBT0 pin) at reception.

Table:11.3.8 Setup for Synchronous Serial Interface Pin (with 3 channels, at reception)

<table>
<tr><td rowspan="3">Setup item</td><td>Data output pin</td><td>Data input pin</td><td colspan="2">Clock I/O pin</td></tr>
<tr><td rowspan="2">SBO0A pin/
SBO0B pin</td><td rowspan="2">SBI0A pin/
SBI0B pin</td><td colspan="2">SBT0A pin/SBT0B pin</td></tr>
<tr><td>Clock master</td><td>Clock slave</td></tr>
<tr><td colspan="3">SC0MD1(SC0MST)</td></tr>
<tr><td>Port pin</td><td>P00/P90</td><td>P01/P91</td><td colspan="2">P02/P92</td></tr>
<tr><td rowspan="2">Port pin selection</td><td colspan="4">Select used pin (A, B)</td></tr>
<tr><td colspan="4">SCSEL(SC0SEL)</td></tr>
<tr><td rowspan="2">SBI0/SBO0 selection</td><td colspan="2">SBI0/SBO0 independent</td><td colspan="2" rowspan="2">-</td></tr>
<tr><td colspan="2">SC0MD1(SC0IOM)</td></tr>
<tr><td rowspan="2">Function</td><td>Port</td><td>Serial data input</td><td>Serial clock input/
output</td><td>Serial clock input/
output</td></tr>
<tr><td>SC0MD1(SC0SBOS)</td><td>SC0MD1(SC0SBIS)</td><td colspan="2">SC0MD1(SC0SBTS)</td></tr>
<tr><td rowspan="2">Style</td><td rowspan="2">-</td><td rowspan="2">-</td><td>Push-pull/ Nch open-drain</td><td>Push-pull/ Nch open-drain</td></tr>
<tr><td colspan="2">P0ODC(P0ODC2)/P9ODC(P9ODC2)</td></tr>
<tr><td rowspan="2">I/O</td><td rowspan="2">-</td><td>Input mode</td><td>Output mode</td><td>Input mode</td></tr>
<tr><td>P0DIR(P0DIR1)
/P9DIR(P9DIR1)</td><td colspan="2">P0DIR(P0DIR2)/P9DIR(P9DIR2)</td></tr>
<tr><td rowspan="2">Pull-up setup</td><td rowspan="2">-</td><td rowspan="2">-</td><td>Added/ Not added</td><td>Added/ Not added</td></tr>
<tr><td colspan="2">P0PLU(P0PLU2)/P9PLU(P9PLU2)</td></tr>
</table>

■ Pins Setup (with 3 channels, at transmission / reception)

Table:11.3.9 shows the setup for synchronous serial interface pin with 3 channels (SBO0 pin, SBI0 pin, SBT0 pin) at transmission / reception.

Table:11.3.9 Setup for Synchronous Serial Interface Pin (with 3 channels, at transmission / reception)

Setup item	Data output pin	Data input pin	Clock I/O pin	
	SBO0A pin/ SBO0B pin	SBI0A pin/ SBI0B pin	SBT0A pin/SBT0B pin	
			Clock master	Clock slave
			SC0SCMD1(SC0MST)	
Port pin	P00/P90	P01/P91	P02/P92	
Port pin selection	Select used pin (A, B)			
	SCSEL(SC0SEL)			
SBI0/SBO0 selection	SBI0/SBO0 independent		-	
	SC0MD1(SC0IOM)			
Function	Serial data output	Serial data input	Serial clock input/ output	Serial clock input/ output
	SC0MD1(SC0SBOS)	SC0MD1(SC0SBIS)	SC0MD1(SC0SBTS)	
Style	Push-pull/ Nch open-drain	-	Push-pull/ Nch open-drain	Push-pull/ Nch open-drain
	P0ODC(P0ODC0) /P9ODC(P9ODC0)		P0ODC(P0ODC2)/P9ODC(P9ODC2)	
I/O	Output mode	Input mode	Output mode	Input mode
	P0DIR(P0DIR0) P9DIR(P9DIR0)	P0DIR(P0DIR1) P9DIR(P9DIR1)	P0DIR(P0DIR2)/P9DIR(P9DIR2)	
Pull-up setup	Added/ Not added	-	Added/ Not added	Added/ Not added
	P0PLU(P0PLU0) /P9PLU(P9PLU0)		P0PLU(P0PLU2)/P9PLU(P9PLU2)	

■ Pins Setup (with 2 channels, at transmission)

Table:11.3.10 shows the setup for synchronous serial interface pin with 2 channels (SBO0 pin, SBT0 pin) at transmission. SBI0 pin can be used as a port.

Table:11.3.10 Setup for Synchronous Serial Interface Pin (with 2 channels, at transmission)

Setup item	Data output pin	Serial unused pin	Clock I/O pin	
	SBO0A pin/ SBO0B pin	SBI0A pin/ SBI0B pin	SBT0A pin/SBT0B pin	
			Clock master	Clock slave
			SC0SCMD1(SC0MST)	
Port pin	P00/P90	P01/P91	P02/P92	
Set port pin	Select used pin (A, B)			
	SCSEL(SC0SEL)			
SBI0/SBO0 selection	SBI0/SBO0 connection		-	
	SC0MD1(SC0IOM)			
Function	Serial data input	"1" input	Serial clock input/ output	Serialclock input/ output
	SC0MD1(SC0SBOS)	SC0MD1(SC0SBIS)	SC0MD1(SC0SBIS)	
Style	Push-pull/ Nch open-drain	-	Push-pull/ Nch open-drain	Push-pull/ Nch open-drain
	P0ODC(P0ODC0) /P9ODC(P9ODC0)		P0ODC(P0ODC2)/P9ODC(P9ODC2)	
I/O	Output mode	-	Output mode	Input mode
	P0DIR(P0DIR0) P6DIR(P6DIR0)		P0DIR(P0DIR2)/P9DIR(P9DIR2)	
Pull-up setup	Added/ Not added	-	Added/ Not added	Added/ Not added
	P0PLU(P0PLU0) /P9PLU(P9PLU0)		P0PLU(P0PLU2) /P9PLU(P9PLU2)	

■ Pins Setup (with 2 channels, at reception)

Table:11.3.11 shows the setup for synchronous serial interface pin with 2 channels (SBO0 pin, SBT0 pin) at reception. SBI0 pin can be used as a port.

Table:11.3.11 Setup for Synchronous Serial Interface Pin (with 2 channels, at reception)

Setup item	Data output pin	Serial unused pin	Clock I/O pin	
	SBO0A pin/ SBO0B pin	SBI0A pin/ SBI0B pin	SBT0A pin/SBT0B pin	
			Clock master	Clock slave
			SC0SCMD1(SC0MST)	
Port pin	P00/P90	P01/P91	P02/P92	
Port pin selection	Select used pin (A, B)			
	SCSEL(SC0SEL)			
SBI0/SBO0 selection	SBI0/SBO0 connection		-	
	SC0MD1(SC0IOM)			
Function	Port	Serial data input	Transfer clock input/ output	Transfer clock input/ output
	SC0MD1(SC0SBOS)	SC0MD1(SC0SBIS)	SC0MD1(SC0SBIS)	
Style	-	-	Push-pull/ Nch open-drain	Push-pull/ Nch open-drain
			P0ODC(P0ODC2)	
I/O	Input mode	-	Output mode	Input mode
	P0DIR(P0DIR0) P9DIR(P9DIR0)		P0DIR(P0DIR2)/P9DIR(P9DIR2)	
Pull-up setup	-	-	Added/ Not added	Added/ Not added
			P0PLU(P0PLU2)/P9PLU(P9PLU2)	

11.3.2 Setup Example

■ Transmission / Reception Setup Example

The setup example for clock synchronous serial communication with serial 0 is shown. Table:11.3.12 shows the conditions at transmission / reception.

Table:11.3.12 Setup Examples for Synchronous Serial Interface Transmission / Reception

Setup item	Set to
Serial data input pin	Independent(3 channels)
Transfer bit count	8 bit
Start condition	None
First transfer bit	MSB
Input edge	Falling edge
Output edge	Rising edge
Clock	Clock master
Clock source	fs/2
Clock source 1/8 dividing	Not divided by 8
Used pins	A (port0)
SBT0/SBO0 pin style	Nch open-drain
SBT0 pin pull-up resistor	Added
SBO0 pin pull-up resistor	Added
serial 0 communication complete interrupt	Enable
SBO0 output after last data output	"1"(H) fix

An example setup procedure, with a description of each step is shown below.

Setup Procedure	Description
(1) Select the prescaler operation SC0MD3(0x03F92) bp3 :SC0PSCE =1	(1) Set the SC0PSCE flag of the SC0MD3 register to "1" to select "prescaler operation".
(2) Select the clock source SC0MD3(0x03F92) bp2-0 :SC0PSC2-0 =100	(2) Set the SC0PSC2 to 0 flag of the SC0MD3 register to "100" to select the fs/2 to clock source.
(3) SBO0A output control after the last data output SC0MD3(0x03F92) bp7,6 :SC0FDC1-0 =00	(3) Set the SC0FDC1 to 0 flag of the SC0MD3 register to "00" to select "1" (High) fix of the SBO0 last data output.

Setup Procedure	Description
(4) Select the used pins SCSEL0(0x03F4F) bp0 :SC0SEL =0	(4) SC0SEL flag of SCSEL register to “0“ to set I/O used pin to A (port0).
(5) Pin style controlt P0ODC(0x03F1C) bp2,0 :P0ODC2,0 =1,1 P0PLU(0x03F40) bp2,0 :P0PLU2,0 =1,1	(5) Set the P0ODC2,0 flag of P0ODC register to “1,1” to select the Nch open-drain as SBO0A/SBT0A pin. Set P0PLU2,0 flag of P0PLU register to “1,1“ to select pull-up resistor.
(6) Control the pin direction P0DIR(0x03F49) bp2 :P0DIR2 =1 bp1 :P0DIR1 =0 bp0 :P0DIR0 =1	(6) Set the P0DIR2, P0DIR0 flag of the Port 0 pin direction control register (P0DIR) to "1,1" and the P0DIR3 flag to "0" to set P02, P00 to the output mode, P01 to the input mode.
(7) Set the SC0MD0 register Select the transfer bit count SC0MD0(0x03F8F) bp2-0 :SC0LNG2-0 =111 Select the start condition SC0MD0(0x03F8F) bp3 :SC0STE =0 Select the first bit to be transferred SC0MD0(0x03F8F) bp4 :SC0DIR =0 Select the transfer edge SC0MD0(0x03F8F) bp7 :SC0CE1 =1	(7) Set the SC0LNG2 to 0 flag of the serial 0 mode register 0 (SC0MD0) to "111" to set the transfer bit count "8 bits". Set the SC0STE flag of the SC0MD0 register to "0" to disable the start condition. Set the SC0DIR flag of the SC0MD0 register to "0" to set MSB as a transfer first bit. Set the SC0CE1 flag of the SC0MD0 register to "1" to set the reception data input edge "falling" and the transmission data output edge "rising".
(8) Set the SC0MD1 register Select the communication style SC0MD1(0x03F90) bp0 :SC0CMD =0 Select the transfer clock SC0MD1(0x03F90) bp2 :SC0MST =1 bp3 :SC0CKM =0 Select the transfer clock SC0MD1(0x03F90) bp4 :SC0SBOS =1 bp5 :SC0SBIS =1 bp6 :SC0SBTS =1 bp7 :SC0IOM =0	(8) Set the SC0CMD flag of the SC0MD1 register to "0" to select the synchronous serial. Set the SC0MST flag of the SC0MD1 register to "0" to select the clock master (internal clock). Set the SC0CKM flag to "0" to select "not divided by 8" for the clock source. Set the SC0SBOS, SC0SBIS, SC0SBTS flag of the SC0MD1 register to "1" to set the SBO0 pin to the serial data output, the SBI0 pin to the serial input, SBT0 pin to the transfer clock input/output. Set the SC0IOM flag "0" to set the serial data input from the SBI0 pin.
(9) Set the interrupt level SC0TICR(0x03FF3) bp7-6 :SC0LV1-0 =10	(9) Set the interrupt level by the SC0TLV1 to 0 flag of the serial 0 UART transmission interrupt control register (SC0TICR).

Setup Procedure	Description
(10) Enable the interrupt SC0TICR(0x03FF3) bp1 :SC0TIE =1	(10) Set the SC0TIE flag of the SC0TICR register to "1" to enable the interrupt. If any interrupt request flag (SC0TIR of the SC0TICR register) is already set, clear SC0TIR before the interrupt is enabled.
(11) Start the serial transmission Transmission data ý TXBUF0(0x03F95) Received data ý input SBI0 pin	(11) Set the transmission data to the serial transmission data buffer TXBUF0. The transmission or reception is started by the internal clock generation. When the transmission finished, the serial 0 UART transmission interrupt SC0TIRQ is generated. [Chapter 3. 3-1-4 Setup]

Note:Each procedure (1) to (3),(7),(8), and (9) can be set at the same time.

When only transmission with 3 channels is operated, set the SC0SBIS of the SC0MD1 register to "0" and set the serial input to "1" input. The SBI0 pin can be used as a general port. Also, when only reception is operated, set the SC0SBOS of the SC0MD1 register to "0" to select a port.

When communicate with 2 channels, the SBO0 pin inputs / outputs serial data. The port direction control register P0DIR switches I/O. At reception, set SC0SBIS of the SC0MD1 register to "1", always, to select "serial input". The SBI0 pin can be used as a general port.

This serial interface contains a emergency reset function. If the communication should be stopped by force, set SC0SBOS and SC0SBIS of the SC0MD1 register to "0".

Each flag should be set as this setup procedure in order. Activation of communication should be operated after all control registers (refer to Table:11.2.1 except TXBUF0) are set.

Transfer rate of transfer clock set by the SC0MD3 register should be under 5.0 MHz.

■ Transmission/Reception Setup Example (Standby Mode Reception)

The setup example for clock synchronous serial communication with serial 0 is shown. Table:11.3.13 shows the condition at standby mode reception.

Table:11.3.13 Setup Examples for Synchronous Serial Interface Transmission / Reception (Standby Mode Reception)

Setup item	Set to
Serial data input pin	Independent (2channels)
Transfer bit count	8 bit
Start condition	None
First transfer bit	MSB
Input edge	Falling edge
Clock	Clock slave
Operation mode	Stop mode
Clock source	fs/2
Clock source 1/8 dividing	Not divided by 8
Used pins	A (port0)
SBT0/SBO0 pin style	Push-pull
SBT0 pin pull-up resistor	Not added
SBO0 pin pull-up resistor	Not added
serial 0 communication complete interrupt	Enable

An example setup procedure, with a description of each step is shown below.

Setup Procedure	Description
(1) Select the prescaler operation SC0MD3(0x03F92) bp3 :SC0PSCE =1	(1) Set the SC0PSCE flag of the SC0MD3 register to "1" to select "prescaler operation".
(2) Select the clock source SC0MD3(0x03F92) bp2-0 :SC0PSC2-0 =100	(2) Set the SC0PSC2 to 0 flag of the SC0MD3 register to "100" to select fs/2 as the clock source.
(3) Select the used pins SCSEL0(0x03F4F) bp0 :SC0SEL =0	(3) SC0SEL flag of SCSEL register to “0“ to set I/O used pin to A (port0).

Setup Procedure	Description
(4) Pin style controlt P0ODC(0x03F1C) bp2,0 :P0ODC2,0 =1,1 P0PLU(0x03F40) bp2,0 :P0PLU2,0 =1,1	(4) Set the P0ODC2,0 flag of P0ODC register to “1,1” to select the Nch open-drain as SBO0A/SBT0A pin. Set P0PLU2,0 flag of P0PLU register to “1,1“ to select pull-up resistor.
(5) Control the pin direction P0DIR(0x03F49) bp2-0 :P0DIR2-0 =1,0,1	(5) Set the P0DIR2, P0DIR3 flag of the Port 0 pin direction control register (P0DIR) to "0,0" and the P0DIR0 flag to "1" to set P02, P01 to the input mode.
(6) ÏSelect the transfer bit count SC0MD0(0x03F8F) bp2-0 :SC0LNG2-0 =111	(6) Set the SC0LNG2 to 0 flag of the serial 0 mode register (SC0MD0) to "111" to set the transfer bit count "8 bits".
(7) Select the start condition SC0MD0(0x03F8F) bp3 :SC0STE =0	(7) Set the SC0LNG2 to 0 flag of the serial 0 mode register (SC0MD0) to "111" to disable the start condition.
(8) Select the first bit to be transferred SC0MD0(0x03F8F) bp4 :SC0DIR =0	(8) Set the SC0DIR flag of the SC0MD0 register to "0" to set MSB as a transfer first bit.
(9) Select the transfer edge SC0MD0(0x03F8F) bp7 :SC0CE1 =1	(9) Set the SC0CE1 flag of the SC0MD0 register to "1" to set the reception data input edge "falling".
(10) Select the communication type SC0MD1(0x03F90) bp0 :SC0CMD =0	(10) Set the SC0CMD flag of the SC0MD1 register to "0" to select the synchronous serial.
(11) Select the transfer clock SC0MD1(0x03F90) bp2 :SC0MST =0 bp3 :SC0CKM =0	(11) Set the SC0MST flag of the SC0MD1 register to "0" to select the clock slave (external slave). Set the SC0CKM flag to "0" to select "not divided by 8" for the clock source.
(12) Control the pin function SC0MD1(0x03F90) bp4 :SC0SBOS =0 bp5 :SC0SBIS =1 bp6 :SC0SBTS =1 bp7 :SC0IOM =0	(12) Set the SC0SBOS flag of the SC0MD1 register to "0", the SC0SBTS flag of the SC0SBIS register to "1" to set the SBI0 pin to the serial data input as the SBO0 pin general port, the SBT0 pin to the transfer clock input/ output. Set the SC0IOM flag "0" to set the serial data input from the SBI0 pin.
(13) Set the interrupt level SC0TICR(0x03FF3) bp7-6 :SC0LV1-0 =10	(13) Set the interrupt level by the SC0LV1 to 0 flag of the serial 0 UART transmission interrupt control register (SC0TICR). (Set level 2)
(14) Enable the interrupt SC0TICR(0x03FF3) bp1 :SC0TIE =1	(14) Set the SC0TIE flag of the SC0TICR register to "1" to enable the interrupt. If any interrupt request flag (SC0TIR of the SC0TICR register) is already set, clear SC0TIR before the interrupt is enabled. [Chapter 3. 3-1-4 Setup]

Setup Procedure	Description
(15) Set the startup factor of the serial communication Dummy data ý TXBUF0(0x03F95)	(15) Set the dummy data to the serial transmission data buffer TXBUF0.
(16) Transfer to STOP mode CPUM(0x03F00) bp3:STOP =1	(16) Set the STOP flag of the CPUM register to "1" to transfer to the stop mode.
(17) Start the serial communication Transmission clock ý input SBT0 pin Received data ý input SBI0 pin	(17) Input the transfer clock to the SBT0 pin and transfer data to the SBI0 pin.
(18) Recover from the standby mode	(18) The serial 0 UART transmission interrupt SC0TIRQ is generated at the same time of the 8th bits data reception, then, CPU is recovered from the stop mode to the normal mode after the oscillation stabilization wait.

Note:Each procedure (1) to (2), (6) to (9), and (10) to (12) can be set at the same time.

The slave reception at the standby mode should be used without the start condition to receive properly.

Each flag should be set as this setup procedure in order. Activation of communication should be operated after all control registers (refer to Table:11.2.1 except TXBUF0,RXBUF0) are set.

11.3.3 UART Serial Interface

serial 0 can be used for full duplex UART communication. Table:11.3.14 shows UART serial interface functions.

Table:11.3.14 URAT Serial Interface Functions

Communication style	UART (full duplex)
Interrupt	SC0TIRQ (transmission), SC0RIRQ (reception)
Used pins	TXD0 (output / input) RXD0 (input)
Specification the first transfer bit	MSB / LSB
Selection of parity bit	O
Parity bit control	0 parity 1 parity odd parity even parity
Frame selection	7 bits + 1 STOP 7 bits + 2 STOP 8 bits + 1 STOP 8 bits + 2 STOP
Continuous operation	O
Maximum transfer rate	300 kbps (standard 300 bps to 38.4 kbps) (with baud rate timer)

■ Activation Factor for Communication

At transmission, if any data is set to the transmission data buffer TXBUF0, a start condition is generated to start transfer. At reception, if a start condition is received, communication is started. At reception, if the data length of "L" for start bit is longer than 0.5 bit, that can be regarded as a start condition.

■ Transmission

Data transfer is automatically started by setting data to the transmission data buffer TXBUF0. When the transmission is completed, the serial 0 transmission interrupt SC0TIRQ is generated.

■ Reception

Once a start condition is received, reception is started after the transfer bit counter that counts transfer bit is cleared. When the reception is completed, the serial 0 reception interrupt SC0RIRQ is generated.

■ Full duplex communication

On full duplex communication, the transmission and reception can be operated separately at the same time. The frame mode and parity bit of the used data on transmission / reception should have the same polarity.

■ Transfer Bit Count Setup

The transfer bit count is automatically set after the frame mode is specified by the SC0FM1 to 0 flag of the SC0MD2 register. If the SC0CMD flag of the SC0MD1 register is set to "1", and UART communication is selected, the setup by the synchronous serial transfer bit count selection flag SC0LNG2 to 0 is no more valid.

■ Switch the used pins

Switch the used pins to A(TXD0A, RXD0A) or B(TXD0B, RXD0B) by SC0SEL flag of SCSEL register.

■ Data Input Pin Setup

The communication mode can be selected from with 2 channels (data output pin (TXD0 pin), data input pin (RXD0 pin)), or with 1 channel (data I/O pin TXD0 pin). The RXD0 pin can be used only for serial data input. The TXD0 pin can be used for serial data input or output. The SC0IOM flag of the SC0MD1 register can specify which pin, RXD0 or TXD0 inputs the serial data. If "data input from TXD0 pin" is selected to be with 1 line communication, transmission / reception is switched by controlling TXD0 pin's direction by the P0DIR0 flag of the P0DIR register. At the same time, the RXD0 pin can be used as a general port.

■ Reception Buffer Empty Flag

When SC0RIRQ is generated, data is stored to RXBUF0 from the internal shift register, automatically. If data is stored to RXBUF0 from the shift register, the reception buffer empty flag SC0REMP of the SC0STR register is set to "1". That indicates that the received data is going to be read out. SC0REMP is cleared to "0" by reading out the data of RXBUF0.

■ Reception BUSY Flag

When the start condition is regarded, the SC0RBSY flag of the SC0STR register is set to "1". That is cleared to "0" by the generation of the reception complete interrupt SC0TIRQ. If the SC0SBIS flag is set to "0" during reception, the SC0RBSY flag is reset to "0".

■ Transmission BUSY Flag

When any data is set to TXBUF0, the SC0TBSY flag of the SC0STR register is set to "1". That is cleared to "0" by the generation of the transmission complete interrupt SC0TIRQ. During continuous communication the SC0TBSY flag is always set. If the transmission buffer empty flag SC0TEMP is set to "0" as the transmission complete interrupt SC0TIRQ is generated, the SC0TBSY is cleared to "0". If the SC0SBOS flag is set to "0", the SC0TBSY flag is reset to "0".

■ Frame Mode and Parity Check Setup

Figure 11-3-17 shows the data format at UART communication.

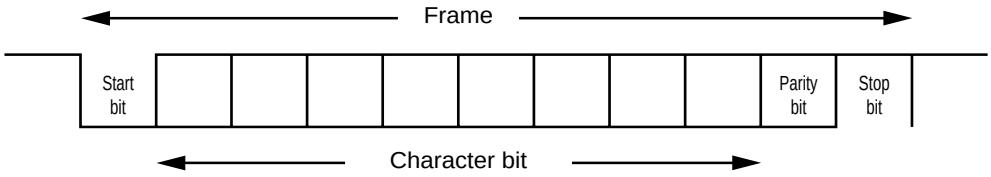


Figure:11.3.17 UART Serial Interface Transmission / Reception Data Format

The transmission / reception data consists of start bit, character bit, parity bit and stop bit. Table:11.3.15 shows its kinds to be set.

Table:11.3.15 UART Serial Interface Transmission / Reception Data

Start bit	1 bit
Character bit	7,8 bit
Parity bit	fixed to 0, fixed to 1, odd, even, none
Stop bit	1,2 bits

The SC0FM1 to 0 flag of the SC0MD2 register sets the frame mode. Table:11.3.16 shows the UART serial interface frame mode settings. If the SC0CMD flag of the SC0MD1 register is set to "1", and UART communication is selected, the transfer bit count on the SC0LNG2 to 0 flag of the SC0MD0 register is no more valid.

Table:11.3.16 UART Serial Interface Frame Mode

SC0MD2 register		Frame mode
SC0FM1	SC0FM0	
0	0	Character bit 7 bits + Stop bit 1 bit
0	1	Character bit 7 bits + Stop bit 2 bits
1	0	Character bit 8 bits + Stop bit 1 bit
1	1	Character bit 8 bits + Stop bit 2 bits

Parity bit is to detect wrong bits with transmission / reception data. Table:11.3.17 shows kinds of parity bit. The SC0NPE, SC0PM1 to 0 flag of the SC0MD2 register set parity bit.

Table:11.3.17 Parity Bit of UART Serial Interface

SC0MD2			Parity bit	Setup
SC0NPE	SC0PM1	SC0PM0		
0	0	0	Fixed to 0	Set parity bit to "0"
0	0	1	Fixed to 1	Set parity bit to "1"
0	1	0	Odd parity	Control that the total of "1" of parity bit and character bit should be odd
0	1	1	Even parity	Control that the total of "1" of parity bit and character bit should be even
1	-	-	None	Do not add parity bit

■ Break Status Transmission Control Setup

The SC0BRKE flag of the SC0MD2 register generates the brake status. If SC0BRKE is set to "1" to select the brake transmission, all bits from start bits to stop bits transfer "0".

■ Reception Error

At reception, there are 3 types of error; overrun error, parity error and framing error. Reception error can be determined by the SC0ORE, SC0PEK, SC0FEF flag of the SC0STR register. Even one of those errors is detected, the SC0ERE flag of the SC0STR register is set to "1". SC0PEK, the SC0FEF flags in reception error flag are renewed at generation of the reception complete interrupt SC0RIRQ. The SC0ORE flag is cleared at the same time of next communication complete interrupt SC0RIRQ generation after the data of the RXBUF0 is read out. The decision of the received error flag should be operated until the next communication is finished. Those error flag has no effect on communication operation. Table:11.3.18 shows the list of reception error source.

Table:11.3.18 Reception Error Source of UART Serial Interface

Flag	Error		
SC0ORE	Overrun error	Next data is received before reading the receive buffer	
SC0PEK	Parity error	at fixed to 0	when parity bit is "1"
		at fixed to 1	When parity bit is "0"
		Odd parity	The total of "1" of parity bit and character bit is even
		Even parity	The total of "1" of parity bit and character bit is odd
SC0FEF	Framing error	Stop bit is not detected	

■ Judgement of Break Status Reception

Reception at break status can be judge. If all received data from start bit and stop bit is "0", the SC0BRKF flag of the SC0MD2 register is set and regards the break status. The SC0BRKF flag is set at generation of the reception complete interrupt SC0RIRQ.

■ Continuous Communication

This serial interface has continuous communication function. If data is set to the transmission data buffer TXBUF0 during communication, the transmission buffer empty flag SC0TEMP is set to continue automatic communication. This does not generate any blank in communication. Set data to TXBUF between previous data setup and generation of the communication complete interrupt SC0TIRQ.

■ Clock Setup

Transfer clock is not necessary for UART communication itself, but necessary for setup of data transmission / reception timing in the serial interface.

Select the timer to be used as a baud rate timer by the SC0MD3 register.

■ Receive Bit Count and First Transfer Bit

In the case of reception, when the transfer bit count is 7 bits, the data storing method to the received data buffer RXBUF0 is different depending on the first transfer bit selection. At MSB first, data are stored to the upper bits of RXBUF0. When there are 7 bits to be transferred, as shown on Table:11.3.18, if data "G" to "A" are stored to bp7 to bp1 of RXBUF0. At LSB first, data are stored to the lower bits of RXBUF0. When there are 7 bits to be transferred, as shown on Table:11.3.19, if data "A" to "G" are stored to bp0 to bp6 of RXBUF0.

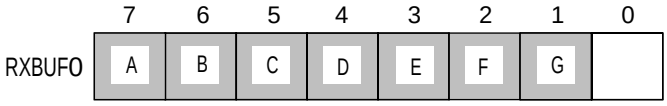


Figure:11.3.18 Transfer Bit Count and First Transfer Bit (starting with MSB)

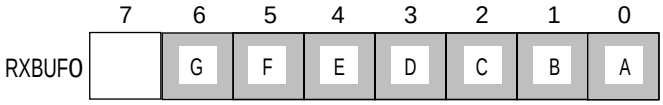


Figure:11.3.19 Transfer Bit Count and First Transfer Bit (starting with LSB)

The following items are the same as clock synchronous serial.

- First Transfer Bit Setup

Refer to:XI-14

- Transmission Data Buffer

Refer to:XI-14

- Received Data Buffer

Refer to:XI14

- Transfer Bit Count and First Transfer Bit

Refer to:XI-16

- Transmission Buffer Empty Flag

Refer to:XI-19

- Emergency Reset

Refer to:XI-20

■ Transmission Timing

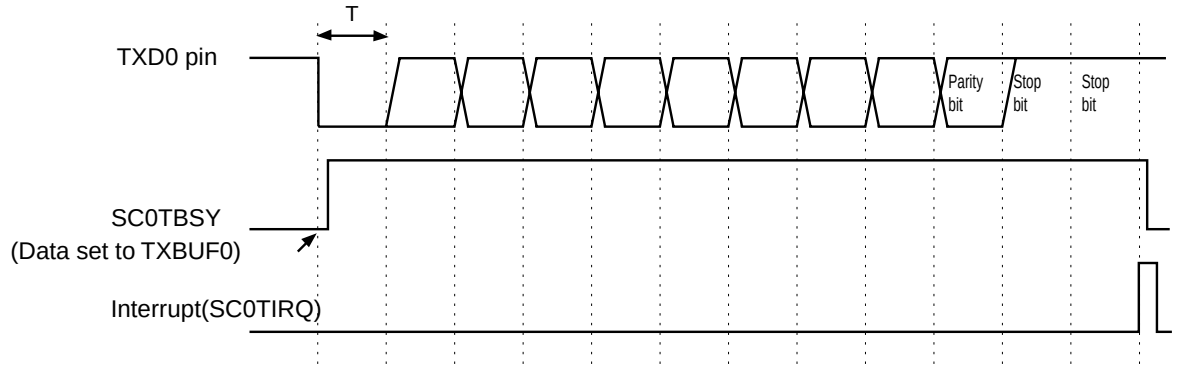


Figure:11.3.20 Transmission Timing (parity bit is enabled)

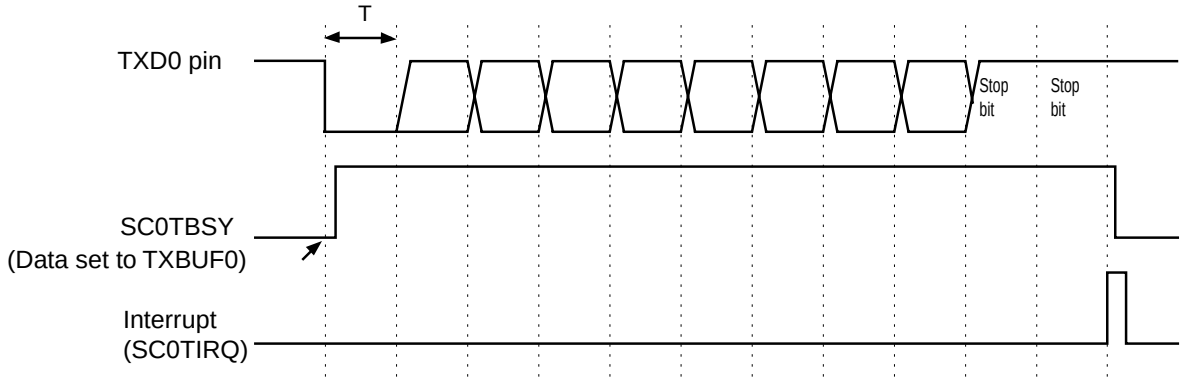


Figure:11.3.21 Transmission Timing (parity bit is disabled)

■ Reception Timing

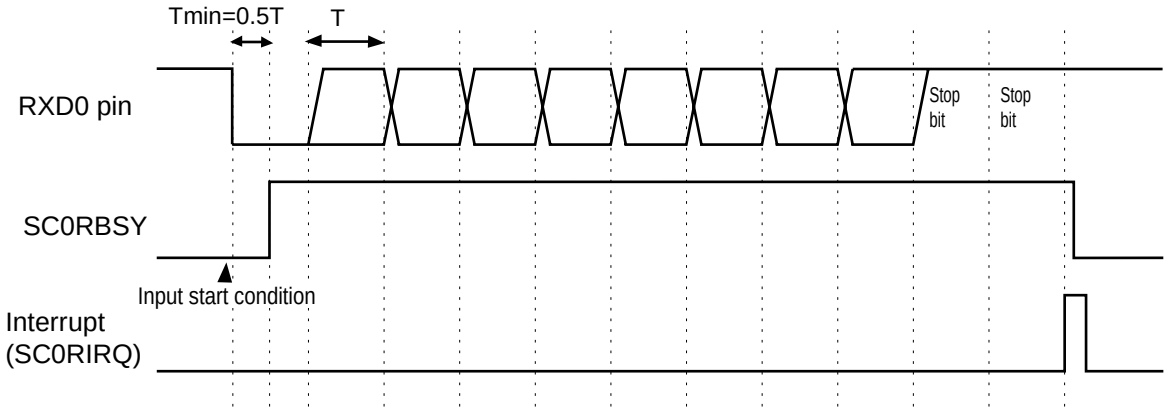


Figure:11.3.22 Reception Timing (parity bit is enabled)

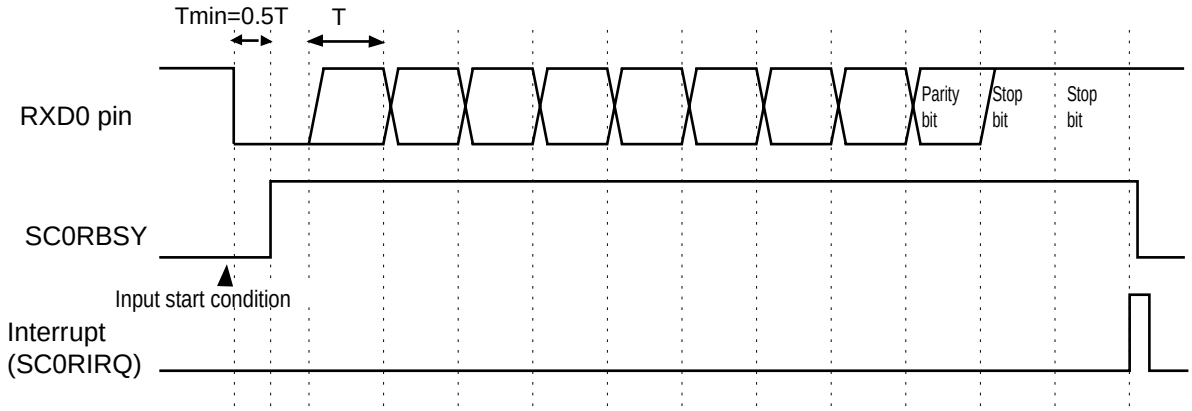


Figure:11.3.23 Reception Timing (parity bit is disabled)

■ Transfer Speed Setup

Baud rate timer (timer 2, timer 4) can set any transfer rate. Table:11.3.19 shows the setup example of the transfer speed.

Table:11.3.19 UART Serial Interface Transfer Speed

Setup	Register	Page
Serial 0 clock source (timer 2 , timer 4)	SC0MD3	XI-10
Timer 2 clock source	TM2MD	V-19
Timer 2 compare register	TM1OC	V-14
Timer 4 clock source	TM4MD	V-21
Timer 4 compare register	TM4OC	V-15

Timer compare register is set as follows;

baud rate = 1 / (overflow cycle × 2 × 8) ("8" means that clock source is divided by 8)

overflow cycle = (set value of compare register + 1)×timer clock cycle

therefore,

set value of compare register = timer clock frequency / (baud rate × 2 × 8) - 1

For example, if baud rate should be 300 bps at timer clock source fs/4 (fosc = 8 MHz, fs = fosc/2), set value should be as follows;

Set value of compare register = $(8\times10^6 / 2 / 4) / (300 \times 2 \times 8) - 1$

= 207

= 0xCF

Timer clock source and the set value of timer compare register at the standard rate are shown in the following page.

Transfer rate should be selected under 300 kbps.

fosc (MHz)	Clock source (Timer)	Transfer Speed (bit/s)									
		300		960		1200		2400		4800	
		Set Value	caluculated value	Set Value	caluculated value	Set Value	caluculated value	Set Value	caluculated value	Set Value	caluculated value
4.00	fosc	-	-	-	-	207	1202	103	2404	51	4808
	fosc/4	207	300	64	962	51	1202	25	2404	12	4808
	fosc/16	51	300	-	-	12	1202	-	-	-	-
	fosc/32	25	300	-	-	-	-	-	-	-	-
	fosc/64	12	300	-	-	-	-	-	-	-	-
	fs/2	207	300	64	962	51	1202	25	2404	12	4808
	fs/4	104	297	-	-	25	1202	12	2404	-	-
4.19	fosc	-	-	-	-	217	1201	108	2403	54	4761
	fosc/4	217	300	67	963	-	-	-	-	-	-
	fosc/16	-	-	16	963	-	-	6	2338	-	-
	fosc/32	-	-	-	-	-	-	-	-	-	-
	fosc/64	-	-	-	-	-	-	-	-	-	-
	fs/2	217	300	67	963	-	-	-	-	-	-
	fs/4	108	300	33	963	-	-	13	2338	-	-
8.00	fosc	-	-	-	-	-	-	207	2404	103	4808
	fosc/4	-	-	129	962	103	1202	51	2404	25	4808
	fosc/16	103	300	-	-	25	1202	12	2404	-	-
	fosc/32	51	300	-	-	12	1202	-	-	-	-
	fosc/64	25	300	-	-	-	-	-	-	-	-
	fs/2	-	-	129	962	103	1202	51	2404	25	4808
	fs/4	207	300	64	962	51	1202	25	2404	12	4808
8.38	fosc	-	-	-	-	-	-	217	2403	108	4805
	fosc/4	-	-	135	963	108	1201	-	-	-	-
	fosc/16	108	300	33	963	-	-	13	2338	-	-
	fosc/32	-	-	16	963	-	-	6	2338	-	-
	fosc/64	-	-	-	-	-	-	-	-	-	-
	fs/2	-	-	135	963	108	1201	-	-	-	-
	fs/4	217	300	67	963	-	-	-	-	-	-
12.00	fosc	-	-	-	-	-	-	-	-	155	4808
	fosc/4	-	-	194	962	155	1202	77	2404	38	4808
	fosc/16	155	300	-	-	38	1202	-	-	-	-
	fosc/32	77	300	-	-	-	-	-	-	-	-
	fosc/64	38	300	-	-	-	-	-	-	-	-
	fs/2	-	-	194	962	155	1202	77	2404	38	4808
	fs/4	-	-	-	-	77	1202	38	2404	-	-
16.00	fosc	-	-	-	-	-	-	-	-	207	4808
	fosc/4	-	-	-	-	207	1202	103	2404	51	4808
	fosc/16	207	300	64	962	51	1202	25	2404	12	4808
	fosc/32	103	300	-	-	25	1202	12	2404	-	-
	fosc/64	51	300	-	-	12	1202	-	-	-	-
	fs/2	-	-	-	-	207	1202	103	2404	51	4808
	fs/4	-	-	129	962	103	1202	51	2404	25	4808

Figure:11.3.24 Setup Value of UART Serial Interface Transfer Speed

		Transfer Speed (bit/s)									
fosc (MHz)	Clock source (Timer)	9600		19200		28800		31250		38400	
		Set Value	caluculated value	Set Value	caluculated value	Set Value	caluculated value	Set Value	caluculated value	Set Value	caluculated value
4.00	fosc	25	9615	12	19231	-	-	7	31250	-	-
	fosc/4	-	-	-	-	-	-	1	31250	-	-
	fosc/16	-	-	-	-	-	-	-	-	-	-
	fosc/32	-	-	-	-	-	-	-	-	-	-
	fosc/64	-	-	-	-	-	-	-	-	-	-
	fs/2	-	-	-	-	-	-	1	31250	-	-
	fs/4	-	-	-	-	-	-	-	-	-	-
4.19	fosc	26	9699	-	-	-	-	-	-	-	-
	fosc/4	-	-	-	-	-	-	-	-	-	-
	fosc/16	-	-	-	-	-	-	-	-	-	-
	fosc/32	-	-	-	-	-	-	-	-	-	-
	fosc/64	-	-	-	-	-	-	-	-	-	-
	fs/2	-	-	-	-	-	-	-	-	-	-
	fs/4	-	-	-	-	-	-	-	-	-	-
8.00	fosc	51	9615	25	19231	-	-	15	31250	12	38462
	fosc/4	12	9615	-	-	-	-	3	31250	-	-
	fosc/16	-	-	-	-	-	-	-	-	-	-
	fosc/32	-	-	-	-	-	-	-	-	-	-
	fosc/64	-	-	-	-	-	-	-	-	-	-
	fs/2	12	9615	-	-	-	-	3	31250	-	-
	fs/4	-	-	-	-	-	-	1	31250	-	-
8.38	fosc	54	9523	26	19398	-	-	-	-	-	-
	fosc/4	-	-	-	-	-	-	-	-	-	-
	fosc/16	-	-	-	-	-	-	-	-	-	-
	fosc/32	-	-	-	-	-	-	-	-	-	-
	fosc/64	-	-	-	-	-	-	-	-	-	-
	fs/2	-	-	-	-	-	-	-	-	-	-
	fs/4	-	-	-	-	-	-	-	-	-	-
12.00	fosc	77	9615	38	19231	25	28846	23	31250	-	-
	fosc/4	-	-	-	-	-	-	5	31250	-	-
	fosc/16	-	-	-	-	-	-	-	-	-	-
	fosc/32	-	-	-	-	-	-	-	-	-	-
	fosc/64	-	-	-	-	-	-	-	-	-	-
	fs/2	-	-	-	-	-	-	5	31250	-	-
	fs/4	-	-	-	-	-	-	2	31250	-	-
16.00	fosc	103	9615	51	19231	-	-	31	31250	25	38462
	fosc/4	25	9615	12	19231	-	-	7	31250	-	-
	fosc/16	-	-	-	-	-	-	-	-	-	-
	fosc/32	-	-	-	-	-	-	-	-	-	-
	fosc/64	-	-	-	-	-	-	-	-	-	-
	fs/2	25	9615	-	-	-	-	7	31250	-	-
	fs/4	12	9615	-	-	-	-	3	31250	-	-

Figure:11.3.25 Setup Value of UART Serial Interface Transfer Speed

■ Pin Setup (with 1,2 channels, at transmission)

Table:11.3.20 shows the pins setup at UART serial interface transmission. The pins setup is common to the TXD0 pin, RXD0 pin, regardless of those pins are independent / connected.

Table:11.3.20 UART Serial Interface Pin Setup (with 1,2 channels, at transmission)

Setup item	Data output pin	Data input pin
	TXD0A pin / TXD0B pin	RXD0A pin / RXD0B pin
Port pin	P00/P90	P01/P91
Port pin selection	Select the used pin(A,B)	
	SCSEL(SC0SEL)	
TXD0/RXD0 pin selection	TXD0/RXD0 pin independent/connect	
	SC0MD1(SC0IOM)	
Function	Serial data output	"1" input
	SC0MD1(SC0SBOS)	SC0MD1(SC0SBIS)
Style	Push-pull/ Nch open-drain	-
	P0ODC(P0ODC0) / P9ODC(P9ODC0)	
I/O	Output mode	-
	P0DIR(P0DIR0) / P9DIR(P9DIR0)	
Pull-up setup	Added / not added	-
	P0PLU(P0PLU0) / P9PLU(P9PLU0)	

■ Pin Setup (with 2 channels, at reception)

Table:11.3.21 shows the pins setup at UART serial interface reception with 2 channels (TXD0 pin, RXD0pin).

Table:11.3.21 UART Serial Interface Pin Setup (with 2 channels, at reception)

Setup item	Data output pin	Data input pin
	TXD0A pin / TXD0B pin	RXD0A pin / RXD0B pin
Port pin	P00 / P90	P01 / P91
Port pin selection	Select the used pin(A,B)	
	SCSEL(SC0SEL)	
Serial data input selection	TXD0/RXD0 pin independent	
	SC0MD1(SC0IOM)	
Function	Port	Serial data input
	SC0MD1(SC0SBOS)	SC0MD1(SC0SBIS)
Style	-	-
I/O	-	Input mode
	-	P0DIR(P0DIR1)/P9DIR(P9DIR1)
Pull-up setup	-	-

■ Pin Setup (with 1 channel, at reception)

Table:11.3.22 shows the pin setup at UART serial interface reception with 1 channel (TXD0 pin). The RXD0 pin in not used, so can be used as a port.

Table:11.3.22 UART Serial Interface Pin Setup (with 1 channel, at reception)

Setup item	Data output pin	Data input pin
	TXD0A pin / TXD0Bpin	RXD0A pin / RXD0B pin
Port pin	P00 / P90	P01 / P91
Port pin selection	Select the used pin(A,B)	
	SCSEL(SC0SEL)	
Serial data input selection	TXD0 / RXD0 pin connect	
	SC0MD1(SC0IOM)	
Function	Port	Serial data input
	SC0MD1(SC0SBOS)	SC0MD1(SC0SBIS)
Style	-	-
I/O	-	Input mode
	-	P0DIR(P0DIR1)/P9DIR(P9DIR1)
Pull-up setup	-	-

■ Pin Setup (with 2 channels, at transmission / reception)

Table:11.3.23 shows the pin setup at UART serial interface transmission / reception with 2 channels (TXD0 pin, RXD0 pin).

Table:11.3.23 UART Serial Interface Pin Setup (with 2 channels, at transmission / reception)

Setup item	Data output pin	Data input pin
	TXD0A pin / TXD0B pin	RXD0A pin / RXD0B pin
Port pin	P00 / P90	P01 / P91
Port pin selection	Select the used pin(A,B)	
	SCSEL(SC0SEL)	
Serial data input selection	TXD0 / RXD0 pin independent	
	SC0MD1(SC0IOM)	
Function	Serial data output	Serial data input
	SC0MD1(SC0SBOS)	SC0MD1(SC0SBIS)
Style	Push-pull / Nch open-drain	-
	P0ODC(P0ODC0)	
I/O	Output mode	Input mode
	P0DIR(P0DIR0) / P9DIR(P9DIR0)	P0DIR(P0DIR1) / P9DIR(P9DIR1)
Pull-up setup	Added / not added	-
	P0PLU(P0PLU0) / P9PLU(P9PLU0)	

11.3.4 Setup Example

■ Transmission / Reception Setup

The setup example at UART transmission / reception with serial 0 is shown. Table:11.3.24 shows the condition at transmission / reception.

Table:11.3.24 UART Interface Transmission Reception Setup

Setup item	SEt to
TXD0/RXD0 pin	Independent (with 2 channels)
Frame mode specification	8 bits + 2 stop bits
First transfer bit	MSB
Clock source	Timer 4
Used pins	A (port0)
TXD0/RXD0 pin type	Nch open-drain
Pull-up resistor of TXD0 pin	Added
Parity bit add/check	"0" added/check
Serial 0 transmission complete interrupt	Enable
Serial 0 reception complete interrupt	Enable

An example setup procedure, with a description of each step is shown below.

Setup Procedure	Description
(1) Set the baud rate timer	(1) Set the baud rate timer by the TM4MD register, the TM4OC register. Set the TM4EN flag to "1" to start timer 4. [Chapter 5. 5.9 Serial Transfer Clock Output Operation]
(2) Select the clock source SC0MD3(0x03F92) bp2-0 :SC0PSC2-0 =111	(2) Set the bp3 to 0 flag of the SC0MD3 register to "111" to select Timer 4 output as a clock source.
(3) Select the used pins SCSEL(0x03F4F) bp0 :SC0SEL=0	(3) Set the SC0SEL flag of SCSEL register to “0” to select the I/O pin to A(port0).
(4) Control the pin type P0ODC(0x03F1C) bp0 :P0ODC0 =1 P0PLU(0x03F40) bp0 :P0PLU0 =1	(4) Set the P0ODC0 flag of the P0ODC register to "1" to select Nch open-drain for the TXD0 pin. P0PLU0 flag of the P0PLU register to "1" to add pull-up register.

Setup Procedure	Description
(5) Control the pin direction P0DIR(0x03F30) bp1-0 :P0DIR1-0 =01	(5) Set the P0DIR1to 0 flag of the Port 0 pin direction control register (P0DIR) to "1" to set P00 to the output mode, P01 to the input mode.
(6) Set the SC0MD0 register Select the start condition SC0MD0(0x03F8F) bp3 :SC0STE =1	(6) Set the SC0STE flag of the SC0MD0 register to "1" to enable start condition.
Select the first bit to be transferred SCO0MD0(0x03F8F) bp4 :SC0DIR =0	Set the SC0DIR flag of the SC0MD0 register to "0" to select MSB as the first transfer bit.
(7) Set the SC0MD2 register Control the output data SC0MD2(0x03F91) bp0 :SC0BRKE =0	(7) Set the SC0BRKE flag of the SC0MD2 register to "0" to select the serial data transmission.
Select the added parity bit SC0MD2(0x03F91) bp3 :SC0NPE =0 bp5-4 :SC0PM1-0 =00	Set the SC0PM1 to 0 flag of the SC0MD2 register to "00" to select 0 parity, and set the SC0NPE flag to "0" to enable add parity bit.
Specify the flame mode SC0MD2(0x03F91) bp7-6 :SC0FM1-0 =11	Set the SC0FM1 to 0 flag of the SC0MD2 register to "11" to select 8 bits + 2 stop bits at the flame mode.
(8) Set the SC0MD1 register Select the communication type SC0MD1(0x03F90) bp0 :SC0CMD =1	(8) Set the SC0CMD flag of the SC0MD1 register to "1" to select full duplex UART.
Select the clock frequency SC0MD1(0x03F90) bp3 :SC0CKM =1 bp2 :SC0MST =1	Set the SC0CKM flag of the SC0MD1 register to "1" to select "divided by 8" at source clock. And, the SC0MST flag should be always set to "1" to select clock master.
Control the pin function SC0MD1(0x03F90) bp4 :SC0SBOS =1 bp5 :SC0SBIS =1 bp7 :SC0IOM =0	Set the SC0SBOS, SC0SBIS flag of the SC0MD1 register to "1" to set the TXD0A pin to serial data output and the RXD0A pin to serial data input.
(9) Select the interrupt level SC0RICR(0x03FF2) bp1 :SC0RIE =1 SC0TICR(0x03FF3) bp1 :SC0TIE =1	(9) Set the SC0RIE flag of the SC0RICR register to "1", and SC0TIE flag of the SC0TICR register to "1" to enable the interrupt request. If any the interrupt request already set, clear them.

Setup Procedure	Description
(10) Start the serial transmission The transmission →TXBUF0(0x03F95) The reception data → input to RXD0	(10) The transmission is started by setting the transmission data to the serial transmission data buffer (TXBUF0). When the transmission is finished, the serial 0 transmission interrupt (SC0TIRQ) is generated. Also, after the received data is stored to the RXBUF0, the serial 0 reception interrupt (SC0RIRQ) is generated.

Note:(6), (7), (8) can be set at the same time.

When the TXD0 / RXD0 pin are connected for communication with 1 channel, the TXD0 pin inputs / outputs serial data. The port direction control register P0DIR switches I/O. At reception, set SC0SBIOS of the SC0MD1 register to "1" to select serial data input. The RXD0 pin can be used as a general port.

This serial interface contains emergency reset function. If communication need to be stopped by force, set SC0SBOS and SC0SBIS of the SC0MD1 register to "0".

Each flag should be set as the setup procedure in order. Activation of communication should be operated after all control registers (refer to Table:11.2.1 TXBUF0, RXBUF0) are set.

Timer 2 and timer 4 can be used as a baud rate timer. Refer to Chapter 5. 5.9 Serial Transfer Clock Output Operation.

Chapter 12 Serial interface 1

12.1 Overview

This LSI contains a serial interface 1 that can be used for both communication types of clock synchronous and UART (full duplex).

12.1.1 Functions

Table:12.1.1 shows functions of serial interface 1.

Table:12.1.1 Serial Interface 1 functions

Communication style	Clock synchronous	UART (full duplex)
Interrupt	SC1TIRQ	SC1TIRQ(on transmission completion) SC1RIRQ(on reception completion)
Used pins	SBO1,SBI1,SBT1	TXD1,RXD1
3 channels type	O	-
2 channels type	O(SBO1,SBT1)	O
1 channel type	-	TXD1
Specification of transfer bit count/ Frame selection	1 to 8 bits	7 bit +1STOP 7 bit +2STOP 8 bit +1STOP 8 bit +2STOP
Selection of parity bit	-	O
Parity bit control	-	0 parity 1 parity odd parity even parity
Selection of start condition	O	Only "enable start condition" is available
Specify of the first transfer bit	O	O
Specify of input edge/ output edge	O	-
SBO1 output control after final data moved out	H/L/final data hold	-
At the standby mode	Only slave reception is available	-
Continuous operation	O	O
Internal clock 1/8 dividing	O	Only 1/8 dividing is available

Clock source	fosc/2 fosc/4 fosc/16 fosc/64 fs/2 fs/4 External clock Timer 4 output Timer 5 output	fosc/2 fosc/4 fosc/16 fosc/64 fs/2 fs/4 Timer 4 output Timer 5 output
Maximum transfer rate	5.0 MHz	300 kbps
fosc:Machine clock (High speed oscillation) fs:System clock		

Set the transfer rate slower than system clock (fs).

12.1.2 Block Diagram

■ Serial interface 1 Block Diagram

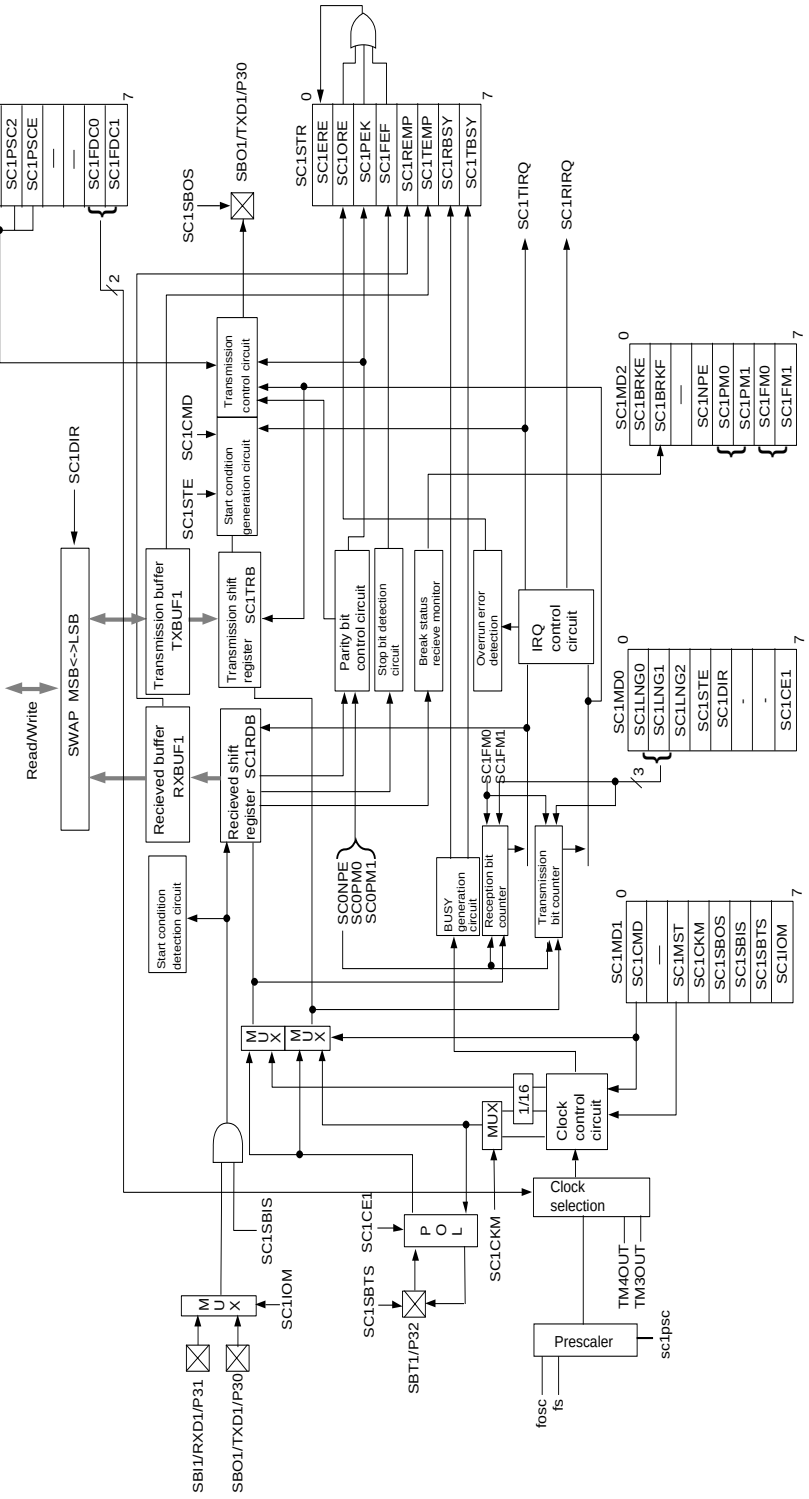


Figure:12.1.1 Serial interface 1 Block Diagram

12.2 Control Registers

12.2.1 Registers

Table:12.2.1 shows registers to control serial interface 1.

Table:12.2.1 Serial interface 1 Control Registers

Register	Address	R/W	Function	Page
SC1MD0	0x03F9D	R/W	Serial interface 1 mode register 0	XII-7
SC1MD1	0x03F9E	R/W	Serial interface 1 mode register 1	XII-8
SC1MD2	0x03F9F	R/W	Serial interface 1 mode register 2	XII-9
SC1MD3	0x03FA0	R/W	Serial interface 1 mode register 3	XII-10
SC1STR	0x03FA1	R	Serial interface 1 status register	XII-11
RXBUF1	0x03FA2	R	Serial interface 1 received data buffer	XII-6
TXBUF1	0x03FA3	R/W	Serial interface 1 transmission data buffer	XII-6
P3ODC	0x03F2C	R/W	Port 3 Nch open drain control register	IV-37
P3DIR	0x03F43	R/W	Port 3 pull-up control register	IV-37
P3PLU	0x03F33	R/W	Port 3 direction control register	IV-36
SC1RICR	0x03FF4	R/W	Serial 1 UART reception interrupt control register	III-38
SC1TICR	0x03FF5	R/W	Serial 1 UART transmission interrupt control register	III-39

R/W:Readable/ Writable

R:Readable only

12.2.2 Data Buffer Registers

Serial interface 1 has each 8-bit data buffer register for transmission, and for reception.

■ Serial interface 1 Received Data Buffer (RXBUF1:0x03FA2)

bp	7	6	5	4	3	2	1	0
Flag	RXBUF17	RXBUF16	RXBUF15	RXBUF14	RXBUF13	RXBUF12	RXBUF11	RXBUF10
Reset	X	X	X	X	X	X	X	X
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

■ Serial interface 1 Transmission Data Buffer (TXBUF1:0x03FA3)

bp	7	6	5	4	3	2	1	0
Flag	TXBUF17	TXBUF16	TXBUF15	TXBUF14	TXBUF13	TXBUF12	TXBUF11	TXBUF10
Reset	X	X	X	X	X	X	X	X
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

12.2.3 Mode Registers

■ Serial interface 1 Mode Register 0 (SC1MD0:0x03F9D)

bp	7	6	5	4	3	2	1	0
Flag	SC1CE1	-	-	SC1DIR	SC1STE	SC1LNG2	SC1LNG1	SC1LNG0
Reset	0	-	-	0	0	1	1	1
Access	R/W	-	-	R/W	R/W	R/W	R/W	R/W

bp	Flag	Description
7	SC1CE1	Transmission data output edge 0:falling 1:rising Reception data input edge 0:rising 1:falling
6-5	-	-
4	SC1DIR	First bit to be transferred 0:MSB first 1:LSB first
3	SC1STE	Start condition selection 0:Disable start condition 1:Enable start condition
2-0	SC1LNG2 SC1LNG1 SC1LNG0	Transfer bit 000:1bit 001:2bit 010:3bit 011:4bit 100:5bit 101:6bit 110:7bit 111:8bit

■ Serial interface 1 Mode Register 1(SC1MD1:0x03F9E)

bp	7	6	5	4	3	2	1	0
Flag	SC1IOM	SC1SBTS	SC1SBIS	SC1SBOS	SC1CKM	SC1MST	-	SC1CMD
Reset	0	0	0	0	0	0	-	0
Access	R/W	R/W	R/W	R/W	-	R/W	-	R/W

bp	Flag	Description
7	SC1IOM	Serial data input selection 0:Data input from SBI1 (RXD1) 1:Data input from SBO1 (TXD1)
6	SC1SBTS	SBT1 pin function selection 0:Port 1:Transfer clock I/O
5	SC1SBIS	Serial input control selection 0:Input "1" 1:Input serial
4	SC1SBOS	SBO1(TXD1) pin function 0:Port 1:Output serial data
3	SC1CKM	1/8 dividing of transfer clock selection 0:Not divided by 8 1:Divided 1/8
2	SC1MST	Clock master/ slave selection 0:Clock slave 1:Clock master
1	-	-
0	SC1CMD	Synchronous serial/ full duplex UART selection 0:Synchronous serial 1:Full duplex UART

■ Serial interface 1 Mode Register 2 (SC1MD2:0x03F9F)

bp	7	6	5	4	3	2	1	0
Flag	SC1FM1	SC1FM0	SC1PM1	SC1PM0	SC1NPE	-	SC1BRKF	SC1BRKE
Reset	0	0	0	0	0	-	0	0
Access	R/W	R/W	R/W	R/W	R/W	-	R	R/W

bp	Flag	Description
7-6	SC1FM1 SC1FM0	Frame mode specification 00:7 data bit + 1 stop bit 01:7 data bit + 2 stop bit 10:8 data bit + 1 stop bit 11:8 data bit + 2 stop bit
5-4	SC1PM1 SC1PM0	Added bit specification Transmission Reception 00:Add "0" Check for 0 01:Add "1" Check for 1 10:Add odd parity Check for odd parity 11:Add even parity Check for even parity
3	SC1NPE	Parity enable 0:Enable parity bit 1:Disable parity bit
2	-	-
1	SC1BRKF	Break status receive monitor 0:Data reception 1:Break reception
0	SC1BRKE	Break status transmit control 0:Data transmission 1:Break transmission

■ Serial interface 1 Mode Register 3 (SC1MD3:0x03FA0)

bp	7	6	5	4	3	2	1	0
Flag	SC1FDC1	SC1FDC0	-	-	SC1PSCE	SC1PSC2	SC1PSC1	SC1PSC1
Reset	0	0	-	-	0	0	0	0
Access	R/W	R/W	-	-	R/W	R/W	R/W	R/W

bp	Flag	Description
7-6	SC1FDC1 SC1FDC0	Output selection after SBO1 final data transmit 00:Fix at "1" (High) output 01:Final data hold 10:Fix at "0" (Low) output 11:Reserved
5-4	-	-
3	SC1PSCE	Prescaler count control 0:Count is forbidden 1:Count is allowed
2-0	SC1PSC2 SC1PSC1 SC1PSC1	Selection clock 000:fosc/2 001:fosc/4 010:fosc/16 011:fosc/64 100:fs/2 101:fs/4 110:Timer 4 output 111:Timer 5 output

■ Serial interface 1 Status Register (SC1STR:0x03FA1)

bp	7	6	5	4	3	2	1	0
Flag	SC1TBSY	SC1RBSY	SC1TEMP	SC1REMP	SC1FEF	SC1PEK	SC1ORE	SC1ERE
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R

bp	Flag	Description
7	SC1TBSY	Serial bus status 0:Other use 1:Serial transmission in progress
6	SC1RBSY	Serial bus status 0:Other use 1:Serial reception in progress
5	SC1TEMP	Transfer buffer empty flag 0:Empty 1:Full
4	SC1REMP	Receive buffer empty flag 0:Empty 1:Full
3	SC1FEF	Framing error detection 0:No error 1:Error
2	SC1PEK	Parity error detection 0:No error 1:Error
1	SC1ORE	Overrun error detection 0:No error 1:Error
0	SC1ERE	Error monitor flag 0:No error 1:Error

12.3 Operation

Serial interface 1 can be used for both clock synchronous and full duplex UART.

12.3.1 Clock Synchronous Serial Interface

■ Activation Factor for Communication

Table:12.3.1 shows activation factors for communication. At master communication, the transfer clock is generated by setting data to the transmission data buffer TXBUF1, or by receiving a start condition. Except during communication, the input signal from SBT1 pin is masked to prevent errors by noise or so.This mask can be released automatically by setting a data to TXBUF1 (access to the TXBUF1 register), or by inputting a start condition to the data input pin. Therefore, at slave communication, set data to TXBUF1, or input an external clock after a start condition is input.

However, the external clock should be input after more than 3.5 transfer clock interval after the data set to TXBUF1. This wait time is needed to load the data from TXBUF1 to the internal shift register.

Table:12.3.1 Synchronous Serial Interface Activation Factor

	Activation factor	
	Transmission	Reception
At master	Set transmission data	Set dummy data
		Input start condition
At slave	Input clock after transmission data is set	Input clock after dummy data is set
		Input clock after start condition is input

■ Transfer Bit Setup

The transfer bit count is selected from 1 to 8 bits. Set them by the SC1LNG 2 to 0 flag of the SC1MD0 register (at reset:111). The SC1LNG2 to 0 flag holds the former set value until it is set again.

Except during communication, SBT1 pin is masked to prevent errors by noise. At slave communication, set data to TXBUF1 or input a clock to SBT1 pin after a start condition is input.

To communicate properly, more than 3.5 transfer clock after the data set to TXBUF1 is needed to input the external clock.

■ Start Condition Setup

The SC1STE flag of the SC1MD0 register sets if a start condition is enabled or not.

The start condition is regarded that when SC1CE1 flag of SC1MD0 is set to "0" and a clock line (SBT1 pin) is "H", data line (SBI1 pin (with 3 lines) or SBO1 pin (with 2 lines)) is changed from "H" to "L". Also, it is regarded that when SC1CE1 flag is set to "0" and a clock line (SBT1 pin) is "L", data line (SBI1 pin (with 3 lines) or SBO1 pin (with 2 lines)) is changed from "H" to "L".

Both the SC1SBOS flag and the SC1SBIS flag of the SC1MD1 register should be set to "0", before the start condition setup is changed.

At the selection of the start condition "enable" and master transmission / reception, after the start condition output, start condition is input from the slave, then data transmission is generated.

■ First Transfer Bit Setup

The SC1DIR flag of the SC1MD0 register can set the transfer bit. MSB first or LSB first can be selected.

■ Transmission Data Buffer

The transmission data buffer, TXBUF1 is a buffer of reserve that stores data to load the internal shift register. Data to be transferred should be set to the transmission data buffer, TXBUF1, to be loaded to the internal shift register automatically. The data load time of 3 transfer clock is needed to load the data. On loading, setting the data to TXBUF1 again may cause error. On loading or not is determined by monitoring the transmission buffer empty flag of the SC1STR. When the data is set to TXBUF1, SC1TEMP flag is set to "1" and when loading is finished, it is cleared "0" automatically.

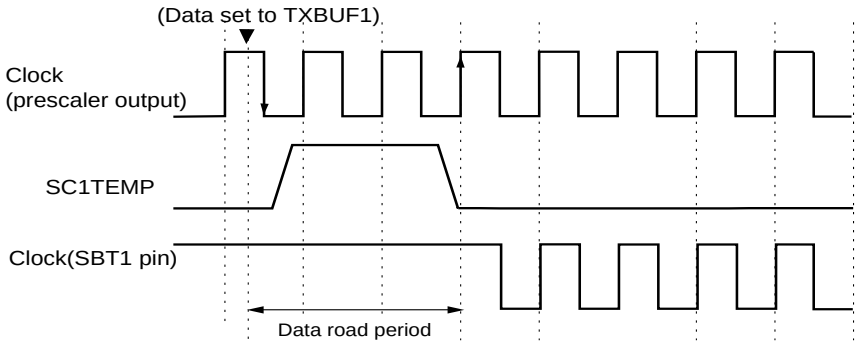


Figure:12.3.1

■ Received Date Buffer

The received data buffer RXBUF1 is a buffer of reserve that pushed the received data in the internal shift register. After the communication complete interrupt SC1TIRQ is generated, all data stored in the internal shift register are stored to the received data buffer RXBUF1 automatically. RXBUF1 can store data up to 1 byte. RXBUF1 is rewritten in every time when communication is completed, so read out data of RXBUF1 till the next receive is completed. The received data buffer empty flag SC1REMP is set to "1" at the same time SC1TIRQ is generated. SC1REMP is cleared to "0" after RXBUF1 is read out.

If a start condition is input to restart during communication, the transmission data is not valid. Set the transmission data to TXBUF1 again to operate the transmission again.

RXBUF1 is rewritten every time when communication is completed. At continuous communication, data of RXBUF1 should be read out until the next reception is completed.

■ Transfer Bit Count and First Transfer Bit

When the transfer bit is 1 bit to 7bit, the data storing method to the transmission data buffer TXBUF1 is different, depending on the first transfer bit selection. At MSB first, use the upper bits of TXBUF1 for storing. When there are 6 bits to be transferred, as shown on Figure:12.3.2, if data "A" to "F" are stored to bp2 to bp7 of TXBUF1, the transmission is operated from "F" to "A". At LSB first, use the lower bits of TXBUF1 for storing. When there are 6 bits to be transferred, as shown on Figure:12.3.3, if data "A" to "F" are stored to bp0 to bp5 of TXBUF1, the transmission is operated from "A" to "F".

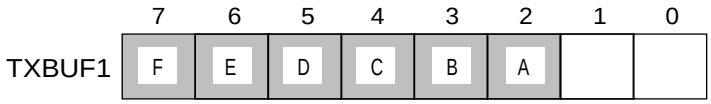


Figure:12.3.2 Transfer Bit Count and First Transfer Bit (starting with MSB)

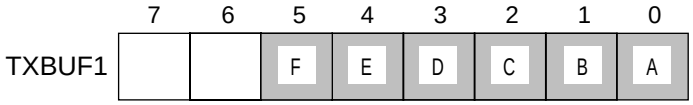


Figure:12.3.3 Transfer Bit Count and First Transfer Bit (starting with LSB)

■ Receive Bit Count and First Transfer Bit

When the transfer bit count is 1 bit to 7 bits, the data storing method to the received data buffer RXBUF1 is different depending on the first transfer bit. At MSB first, data are stored to the lower bits of RXBUF1. When there are 6 bits to be transferred, as shown on figure Figure:12.3.4, if data "A" to "F" are stored to bp0 to bp5 of RXBUF1, the transmission is operated from "F" to "A". At LSB first, data are stored to the upper bits of RXBUF1. When there are 6 bits to be transferred, as shown on Figure:12.3.5, if data "A" to "F" are stored to bp2 to bp7 of RXBUF1, the transmission is operated from "A" to "F".

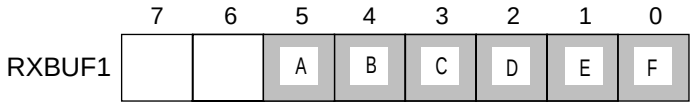


Figure:12.3.4 Receive Bit Count and Transfer First Bit (starting with MSB bit)

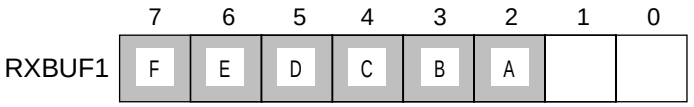


Figure:12.3.5 Receive Bit Count and Transfer First Bit (starting with LSB bit)

When the serial transfer bit is set between 1 to 7, the data except for received data of the specified transfer bit count is unknown. Use the received data after being masked by AND/ OR instruction.

■ Continuous Mode

This serial has a function for continuous communication. If data is set to the transmission data buffer TXBUF1 during communication, the transmission buffer empty flag SC1TEMP is automatically set to interrupt SC1TIRQ is generated after the former data is set. Data setup to TXBUF1 should be done till the communication complete interrupt SC1TIRQ is generated after the data is loaded to the internal shift register. At master communication, there is output after the pension of communication for 4 transfer clocks till the next transmission clock is output after the SC1TIRQ generation.

■ ATC Automatic Continuous Transfer

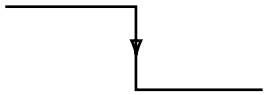
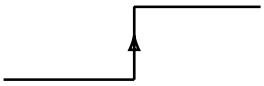
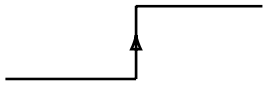
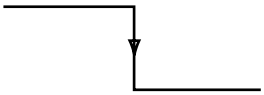
This serial enables the start-up by the data automatic transfer (ATC1). On start-up by ATC1, 255 bytes data transfer can be operated.

Refer to [chapter 18 Automatic Transfer Controller : overview : transfer mode 8 to 9 about the generation of ATC1.]

■ Input Edge/ Output Edge Setup

The SC1CE1 flag of the SC1MD0 register set an output edge of the transmission data, an input edge of the received data. As the SC1CE1 flag = "0", the transmission data is output at the falling edge, and as "1", output at the rising edge. As SC1CE1 = "0", the received data is received at the inversion edge to the output edge of transmission data, and as "1", stored at the same edge.

Table:12.3.2 Transmission Data Output Edge and Received Data Input Edge

SC1CE1	Transmission data output edge	Received data input edge
0		
1		

■ Clock Setup

The SC1PSC2 to 0 of the SC1MD3 register selects the clock source from the special prescaler and timer 4, timer 5 (2 lines) output. The special prescaler starts its operation after the SC1PSCE flag of the SC1MD1 register selects "enable count". The SC1MST flag of the SC1MD1 register can select the internal clock (clock master), or the external clock (clock slave). Even if the external clock is selected, set the internal clock that has the same clock cycle or lower to the external clock, by the SC1MD3 register.

Table:12.3.3 Synchronous Serial Interface Clock Source

	serial 1
Clock source (internal clock)	fosc/2
	fosc/4
	fosc/16
	fosc/64
	fs/2
	fs/4
	Timer 4 output
	Timer 5 output

When the clock setup is switched, the SC1SBIS flag and SC1SBOS flag of the SC1MD1 register should be set to "0".

When the slave reception is done with enabled start condition, set the speed of the transfer clock slower than the system clock.

■ Data Input Pin Setup

3 channels type (clock pin (SBT1 pin), data output pin (SBO1 pin), data input pin (SBI1 pin)) or 2 channels type (clock pin (SBT1 pin), data I/O pin (SBO1 pin)) can be selected as a communication mode. SBI1 pin can be used for only serial data input. SBO1 pin can select serial data input or output. The SC1IOM flag of the SC1MD1 register can select if the serial data is input to SBI1 pin or SBO1 pin. When "data input from SBO1 pin" is selected to set the 2 lines type, the P3DIR0 flag of the P3DIR register controls direction of SBO1 pin to switch transmission/ reception. At this time, SBI1 pin can be used as a general port, too.

The transfer speed should be up to 5.0 MHz. If the transfer clock is over 5.0 MHz, the transmission data may not be sent correctly.

At reception, if SC1IOM of the SC1MD1 register is set to "1" and "serial data input from SBO1" is selected, SBI1 pin can be used as a general port.

■ Reception Buffer Empty Flag

After reception is completed (SC1TIRQ is generated), data is automatically stored to RXBUF1 from the internal shift register. If data is stored to the shift register RXBUF1 when the SC1SBIS of the SC1MD1 register is set to "serial input", the reception buffer empty flag SC1REMP of the SC1STR register is set to "1". This indicates that the received data is going to read out. SC1REMP is cleared to "0" by reading out the data of RXBUF1.

■ Transmission Buffer Empty Flag

During the communication (after setting data to TXBUF1 and before the communication complete interrupt SC1TIRQ is generated) if any data is set to TXBUF1 again, the transmission buffer empty flag SC1REMP of the SC1STR register is set to "1". This indicates that the next transmission data is going to be loaded. Data is loaded to the inside shift register from TXBUF1 by generation of SC1TIRQ, and the next transfer is started as SC1TEMP is cleared to "0".

■ Overrun Error and Error Monitor Flag

After reception complete, if the next data has been already received before reading out of the data of the received data buffer RXBUF1, overrun error is generated and the SC1ORE flag of the SC1STR register is set to "1". At the same time, the error monitor flag SC1ERE is set to indicate that error is occurred on reception. The SC1ERE flag is not cleared till the next communication complete interrupt SC1TIRQ is generated after loading data of the RXBUF1. SC1ERE is cleared as SC1ORE flag is cleared. These error flags have no effect on communication operation.

■ Reception BUSY Flag

If the data is set to the TXBUF1 or recognized the start condition when the SC1SBIS flag of the SC1MD1 register is set to "serial data input", the BUSY flag SC1RBSY of the SC1STR register is set to "1". And, on the generation of the communication complete interrupt SC1TIRQ, the flag is cleared to "0". And, during continuous communication, the SC1RBSY flag is always set. If the transmission buffer empty flag SC1TEMP is cleared to "0" as the communication complete interrupt SC1TIRQ is generated, SC1RBSY is cleared to "0". If the SC1SBIS flag is set to "0" during communication, the SC1RBSY flag is cleared to "0".

■ Transmission BUSY Flag

Data is set to the TXBUF1 or recognized the start condition when the SC1SBOS flag of the SC1MD1 register is set to "serial data output", if the SC1SBOS flag of the SC1MD1 register is "1", SC1TBSY flag of the SC1STR register is set. And, on the generation of the communication complete interrupt SC1TIRQ, the flag is cleared "0". And, during continuous communication, the SC1TBSY flag is always set. If the transmission buffer empty flag SC1TEMP is cleared to "0" as the communication complete interrupt SC1TIRQ is generated,SC1TBSY is cleared to "0". If the SC1SBOS flag is set to "0" during communication, the SC1TBSy flag is cleared to "0".

■ Emergency Reset

This serial interface contains emergency reset for abnormal operation. For emergency reset, the SC1SBOS flag and the SC1SBIOS flag of the SC1MD1 register should be set to "0" (SBO1 pin:port, input data:"1" input).

At emergency reset, the status register (the SC1BRKF flag of the SC1MD2 register, all flags of the SC1STR register) are initialized as they are set at reset, but the control register holds the set value.

■ Last Bit of Transfer Data

Table:12.3.4 shows the data output holding period of the last bit at transmission, and the minimum data input period of the last bit at reception. The internal clock should be set up at slave to keep the data hold time at reception.

Table:12.3.4 Last Bit Data Length of Transfer Data

	The last bit data holding period at transmission	The last data input period at reception
At master	1 bit data length	1 bit data length (Minimum)
At slave	[1 bit data length of external clock × 1/2] + [internal clock cycle × (1/2-3/2)]	

In the case of disabled start condition (at SC1STE flag = 0), the SBO1 output after the data output holding period of the final bit can be set as Table:12.3.5 by the setting value of the SC1FDC1 to 0 flag of the SC1MD3 register.

After released the reset, despite of the setting value of the SC1FDC1 to 0 flag, output before the serial transfer is "H". In the case of the enabled start condition (at SC1STE flag = 1), "H" is output despite of the setting value of the SC1FDC1 to 0.

Table:12.3.5 SBO1 Output after the Data Output Holding Period of the Last Bit (without start condition)

SC1FDC1 flag	SC1FDC0 flag	SBO1 output after the data output holding period of the last bit
0	0	"1"(High) output fix
1	0	Last data holding
0	1	"0"(Low) output fix
1	1	Reserved

■ Other Control Flag Setup

Table:12.3.6 shows flags that are not used at clock synchronous communication. So, they are not needed to set or monitor.

Table:12.3.6 Other Control Flag

Register	Flag	Detail
SC1MD2	SC1BRKE	Break status transmission control
	SC1BRKF	Break status reception monitor
	SC1NPE	Parity enable
	SC1PM1 to 0	Added mode specification
	SC1FM1 to 0	Frame mode specification
SC1STR	SC1PEK	Parity error detection
	SC1FEF	Frame error detection

■ Transmission Timing

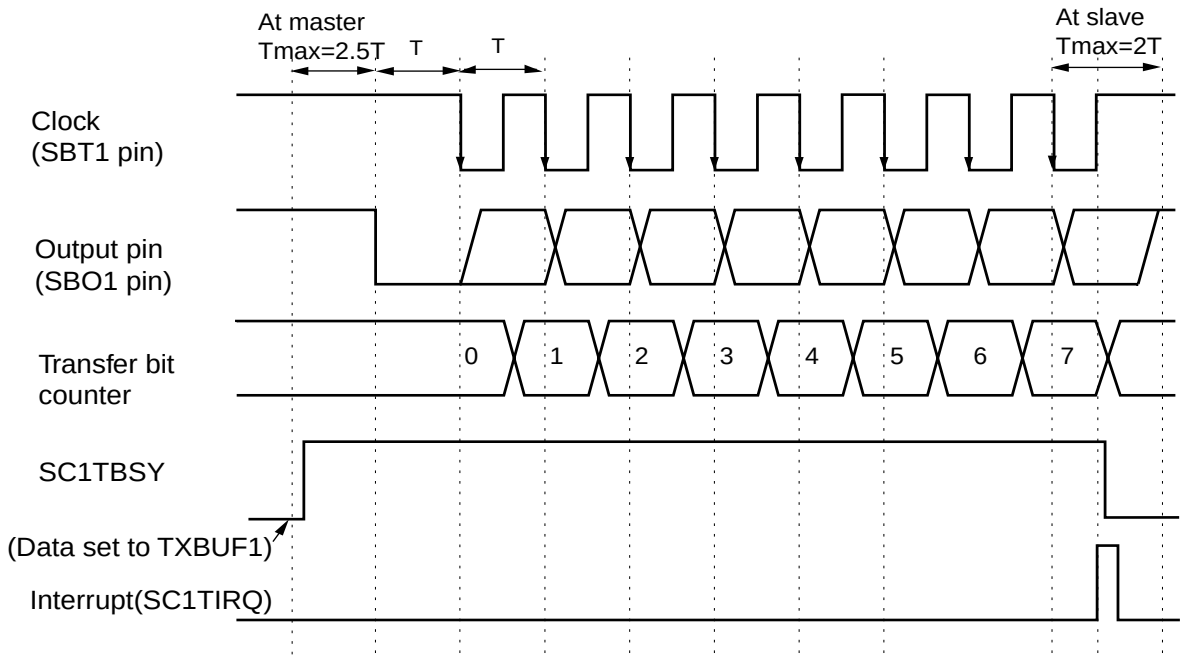


Figure:12.3.6 Transmission Timing (at falling edge, start condition is enabled)

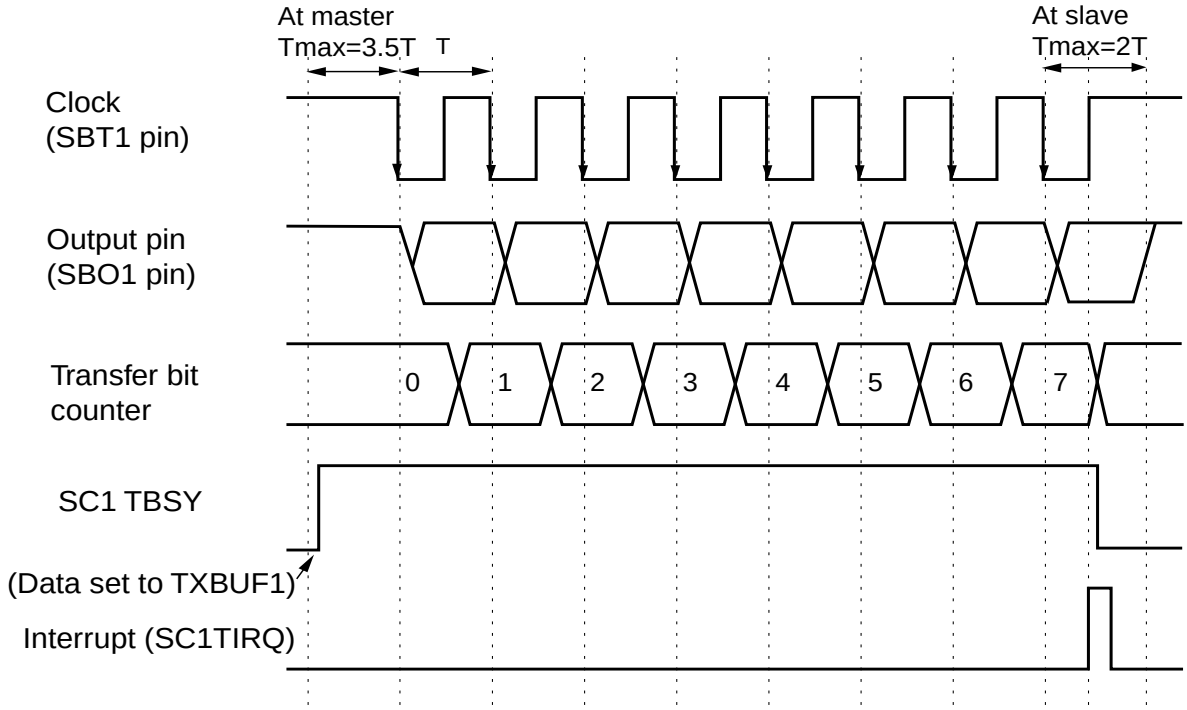


Figure:12.3.7 Transmission Timing (at falling edge, start condition is disabled)

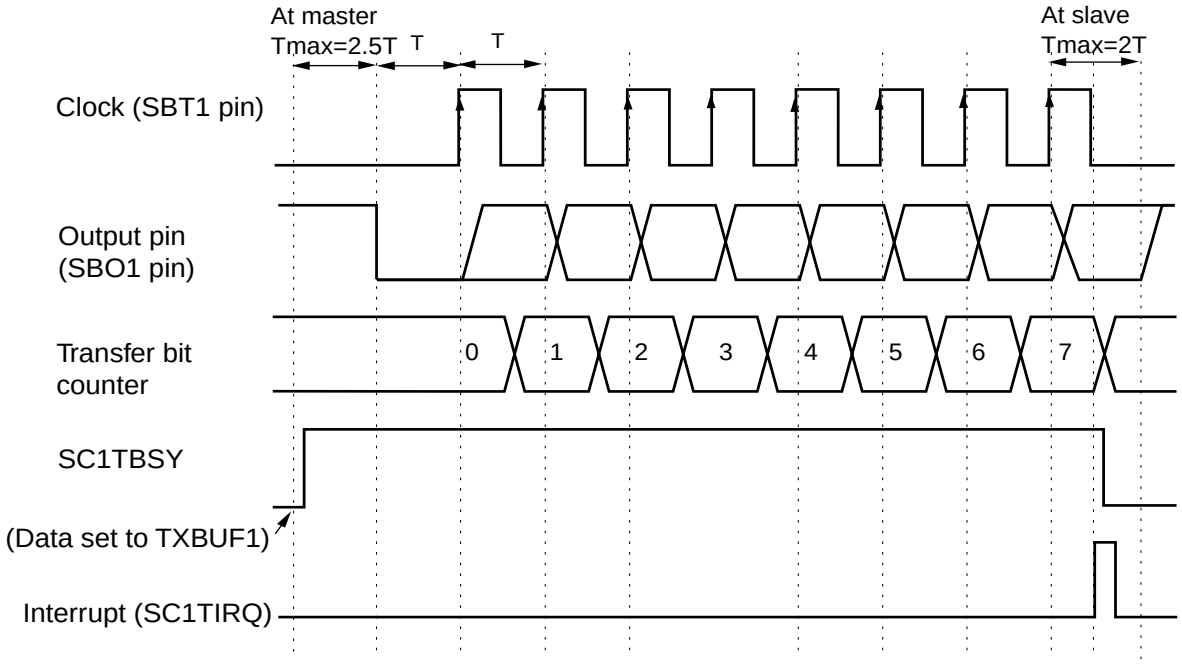


Figure:12.3.8 Transmission Timing (at rising edge, start condition is enabled)

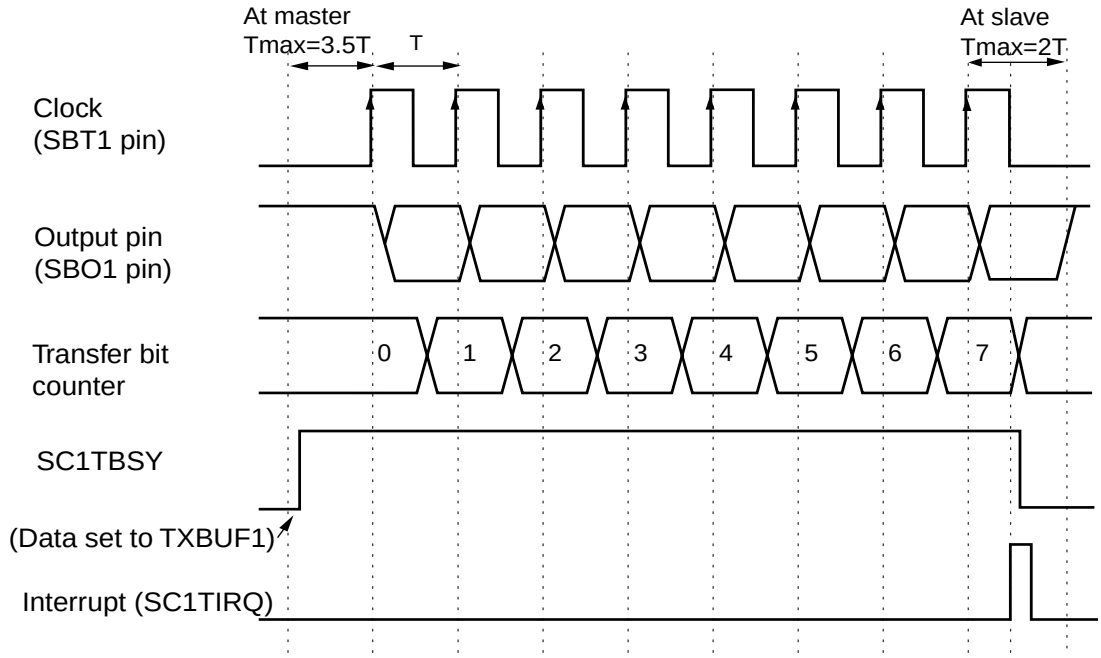


Figure:12.3.9 Transmission Timing (at rising edge, start condition is disabled)

■ Reception Timing

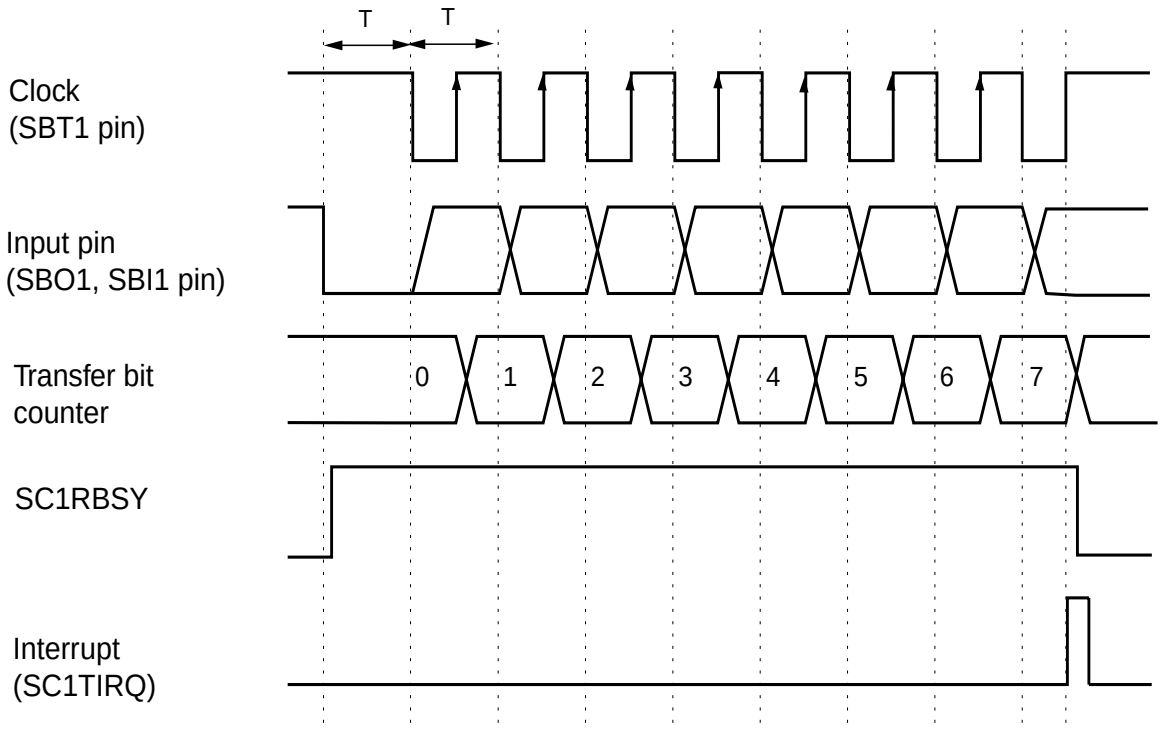


Figure:12.3.10 Reception Timing (at rising edge, start condition is enabled)

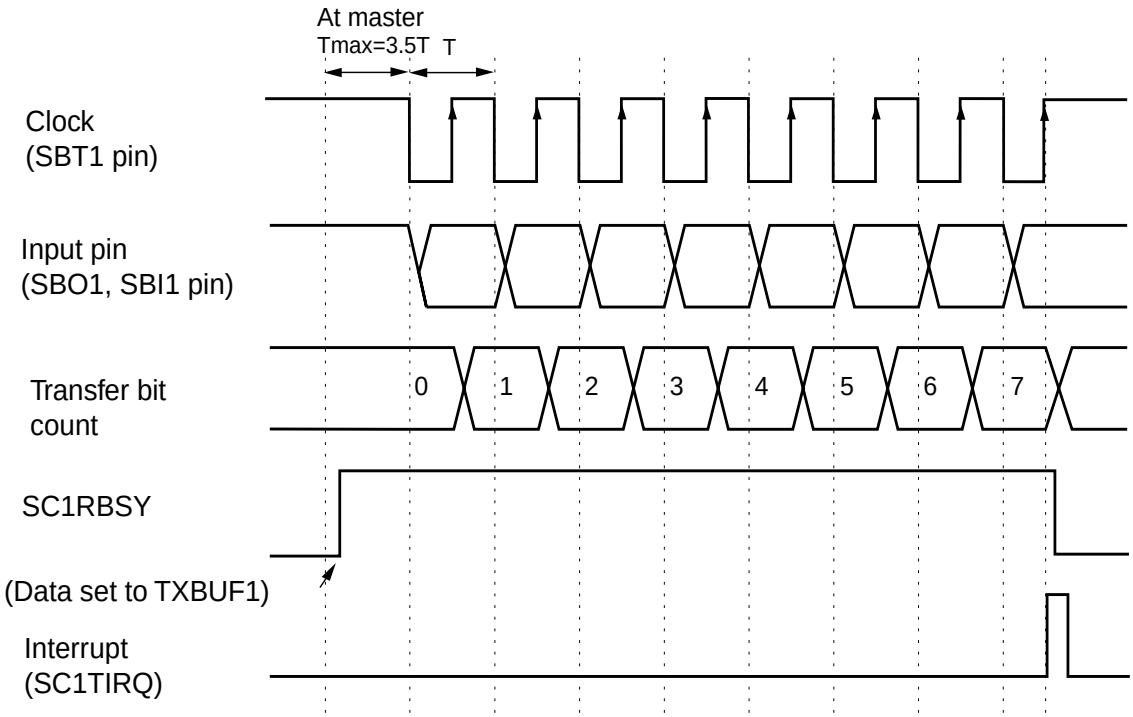


Figure:12.3.11 Reception Timing (at rising edge, start condition is disabled)

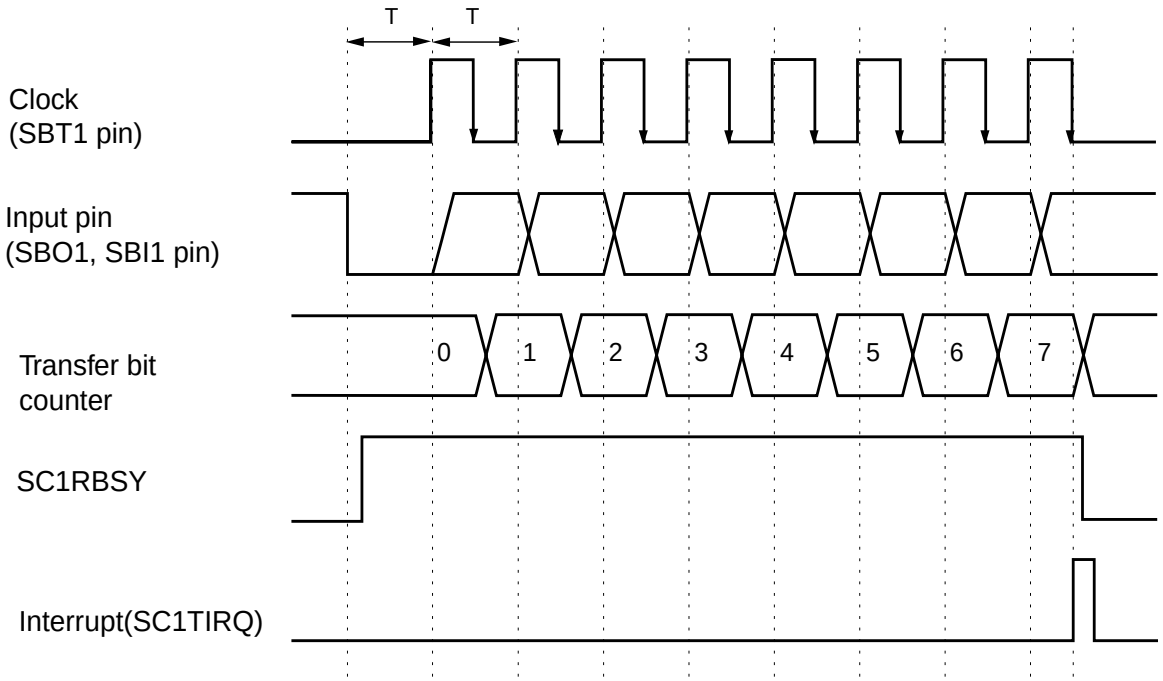


Figure:12.3.12 Reception Timing (at falling edge, start condition is enabled)

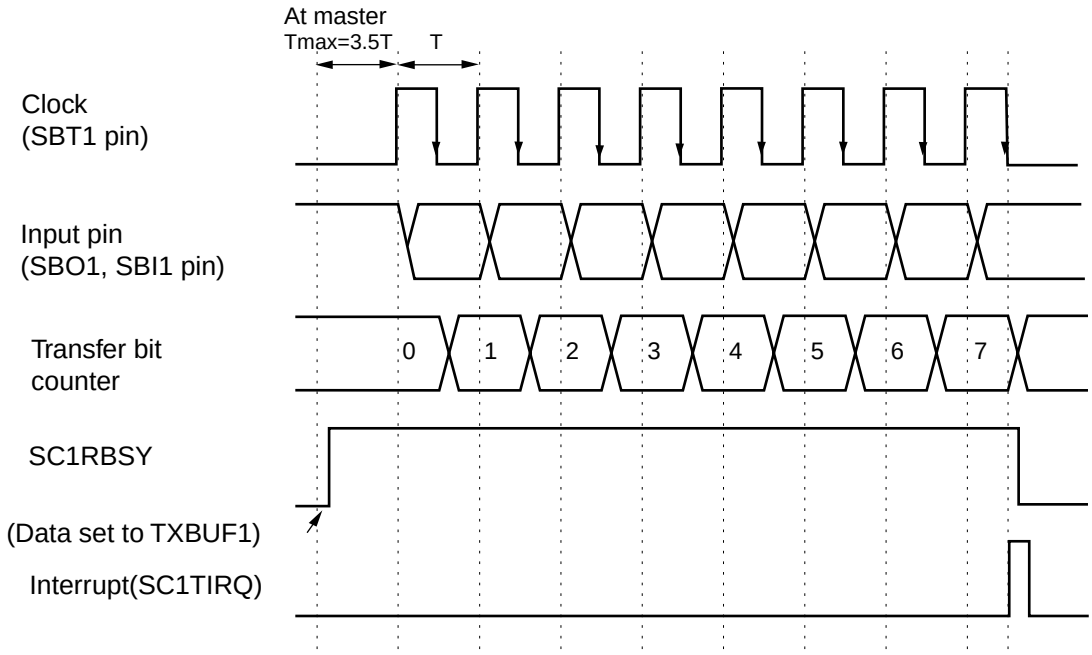


Figure:12.3.13 Reception Timing (at falling edge, start condition is disabled)

■ Transmission/ Reception Timing

When transmission and reception are operated at the same time, set the SC1CE1 flag of the SC1MD0 register to "0" or "1". Data is received at the opposite output edge of the transmission data, so that the input edge of the received data should be the opposite output edge of the transmission data from the other side.

Also, in the case transmission/ reception is done with the start condition, opposite of the communication should be done with the same condition to communicate properly. The normal communication may not be operated.

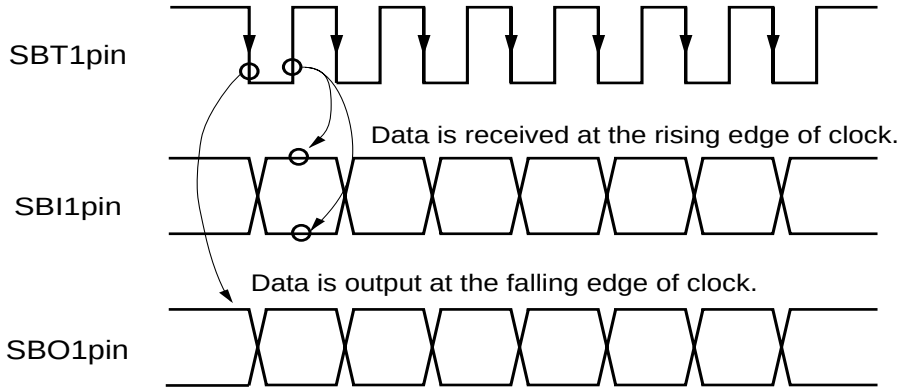


Figure:12.3.14 Transmission/ Reception Timing (Reception:at rising edge, Transmission:at falling edge)

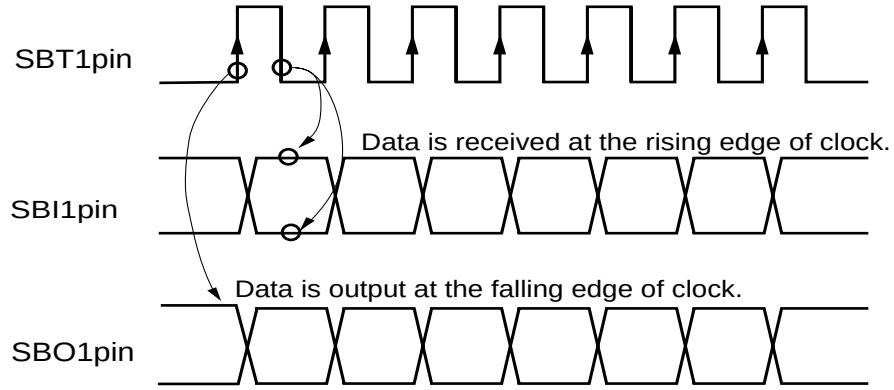


Figure:12.3.15 Transmission/ Reception Timing (Reception:at falling edge, Transmission:at rising edge)

■ Communication Function at Standby Mode

This serial interface has the following way about the return from the standby mode.

This serial interface can do the slave reception at the standby mode. CPU operation status can be recovered from standby to normal by the communication complete interrupt SC1TIRQ that is generated after the slave reception.

(At the standby mode, if the transfer bit count data is received once that is set by the SC1LNG2 to 0 flag of the SC1MD0 register, the continuous reception is not available because the next data is not allowed.) The received data should be read out from the received data buffer RXBUF1 after recovering the normal mode.

In the reception at the standby mode, the communication with enabled start condition is not available. Disable the start condition. The dummy data should be set to the transmission data buffer TXBUF1 before the transition to the standby mode.

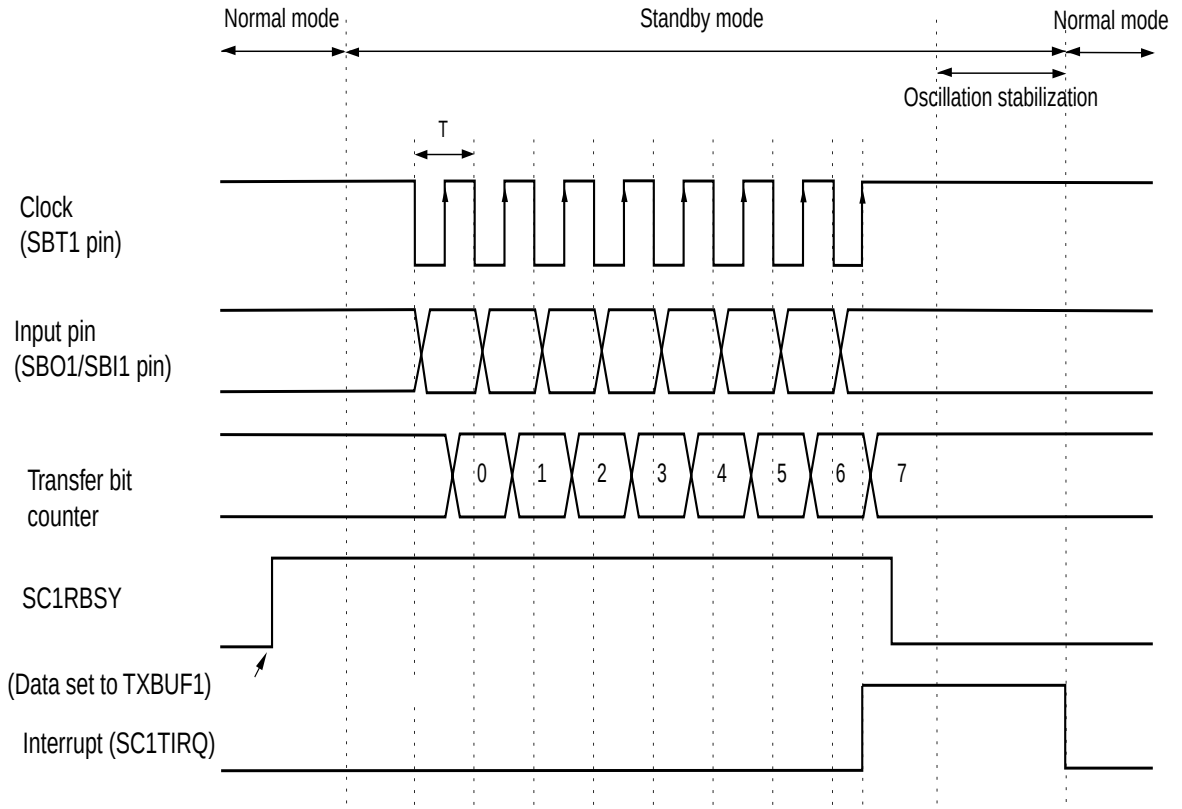


Figure:12.3.16 Reception Timing at Standby Mode (Reception:at rising edge, start condition is disabled)

■ Pins Setup (with 3 channels, at transmission)

Table:12.3.7 shows the setup for synchronous serial interface pin with 3 channels (SBO1 pin, SBI1 pin, SBT1 pin) at transmission.

Table:12.3.7 Setup for Synchronous Serial Interface Pin (with 3 channels, at transmission)

Setup item	Data output pin	Data input pin	Clock I/O pin	
	SBO1 pin	SBI1 pin	SBT1 pin	
			Clock master	Clock slave
			SC1MD1(SC1MST)	
Port pin	P30	P31	P32	
Serial data input selection	SBI1		-	
	SC1MD1(SC1IOM)			
Function	Serial data output	"1" input	Transfer clock input/ output	Transfer clock input/ output
	SC1MD1(SC1SBOS)	SC1MD1(SC1SBIS)	SC1MD1(SC1SBTS)	
Style	Push-pull/ Nch open-drain	-	Push-pull/ Nch open-drain	Push-pull/ Nch open-drain
	P3ODC(P3ODC0)		P3ODC(P3ODC2)	
I/O	Output mode	-	Output mode	Input mode
	P3DIR(P3DIR0)		P3DIR(P3DIR2)	
Pull-up setup	Added/ Not added	-	Added/ Not added	Added/ Not added
	P3PLU(P3PLU0)		P3PLU(P3PLU2)	

■ Pins Setup (with 3 channels, at reception)

Table:12.3.8 shows the setup for synchronous serial interface pin with 3 channels (SBO1 pin, SBI1 pin, SBT1 pin) at reception.

Table:12.3.8 Setup for Synchronous Serial Interface Pin (with 3 channels, at reception)

Setup item	Data output pin	Data input pin	Clock I/O pin	
	SBO1 pin	SBI1 pin	SBT1 pin	
			Clock master	Clock slave
			SC1MD1(SC1MST)	
Port pin	P30	P31	P32	
Serial data input selection	SBI1		-	
	SC1MD1(SC1IOM)			
Function	Port	Serial input	Transfer clock input/ output	Transfer clock input/ output
	P3DIR(P3DIR0)	SC1MD1(SC1SBIS)	SC1MD1(SC1SBTS)	
Style	-	-	Push-pull/ Nch open-drain	Push-pull/ Nch open-drain
			P3ODC(P3ODC2)	
I/O	-	Input mode	Output mode	Input mode
		P3DIR(P3DIR1)	P3DIR(P3DIR2)	
Pull-up setup	-	-	Added/ Not added	Added/ Not added
			P3PLU(P3PLU2)	

■ Pins Setup (with 3 channels, at transmission / reception)

Table:12.3.9 shows the setup for synchronous serial interface pin with 3 channels (SBO1 pin, SBI1 pin, SBT1 pin) at transmission / reception.

Table:12.3.9 Setup for Synchronous Serial Interface Pin (with 3 channels, at transmission / reception)

Setup item	Data output pin	Data input pin	Clock I/O pin	
	SBO1 pin	SBI1 pin	SBT1 pin	
			Clock master	Clock slave
			SC1MD1(SC1MST)	
Port pin	P30	P31	P32	
Serial data input selection	SBI1		-	
	SC1MD1(SC1IOM)			
Function	Serial data output	Serial input	Transfer clock input/ output	Transfer clock input/ output
	SC1MD1(SC1SBOS)	SC1MD1(SC1SBIS)	SC1MD1(SC1SBTS)	
Style	Push-pull/ Nch open-drain	-	Push-pull/ Nch open-drain	Push-pull/ Nch open-drain
	P3ODC(P3ODC0)		P3ODC(P3ODC2)	
I/O	Output mode	Input mode	Output mode	Input mode
	P3DIR(P3DIR0)	P3DIR(P3DIR1)	P3DIR(P3DIR2)	
Pull-up setup	Added/ Not added	-	Added/ Not added	Added/ Not added
	P3PLU(P3PLU0)		P3PLU(P3PLU2)	

■ Pins Setup (with 2 channels, at transmission)

Table:12.3.10 shows the setup for synchronous serial interface pin with 2 channels (SBO1 pin, SBT1 pin) at transmission. SBI1 pin can be used as a port.

Table:12.3.10 Setup for Synchronous Serial Interface Pin (with 2 channels, at transmission)

Setup item	Data output pin	Serial unused pin	Clock I/O pin	
	SBO1 pin	SBI1 pin	SBT1 pin	
			Clock master	Clock slave
			SC1MD1(SC1MST)	
Port pin	P30	P31	P32	
Serial data input selection	SBI1		-	
	SC1MD1(SC1IOM)			
Function	Serial data input	"1" input	Transfer clock input/ output	Transfer clock input/ output
	SC1MD1(SC1SBOS)	SC1MD1(SC1SBIS)	SC1MD1(SC1MST)	
Style	Push-pull/ Nch open-drain	-	Push-pull/ Nch open-drain	Push-pull/ Nch open-drain
	P3ODC(P3ODC0)		P3ODC(P3ODC2)	
I/O	Output mode	-	Output mode	Input mode
	P3DIR(P3DIR0)		P3DIR(P3DIR2)	
Pull-up setup	Added/ Not added	-	Added/ Not added	Added/ Not added
	P3PLU(P3PLU0)		P3PLU(P3PLU2)	

■ Pins Setup (with 2 channels, at reception)

Table:12.3.11 shows the setup for synchronous serial interface pin with 2 channels (SBO1 pin, SBT1 pin) at reception. SBI1 pin can be used as a port.

Table:12.3.11 Setup for Synchronous Serial Interface Pin (with 2 channels, at reception)

Setup item	Data output pin	Serial unused pin	Clock I/O pin	
	SBO1 pin	SBI1 pin	SBT1 pin	
			Clock master	Clock slave
			SC1MD1(SC1MST)	
Port pin	P30	P31	P32	
Serial data input selection	SBI1		-	
	SC1MD1(SC1IOM)			
Function	Port	Serial input	Transfer clock input/ output	Transfer clock input/ output
	SC1MD1(SC1SBOS)	SC1MD1(SC1SBIS)	SC1MD1(SC1SBIS)	
Style	-	-	Push-pull/ Nch open-drain	Push-pull/ Nch open-drain
			P3ODC(P3ODC2)	
I/O	Input mode	-	Output mode	Input mode
	P3DIR(P3DIR0)		P3DIR(P3DIR2)	
Pull-up setup	-	-	Added/ Not added	Added/ Not added
			P3PLU(P3PLU2)	

12.3.2 Setup Example

■ Transmission / Reception Setup Example

The setup example for clock synchronous serial communication with serial 1 is shown. Table:12.3.12 shows the conditions at transmission / reception.

Table:12.3.12 Setup Examples for Synchronous Serial Interface Transmission / Reception

Setup item	Set to
Serial data input pin	Independent(3 channels)
Transfer bit count	8 bit
Start condition	None
First transfer bit	MSB
Input edge	Falling edge
Output edge	Rising edge
Clock	Clock master
Clock source	fs/2
Clock source 1/8 dividing	Not divided by 8
SBT1/SBO1 pin style	Nch open-drain
SBT1 pin pull-up resistor	Added
SBO1 pin pull-up resistor	Added
serial 1 communication complete interrupt	Enable
SBO1 output after last data output	"1"(H) fix

An example setup procedure, with a description of each step is shown below.

Setup Procedure	Description
(1) Select the prescaler operation SC1MD3(0x03FA0) bp3 :SC1PSCE =1	(1) Set the SC1PSCE flag of the SC1MD3 register to "1" to select "prescaler operation".
(2) Select the clock source SC1MD3(0x03FA0) bp2-0 :SC1PSC2-0 =100	(2) Set the SC1PSC2 to 0 flag of the SC1MD3 register to "100" to select the fs/2 to clock source.
(3) SBO1A output control after the last data output SC1MD3(0x03FA0) bp7,6 :SC1FDC1-0 =00	(3) Set the SC1FDC1 to 0 flag of the SC1MD3 register to "00" to select "1" (High) fix of the SBO1 last data output.

Setup Procedure	Description
(4) Control the pin style P3ODC(0x03F2C) bp2,0 :P3ODC2,0 =1,1 P3PLU(0x03F43) bp2,0 :P3PLU2,0 =1,1	(4) Set the P3ODC2, P3ODC0 flag of the P3ODC register (P3DIR) to "1,1" and select the Nch open drain at SBO1/SBT1 pins. Then set the P1PLU2, P1PLU0 flag of the P3PLU register to "1,1" and select enable pull up resistance.
(5) Control the pin direction P3DIR(0x03F43) bp2,1,0 :P3DIR2,1,0 =1,0,1	(5) Set the P3DIR2, P3DIR0 flag of the Port 3 pin direction control register (P3DIR) to "1,1" and the P3DIR3 flag to "0" to set P32, P30 to the output mode, P31 to the input mode.
(6) Set the SC1MD0 register Select the transfer bit count SC1MD0(0x03F9D) bp2-0 :SC1LNG2-0 =111 Select the start condition SC1MD0(0x03F9D) bp3 :SC1STE =0 Select the first bit to be transferred SC1MD0(0x03F9D) bp4 :SC1DIR =0 Select the transfer edge SC1MD0(0x03F9D) bp7 :SC1CE1 =1	(6) Set the SC1LNG2 to 0 flag of the serial 1 mode register 0 (SC1MD0) to "111" to set the transfer bit count "8 bits". Set the SC1STE flag of the SC1MD0 register to "0" to disable the start condition. Set the SC1DIR flag of the SC1MD0 register to "0" to set MSB as a transfer first bit. Set the SC1CE1 flag of the SC1MD0 register to "1" to set the reception data input edge "falling" and the transmission data output edge "rising".
(7) Set the SC1MD1 register Select the communication style SC1MD1(0x03F9E) bp0 :SC1CMD =0 Select the transfer clock SC1MD1(0x03F9E) bp2 :SC1MST =1 bp3 :SC1CKM =0 Select the transfer clock SC1MD1(0x03F9E) bp4 :SC1SBOS =1 bp5 :SC1SBIS =1 bp6 :SC1SBTS =1 bp7 :SC1IOM =0	(7) Set the SC1CMD flag of the SC1MD1 register to "0" to select the synchronous serial. Set the SC1MST flag of the SC1MD1 register to "0" to select the clock master (internal clock). Set the SC1CKM flag to "0" to select "not divided by 8" for the clock source. Set the SC1SBOS, SC1SBIS, SC1SBTS flag of the SC1MD1 register to "1" to set the SBO1 pin to the serial data output, the SBI1 pin to the serial input, SBT1 pin to the transfer clock input/output. Set the SC1IOM flag "0" to set the serial data input from the SBI1 pin.
(8) Set the interrupt level SC1TICR(0x03FF5) bp7-6 :SC1LV1-0 =10	(8) Set the interrupt level by the SC1TLV1 to 0 flag of the serial 1 UART transmission interrupt control register (SC1TICR).
(9) Enable the interrupt SC1TICR(0x03FF5) bp1 :SC1TIE =1	(9) Set the SC1TIE flag of the SC1TICR register to "1" to enable the interrupt. If any interrupt request flag (SC1TIR of the SC1TICR register) is already set, clear SC1TIR before the interrupt is enabled.

Setup Procedure	Description
(10) Start the serial transmission Transmission data ý TXBUF1(0x03FA3) Received data ý input SBI1 pin	(10) Set the transmission data to the serial transmission data buffer TXBUF1. The transmission or reception is started by the internal clock generation. When the transmission finished, the serial 1 UART transmission interrupt SC1TIRQ is generated. [Chapter 3. 3-1-4 Setup]

Each procedure (1) to (3), (6), (7) ,and (8) can be set at the same time.

When only reception with 3 channels is operated, set the SC1SBIS of the SC1MD1 register to "0" and set the serial input to "1" input. The SBI1 pin can be used as a general port. Also, when only transmission is operated, set the SC1SBOS of the SC1MD1 register to "0" to select a port.

When communicate with 2 channels, the SBO1 pin inputs / outputs serial data. The port direction control register P3DIR switches I/O. At reception, set SC1SBIS of the SC1MD1 register to "1", always, to select "serial input". The SBI1 pin can be used as a general port.

This serial interface contains a emergency reset function. If the communication should be stopped by force, set SC1SBOS and SC1SBIS of the SC1MD1 register to "0".

Each flag should be set as this setup procedure in order. Activation of communication should be operated after all control registers (refer to Table:12.2.1 except TXBUF1) are set.

Transfer rate of transfer clock set by the SC1MD3 register should be under 5.0 MHz.

■ Transmission / Reception Setup Example (Standby Mode Reception)

The setup example for clock synchronous serial communication with serial 1 is shown. Table:12.3.13 shows the condition at standby mode reception.

Table:12.3.13 Setup Examples for Synchronous Serial Interface Transmission / Reception (Standby Mode Reception)

Setup item	Set to
Serial data input pin	Independent (2channels)
Transfer bit count	8 bit
Start condition	None
First transfer bit	MSB
Input edge	Falling edge
Clock	Clock slave
Operation mode	Stop mode
Clock source	fs/2
Clock source 1/8 dividing	Not divided by 8
SBT1/SBO1 pin style	Push-pull
SBT1 pin pull-up resistor	Not added
SBO1 pin pull-up resistor	Not added
serial 1 communication complete interrupt	Enable

An example setup procedure, with a description of each step is shown below.

Setup Procedure	Description
(1) Select the prescaler operation SC1MD3(0x03FA0) bp3 :SC1PSCE =1	(1) Set the SC1PSCE flag of the SC1MD3 register to "1" to select "prescaler operation".
(2) Select the clock source SC1MD3(0x03FA0) bp2-0 :SC1PSC2-0 =100	(2) Set the SC1PSC2 to 0 flag of the SC1MD3 register to "100" to select fs/2 as the clock source.
(3) Control the pin style P3ODC(0x03F2C) bp2,0 :P3ODC2,0 =0,0 P3PLU(0x03F43) bp2,0 :P3PLU2,0 =0,0	(3) Set the P3ODC2, P3ODC0 flag of the P3ODC register (P3DIR) to "0,0" and select the Nch open drain at SBO1/SBT1 pins. Then set the P1PLU2, P1PLU0 flag of the P3PLU register to "0,0" and select enable pull up resistance.
(4) Control the pin direction P3DIR(0x03F43) bp2 :P3DIR2 =0 bp1 :P3DIR1 =0 bp0 :P3DIR0 =1	(4) Set the P3DIR2, P3DIR3 flag of the Port 3 pin direction control register (P3DIR) to "0,0" and the P3DIR0 flag to "1" to set P32, P31 to the input mode.

Setup Procedure	Description
(5) ÏSelect the transfer bit count SC1MD0(0x03F9D) bp2-0 :SC1LNG2-0 =111	(5) Set the SC1LNG2 to 0 flag of the serial 1 mode register (SC1MD0) to "111" to set the transfer bit count "8 bits".
(6) Select the start condition SC1MD0(0x03F9D) bp3 :SC1STE =0	(6) Set the SC1LNG2 to 0 flag of the serial 1 mode register (SC1MD0) to "111" to disable the start condition.
(7) Select the first bit to be transferred SC1MD0(0x03F9D) bp4 :SC1DIR =0	(7) Set the SC1DIR flag of the SC1MD0 register to "0" to set MSB as a transfer first bit.
(8) Select the transfer edge SC1MD0(0x03F9D) bp7 :SC1CE1 =1	(8) Set the SC1CE1 flag of the SC1MD0 register to "1" to set the reception data input edge "falling".
(9) Select the communication type SC1MD1(0x03F9E) bp0 :SC1CMD =0	(9) Set the SC1CMD flag of the SC1MD1 register to "0" to select the synchronous serial.
(10) Select the transfer clock SC1MD1(0x03F9E) bp2 :SC1MST =0 bp3 :SC1CKM =0	(10) Set the SC1MST flag of the SC1MD1 register to "0" to select the clock slave (external slave). Set the SC1CKM flag to "0" to select "not divided by 8" for the clock source.
(11) Control the pin function SC1MD1(0x03F9E) bp4 :SC1SBOS =0 bp5 :SC1SBIS =1 bp6 :SC1SBTS =1 bp7 :SC1IOM =0	(11) Set the SC1SBOS flag of the SC1MD1 register to "0", the SC1SBTS flag of the SC1SBIS register to "1" to set the SBI1 pin to the serial data input as the SBO1 pin general port, the SBT1 pin to the transfer clock input/ output. Set the SC1IOM flag "0" to set the serial data input from the SBI1 pin.
(12) Set the interrupt level SC1TICR(0x03FF5) bp7-6 :SC1LV1-0 =10	(12) Set the interrupt level by the SC1LV1 to 0 flag of the serial 1 UART transmission interrupt control register (SC1TICR). (Set level 2)
(13) Enable the interrupt SC1TICR(0x03FF5) bp1 :SC1TIE =1	(13) Set the SC1TIE flag of the SC1TICR register to "1" to enable the interrupt. If any interrupt request flag (SC1TIR of the SC1TICR register) is already set, clear SC1TIR before the interrupt is enabled. [Chapter 3. 3-1-4 Setup]
(14) Set the startup factor of the serial communication Dummy data ý TXBUF1(0x03FA3)	(14) Set the dummy data to the serial transmission data buffer TXBUF1.
(15) Transfer to STOP mode CPUM(0x03F00) bp3:STOP =1	(15) Set the STOP flag of the CPUM register to "1" to transfer to the stop mode.
(16) Start the serial communication Transmission clock ý input SBT1 pin Received data ý input SBI1 pin	(16) Input the transfer clock to the SBT1 pin and transfer data to the SBI1 pin.

Setup Procedure	Description
(17) Recover from the standby mode	(17) The serial 1 UART transmission interrupt SC1TIRQ is generated at the same time of the 8th bits data reception, then, CPU is recovered from the stop mode to the normal mode after the oscillation stabilization wait.

Note:Each procedure (1) to (2), (5) to (8), (9) to (11) can be set at the same time.

The slave reception at the standby mode should be used without the start condition to receive properly.

Each flag should be set as this setup procedure in order. Activation of communication should be operated after all control registers (refer to Table:12.2.1 except TXBUF1) are set.

12.3.3 UART Serial Interface

serial 1 can be used for full duplex UART communication. Table:12.3.14 shows UART serial interface functions.

Table:12.3.14 URAT Serial Interface Functions

Communication style	UART (full duplex)
Interrupt	SC1TIRQ (transmission), SC1RIRQ (reception)
Used pins	TXD1 (output / input) RXD1 (input)
Specification the first transfer bit	MSB / LSB
Selection of parity bit	O
Parity bit control	0 parity 1 parity odd parity even parity
Frame selection	7 bits + 1 STOP 7 bits + 2 STOP 8 bits + 1 STOP 8 bits + 2 STOP
Continuous operation	O
Maximum transfer rate	300 kbps (standard 300 bps to 38.4 kbps) (with baud rate timer)

■ Activation Factor for Communication

At transmission, if any data is set to the transmission data buffer TXBUF1, a start condition is generated to start transfer. At reception, if a start condition is received, communication is started. At reception, if the data length of "L" for start bit is longer than 0.5 bit, that can be regarded as a start condition.

■ Transmission

Data transfer is automatically started by setting data to the transmission data buffer TXBUF1. When the transmission is completed, the serial 1 transmission interrupt SC1TIRQ is generated.

■ Reception

Once a start condition is received, reception is started after the transfer bit counter that counts transfer bit is cleared. When the reception is completed, the serial 1 reception interrupt SC1RIRQ is generated.

■ Full duplex communication

On full duplex communication, the transmission and reception can be operated separately at the same time. The frame mode and parity bit of the used data on transmission / reception should have the same polarity.

■ Transfer Bit Count Setup

The transfer bit count is automatically set after the frame mode is specified by the SC1FM1 to 0 flag of the SC1MD2 register. If the SC1CMD flag of the SC1MD1 register is set to "1", and UART communication is selected, the setup by the synchronous serial transfer bit count selection flag SC1LNG2 to 0 is no more valid.

■ Data Input Pin Setup

The communication mode can be selected from with 2 channels (data output pin (TXD1 pin), data input pin (RXD1 pin)), or with 1 channel (data I/O pin TXD1 pin). The RXD1 pin can be used only for serial data input. The TXD1 pin can be used for serial data input or output. The SC1IOM flag of the SC1MD1 register can specify which pin, RXD1 or TXD1 inputs the serial data. If "data input from TXD1 pin" is selected to be with 1 line communication, transmission / reception is switched by controlling TXD1 pin's direction by the P3DIR0 flag of the P3DIR register. At the same time, the RXD1 pin can be used as a general port.

■ Reception Buffer Empty Flag

When SC1RIRQ is generated, data is stored to RXBUF1 from the internal shift register, automatically. If data is stored to RXBUF1 from the shift register, the reception buffer empty flag SC1REMP of the SC1STR register is set to "1". That indicates that the received data is going to be read out. SC1REMP is cleared to "0" by reading out the data of RXBUF1.

■ Reception BUSY Flag

When the start condition is regarded, the SC1RBSY flag of the SC1STR register is set to "1". That is cleared to "0" by the generation of the reception complete interrupt SC1TIRQ. If the SC1SBIS flag is set to "0" during reception, the SC1RBSY flag is reset to "0".

■ Transmission BUSY Flag

When any data is set to TXBUF1, the SC1TBSY flag of the SC1STR register is set to "1". That is cleared to "0" by the generation of the transmission complete interrupt SC1TIRQ. During continuous communication the SC1TBSY flag is always set. If the transmission buffer empty flag SC1TEMP is set to "0" as the transmission complete interrupt SC1TIRQ is generated, the SC1TBSY is cleared to "0". If the SC1SBOS flag is set to "0", the SC1TBSY flag is reset to "0".

■ Frame Mode and Parity Check Setup

Figure 11-3-17 shows the data format at UART communication.

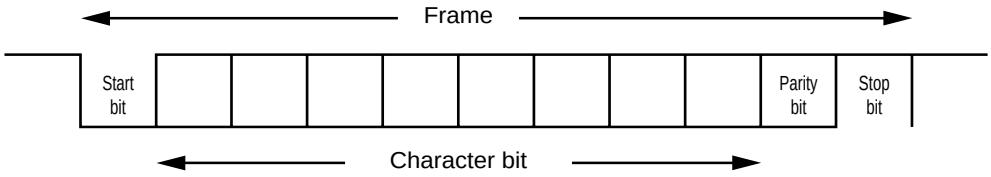


Figure:12.3.17 UART Serial Interface Transmission / Reception Data Format

The transmission / reception data consists of start bit, character bit, parity bit and stop bit. Table:12.3.15 shows its kinds to be set.

Table:12.3.15 UART Serial Interface Transmission / Reception Data

Start bit	1 bit
Character bit	7,8 bit
Parity bit	fixed to 0, fixed to 1, odd, even, none
Stop bit	1,2 bits

The SC1FM1 to 0 flag of the SC1MD2 register sets the frame mode. Table:12.3.16 shows the UART serial interface frame mode settings. If the SC1CMD flag of the SC1MD1 register is set to "1", and UART communication is selected, the transfer bit count on the SC1LNG2 to 0 flag of the SC1MD0 register is no more valid.

Table:12.3.16 UART Serial Interface Frame Mode

SC1MD2 register		Frame mode
SC1FM1	SC1FM0	
0	0	Character bit 7 bits + Stop bit 1 bit
0	1	Character bit 7 bits + Stop bit 2 bits
1	0	Character bit 8 bits + Stop bit 1 bit
1	1	Character bit 8 bits + Stop bit 2 bits

Parity bit is to detect wrong bits with transmission / reception data. Table:12.3.17 shows kinds of parity bit. The SC1NPE, SC1PM1 to 0 flag of the SC1MD2 register set parity bit.

Table:12.3.17 Parity Bit of UART Serial Interface

SC1MD2			Parity bit	Setup
SC1NPE	SC1PM1	SC1PM0		
0	0	0	Fixed to 0	Set parity bit to "0"
0	0	1	Fixed to 1	Set parity bit to "1"
0	1	0	Odd parity	Control that the total of "1" of parity bit and character bit should be odd
0	1	1	Even parity	Control that the total of "1" of parity bit and character bit should be even
1	-	-	None	Do not add parity bit

■ Break Status Transmission Control Setup

The SC1BRKE flag of the SC1MD2 register generates the brake status. If SC1BRKE is set to "1" to select the brake transmission, all bits from start bits to stop bits transfer "0".

■ Reception Error

At reception, there are 3 types of error; overrun error, parity error and framing error. Reception error can be determined by the SC1ORE, SC1PEK, SC1FEF flag of the SC1STR register. Even one of those errors is detected, the SC1ERE flag of the SC1STR register is set to "1". SC1PEK, the SC1FEF flags in reception error flag are renewed at generation of the reception complete interrupt SC1RIRQ. The SC1ORE flag is cleared at the same time of next communication complete interrupt SC1RIRQ generation after the data of the RXBUF1 is read out. The decision of the received error flag should be operated until the next communication is finished. Those error flag has no effect on communication operation. Table:12.3.18 shows the list of reception error source.

Table:12.3.18 Reception Error Source of UART Serial Interface

Flag	Error		
SC1ORE	Overrun error	Next data is received before reading the receive buffer	
SC1PEK	Parity error	at fixed to 0	when parity bit is "1"
		at fixed to 1	When parity bit is "0"
		Odd parity	The total of "1" of parity bit and character bit is even
		Even parity	The total of "1" of parity bit and character bit is odd
SC1FEF	Framing error	Stop bit is not detected	

■ Judgement of Break Status Reception

Reception at break status can be judge. If all received data from start bit and stop bit is "0", the SC1BRKF flag of the SC1MD2 register is set and regards the break status. The SC1BRKF flag is set at generation of the reception complete interrupt SC1RIRQ.

■ Continuous Communication

This serial interface has continuous communication function. If data is set to the transmission data buffer TXBUF1 during communication, the transmission buffer empty flag SC1TEMP is set to continue automatic communication. This does not generate any blank in communication. Set data to TXBUF between previous data setup and generation of the communication complete interrupt SC1TIRQ.

■ Clock Setup

Transfer clock is not necessary for UART communication itself, but necessary for setup of data transmission / reception timing in the serial interface.

Select the timer to be used as a baud rate timer by the SC1MD3 register.

■ Receive Bit Count and First Transfer Bit

In the case of reception, when the transfer bit count is 7 bits, the data storing method to the received data buffer RXBUF1 is different depending on the first transfer bit selection. At MSB first, data are stored to the upper bits of RXBUF1. When there are 7 bits to be transferred, as shown on Table:12.3.18, if data "G" to "A" are stored to bp7 to bp1 of RXBUF1. At LSB first, data are stored to the lower bits of RXBUF1. When there are 7 bits to be transferred, as shown on Table:12.3.19, if data "A" to "G" are stored to bp0 to bp6 of RXBUF1.

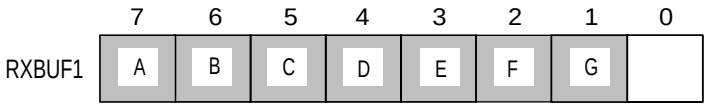


Figure:12.3.18 Transfer Bit Count and First Transfer Bit (starting with MSB)

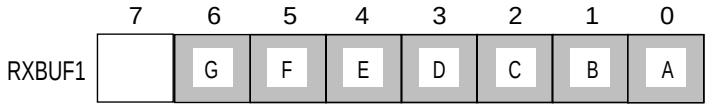


Figure:12.3.19 Transfer Bit Count and First Transfer Bit (starting with LSB)

The following items are the same as clock synchronous serial.

■ First Transfer Bit Setup

Refer to:XII-13

■ Transmission Data Buffer

Refer to:XII-13

■ Received Data Buffer

Refer to:XII13

■ Transfer Bit Count and First Transfer Bit

Refer to:XII-14

■ Transmission Buffer Empty Flag

Refer to:XII-18

■ Emergency Reset

Refer to:XII-19

■ Transmission Timing

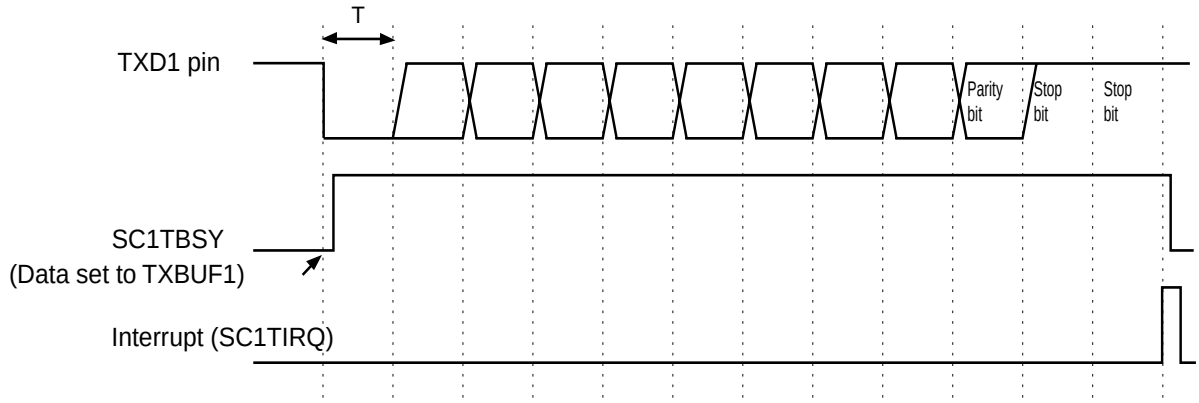


Figure:12.3.20 Transmission Timing (parity bit is enabled)

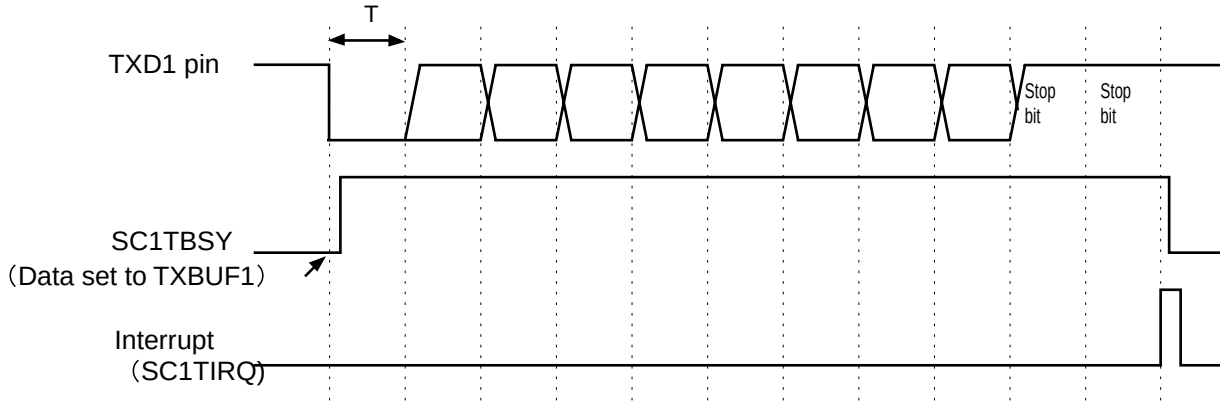


Figure:12.3.21 Transmission Timing (parity bit is disabled)

■ Reception Timing

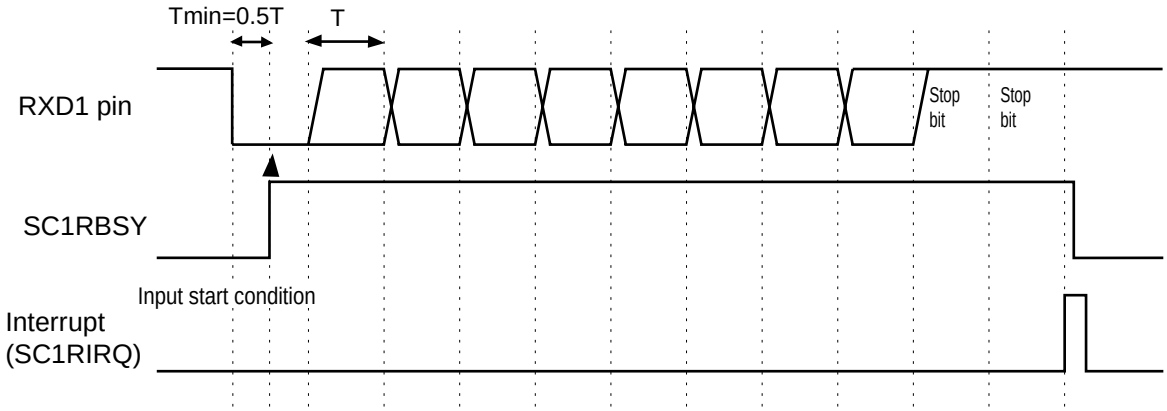


Figure:12.3.22 Reception Timing (parity bit is enabled)

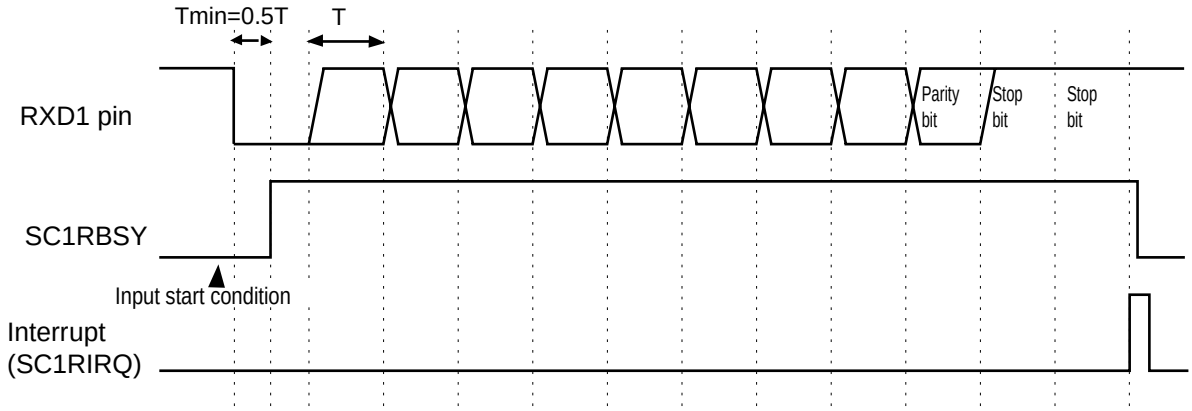


Figure:12.3.23 Reception Timing (parity bit is disabled)

■ Transfer Speed Setup

Baud rate timer (timer 1, timer 2) can set any transfer rate. Table:12.3.19 shows the setup example of the transfer speed.

Table:12.3.19 UART Serial Interface Transfer Speed

Setup	Register	Page
Serial 1 clock source (timer 4 , timer 5)	SC1MD3	XII-10
Timer 4 clock source	TM4MD	V-21
Timer 4 compare register	TM1OC	V-15
Timer 5 clock source	TM5MD	V-22
Timer 5 compare register	TM50C	V-15

Timer compare register is set as follows;

baud rate = 1 / (overflow cycle $\times$ 2 $\times$ 8) ("8" means that clock source is divided by 8)

overflow cycle = (set value of compare register + 1) $\times$ timer clock cycle

therefore,

set value of compare register = timer clock frequency / (baud rate $\times$ 2 $\times$ 8) - 1

For example, if baud rate should be 300 bps at timer clock source fs/4 (fosc = 8 MHz, fs = fosc/2), set value should be as follows;

Set value of compare register = $(8 \times 10^6 / 2 / 4) / (300 \times 2 \times 8) - 1$

= 207

= 0xCF

Timer clock source and the set value of timer compare register at the standard rate are shown in the following page.

Transfer rate should be selected under 300 kbps.

fosc (MHz)	Clock source (Timer)	Transfer Speed (bit/s)									
		300		960		1200		2400		4800	
		Set Value	caluculated value	Set Value	caluculated value	Set Value	caluculated value	Set Value	caluculated value	Set Value	caluculated value
4.00	fosc	-	-	-	-	207	1202	103	2404	51	4808
	fosc/4	207	300	64	962	51	1202	25	2404	12	4808
	fosc/16	51	300	-	-	12	1202	-	-	-	-
	fosc/32	25	300	-	-	-	-	-	-	-	-
	fosc/64	12	300	-	-	-	-	-	-	-	-
	fs/2	207	300	64	962	51	1202	25	2404	12	4808
	fs/4	104	297	-	-	25	1202	12	2404	-	-
4.19	fosc	-	-	-	-	217	1201	108	2403	54	4761
	fosc/4	217	300	67	963	-	-	-	-	-	-
	fosc/16	-	-	16	963	-	-	6	2338	-	-
	fosc/32	-	-	-	-	-	-	-	-	-	-
	fosc/64	-	-	-	-	-	-	-	-	-	-
	fs/2	217	300	67	963	-	-	-	-	-	-
	fs/4	108	300	33	963	-	-	13	2338	-	-
8.00	fosc	-	-	-	-	-	-	207	2404	103	4808
	fosc/4	-	-	129	962	103	1202	51	2404	25	4808
	fosc/16	103	300	-	-	25	1202	12	2404	-	-
	fosc/32	51	300	-	-	12	1202	-	-	-	-
	fosc/64	25	300	-	-	-	-	-	-	-	-
	fs/2	-	-	129	962	103	1202	51	2404	25	4808
	fs/4	207	300	64	962	51	1202	25	2404	12	4808
8.38	fosc	-	-	-	-	-	-	217	2403	108	4805
	fosc/4	-	-	135	963	108	1201	-	-	-	-
	fosc/16	108	300	33	963	-	-	13	2338	-	-
	fosc/32	-	-	16	963	-	-	6	2338	-	-
	fosc/64	-	-	-	-	-	-	-	-	-	-
	fs/2	-	-	135	963	108	1201	-	-	-	-
	fs/4	217	300	67	963	-	-	-	-	-	-
12.00	fosc	-	-	-	-	-	-	-	-	155	4808
	fosc/4	-	-	194	962	155	1202	77	2404	38	4808
	fosc/16	155	300	-	-	38	1202	-	-	-	-
	fosc/32	77	300	-	-	-	-	-	-	-	-
	fosc/64	38	300	-	-	-	-	-	-	-	-
	fs/2	-	-	194	962	155	1202	77	2404	38	4808
	fs/4	-	-	-	-	77	1202	38	2404	-	-
16.00	fosc	-	-	-	-	-	-	-	-	207	4808
	fosc/4	-	-	-	-	207	1202	103	2404	51	4808
	fosc/16	207	300	64	962	51	1202	25	2404	12	4808
	fosc/32	103	300	-	-	25	1202	12	2404	-	-
	fosc/64	51	300	-	-	12	1202	-	-	-	-
	fs/2	-	-	-	-	207	1202	103	2404	51	4808
	fs/4	-	-	129	962	103	1202	51	2404	25	4808

Figure:12.3.24 Setup Value of UART Serial Interface Transfer Speed

		Transfer Speed (bit/s)									
fosc (MHz)	Clock source (Timer)	9600		19200		28800		31250		38400	
		Set Value	caluculated value	Set Value	caluculated value	Set Value	caluculated value	Set Value	caluculated value	Set Value	caluculated value
4.00	fosc	25	9615	12	19231	-	-	7	31250	-	-
	fosc/4	-	-	-	-	-	-	1	31250	-	-
	fosc/16	-	-	-	-	-	-	-	-	-	-
	fosc/32	-	-	-	-	-	-	-	-	-	-
	fosc/64	-	-	-	-	-	-	-	-	-	-
	fs/2	-	-	-	-	-	-	1	31250	-	-
	fs/4	-	-	-	-	-	-	-	-	-	-
4.19	fosc	26	9699	-	-	-	-	-	-	-	-
	fosc/4	-	-	-	-	-	-	-	-	-	-
	fosc/16	-	-	-	-	-	-	-	-	-	-
	fosc/32	-	-	-	-	-	-	-	-	-	-
	fosc/64	-	-	-	-	-	-	-	-	-	-
	fs/2	-	-	-	-	-	-	-	-	-	-
	fs/4	-	-	-	-	-	-	-	-	-	-
8.00	fosc	51	9615	25	19231	-	-	15	31250	12	38462
	fosc/4	12	9615	-	-	-	-	3	31250	-	-
	fosc/16	-	-	-	-	-	-	-	-	-	-
	fosc/32	-	-	-	-	-	-	-	-	-	-
	fosc/64	-	-	-	-	-	-	-	-	-	-
	fs/2	12	9615	-	-	-	-	3	31250	-	-
	fs/4	-	-	-	-	-	-	1	31250	-	-
8.38	fosc	54	9523	26	19398	-	-	-	-	-	-
	fosc/4	-	-	-	-	-	-	-	-	-	-
	fosc/16	-	-	-	-	-	-	-	-	-	-
	fosc/32	-	-	-	-	-	-	-	-	-	-
	fosc/64	-	-	-	-	-	-	-	-	-	-
	fs/2	-	-	-	-	-	-	-	-	-	-
	fs/4	-	-	-	-	-	-	-	-	-	-
12.00	fosc	77	9615	38	19231	25	28846	23	31250	-	-
	fosc/4	-	-	-	-	-	-	5	31250	-	-
	fosc/16	-	-	-	-	-	-	-	-	-	-
	fosc/32	-	-	-	-	-	-	-	-	-	-
	fosc/64	-	-	-	-	-	-	-	-	-	-
	fs/2	-	-	-	-	-	-	5	31250	-	-
	fs/4	-	-	-	-	-	-	2	31250	-	-
16.00	fosc	103	9615	51	19231	-	-	31	31250	25	38462
	fosc/4	25	9615	12	19231	-	-	7	31250	-	-
	fosc/16	-	-	-	-	-	-	-	-	-	-
	fosc/32	-	-	-	-	-	-	-	-	-	-
	fosc/64	-	-	-	-	-	-	-	-	-	-
	fs/2	25	9615	-	-	-	-	7	31250	-	-
	fs/4	12	9615	-	-	-	-	3	31250	-	-

Figure:12.3.25 Setup Value of UART Serial Interface Transfer Speed

■ Pin Setup (with 1,2 channels, at transmission)

Table:12.3.20 shows the pins setup at UART serial interface transmission. The pins setup is common to the TXD1 pin, RXD1 pin, regardless of those pins are independent / connected.

Table:12.3.20 UART Serial Interface Pin Setup (with 1,2 channels, at transmission)

Setup item	Data output pin	Data input pin
	TXD1 pin	RXD1 pin
Port pin	P30	P31
TXD1/RXD1 pins selection	TXD1/RXD1 pins independent/connect	
	SC1MD1(SC1IOM)	
Function	Serial data output	"1" output
	SC1MD1(SC1SBOS)	SC1MD1(SC1SBIS)
Style	Push-pull/ Nch open-drain	-
	P3ODC(P3ODC0)	
I/O	Output mode	-
	P3DIR(P3DIR0)	
Pull-up setup	Added / not added	-
	P3PLU(P3PLU0)	

■ Pin Setup (with 2 channels, at reception)

Table:12.3.21 shows the pins setup at UART serial interface reception with 2 channels (TXD1 pin, RXD1pin).

Table:12.3.21 UART Serial Interface Pin Setup (with 2 channels, at reception)

Setup item	Data output pin	Data input pin
	TXD1 pin	RXD1 pin
Port pin	P30	P31
TXD1/RXD1 pins selection	TXD1/RXD1 pins independent	
	SC1MD1(SC1IOM)	
Function	Port	Serial data input
	SC1MD1(SC1SBOS)	SC1MD1(SC1SBIS)
Style	-	-
I/O	-	Input mode
	-	P3DIR(P3DIR1)
Pull-up setup	-	-

■ Pin Setup (with 1 channel, at reception)

Table:12.3.22 shows the pin setup at UART serial interface reception with 1 channel (TXD1 pin). The RXD1 pin in not used, so can be used as a port.

Table:12.3.22 UART Serial Interface Pin Setup (with 1 channel, at reception)

Setup item	Data output pin	Data input pin
	TXD1 pin	RXD1 pin
Port pin	P30	P31
TXD1/RXD1 pins selection	TXD1/RXD1 pins connect	
	SC1MD1(SC1IOM)	
Function	Port	Serial data input
	SC1MD1(SC1SBOS)	SC1MD1(SC1SBIS)
Style	-	-
I/O	-	Input mode
	-	P3DIR(P3DIR1)
Pull-up setup	-	-

■ Pin Setup (with 2 channels, at transmission / reception)

Table:12.3.23 shows the pin setup at UART serial interface transmission / reception with 2 channels (TXD1 pin, RXD1 pin).

Table:12.3.23 UART Serial Interface Pin Setup (with 2 channels, at transmission / reception)

Setup item	Data output pin	Data input pin
	TXD1 pin	RXD1 pin
Port pin	P30	P31
TXD1/RXD1 pins selection	TXD1/RXD1 pins independent	
	SC1MD1(SC1IOM)	
Function	Serial data output	Serial data input
	SC1MD1(SC1SBOS)	SC1MD1(SC1SBIS)
Style	Push-pull/ Nch open-drain	-
	P3ODC(P3ODC0)	
I/O	Output mode	Input mode
	P3DIR(P3DIR0)	P3DIR(P3DIR1)
Pull-up setup	Added / not added	-
	P3PLU(P3PLU0)	

12.3.4 Setup Example

■ Transmission / Reception Setup

The setup example at UART transmission / reception with serial 1 is shown. Table:12.3.24 shows the condition at transmission / reception.

Table:12.3.24 UART Interface Transmission Reception Setup

Setup item	SEt to
TXD1/RXD1 pin	Independent (with 2 channels)
Frame mode specification	8 bits + 2 stop bits
First transfer bit	MSB
Clock source	Timer 5
TXD1/RXD1 pin type	Nch open-drain
Pull-up resistor of TXD1 pin	Added
Parity bit add/check	"0" added/check
Serial 1 transmission complete interrupt	Enable
Serial 1 reception complete interrupt	Enable

An example setup procedure, with a description of each step is shown below.

Setup Procedure	Description
(1) Set the baud rate timer	(1) Set the baud rate timer by the TM5MD register, the TM5OC register. Set the TM5EN flag to "1" to start timer 5. [Chapter 5. 5.9 Serial Transfer Clock Output Operation]
(2) Select the clock source SC1MD3(0x03FA0) bp2-0 :SC1PSC2-0 =110	(2) Set the bp3 to 0 flag of the SC1MD3 register to "111" to select Timer 5 output as a clock source.
(3) Control the pin style P3ODC(0x03F2C) bp0 :P3ODC0 =1 P3PLU(0x03F33) bp0 :P3PLU0 =1	(3) Set the P3ODC0 flag of the P3ODC register to "1" to select Nch open-drain for the TXD1 pin. P3PLU0 flag of the P3PLU register to "1" to add pull-up register.
(4) Control the pin direction P3DIR(0x03F43) bp1-0 :P3DIR1-0 =0, 1	(4) Set the P3DIR0 flag of the Port 3 pin direction control register (P3DIR) to "1" and the P3DIR3 flag to "0" to set P30 to the output mode, P31 to the input mode.

Setup Procedure	Description
(5) Set the SC1MD0 register Select the start condition SC1MD0(0x03F9D) bp3 :SC1STE =1	(5) Set the SC1STE flag of the SC1MD0 register to "1" to enable start condition.
Select the first bit to be transferred SC1MD0(0x03F9D) bp4 :SC1DIR =0	Set the SC1DIR flag of the SC1MD0 register to "0" to select MSB as first transfer bit.
(6) Set the SC1MD2 register Control the output data SC1MD2(0x03F9F) bp0 :SC1BRKE =0	(6) Set the SC1BRKE flag of the SC1MD2 register to "0" to select the serial data transmission.
Select the added parity bit SC1MD2(0x03F9F) bp3 :SC1NPE =0 bp5-4 :SC1PM1-0 =00	Set the SC1PM1 to 0 flag of the SC1MD2 register to "00" to select 0 parity, and set the SC1NPE flag to "0" to enable add parity bit.
Specify the flame mode SC1MD2(0x03F9F) bp7-6 :SC1FM1-0 =11	Set the SC1FM1 to 0 flag of the SC1MD2 register to "11" to select 8 bits + 2 stop bits at the flame mode.
(7) Set the SC1MD1 register Select the communication type SC1MD1(0x03F9E) bp0 :SC1CMD =1	(7) Set the SC1CMD flag of the SC1MD1 register to "1" to select full duplex UART.
Select the clock frequency SC1MD1(0x03F9E) bp3 :SC1CKM =1 bp2 :SC1MST =1	Set the SC1CKM flag of the SC1MD1 register to "1" to select "divided by 8" at source clock. And, the SC1MST flag should be always set to "1" to select clock master.
Control the pin function SC1MD1(0x03F9E) bp4 :SC1SBOS =1 bp5 :SC1SBIS =1 bp7 :SC1IOM =0	Set the SC1SBOS, SC1SBIS, SC1IOM flag of the SC1MD1 register to "1" to set the RXD1 pin to serial data output and the RXD1 pin to serial data input.
(8) Enable the interrupt SC1RICR(0x03FF4) bp1 :SC1RIE =1 SC1TICR(0x03FF5) bp1 :SC1TIE =1	(8) Set the SC1RIE flag of the SC1RICR register to "1", and SC1TIE flag of the SC1TICR register to "1" to enable the interrupt request. If any the interrupt request already set, clear them.
(9) Start the serial transmission The transmission → TXBUF1(0x03FA3) The reception data → input to RXD1	(9) The transmission is started by setting the transmission data to the serial transmission data buffer (TXBUF1). When the transmission is finished, the serial 1 transmission interrupt (SC1TIRQ) is generated. Also, after the received data is stored to the RXBUF1, the serial 1 reception interrupt (SC1RIRQ) is generated.

Note:(6), (7), (8) can be set at the same time.

When the TXD1 / RXD1 pin are connected for communication with 1 channel, the TXD1 pin inputs / outputs serial data. The port direction control register P3DIR switches I/O. At reception, set SC1SBIOS of the SC1MD1 register to "1" to select serial data input. The RXD1 pin can be used as a general port.

This serial interface contains emergency reset function. If communication need to be stopped by force, set SC1SBOS and SC1SBIS of the SC1MD1 register to "0".

Each flag should be set as the setup procedure in order. Activation of communication should be operated after all control registers (refer to Table:12.2.1 TXBUF1, RXBUF1) are set.

Timer 4 and timer 5 can be used as a baud rate timer. Refer to Chapter 6. 6.8 Serial Transfer Clock Output Operation.

Chapter 13 Serial Interface 2

13

13.1 Overview

This LSI contains a serial interface 2 that is capable of both clock synchronous / IIC (single master) serial communication.

13.1.1 Functions

Table:13.1.1 shows the serial interface 2 functions.

Table:13.1.1 Serial Interface 2 Functions

Communication style	Clock synchronous	IIC (single master)
Interrupt	SC2IRQ	SC2IRQ
Pins	SBO2,SBI2,SBT2	SDA2,SCL2
3 channels type	O	-
2 channels type	O (SBO2,SBT2)	O
Transfer bit count	1 to 8 bit	1 to 8 bit
Start condition	O	O
First transfer bit	O	O
Input edge / Output edge	O	-
SBO2 output control after transfer of last data	H/L/ last data hold	-
Function in STANDBY mode	Slave reception only	-
ACK bit	-	O
ACK bit level	-	O
Continuous operation (with ATC1)	O	-
Clock sources	fosc/2 fosc/4 fosc/16 fosc/32 fs/2 fs/4 external clock timer 2 output timer 3 output	fosc/2 fosc/4 fosc/16 fosc/32 fs/2 fs/4 timer 2 output timer 3 output
Maximum transfer rate	5.0 MHz	NORMAL mode: 100 kHz High speed mode: 400 kHz
fosc : machine clock (for high speed ocillation) fs : system clock In IIC communication, transfer clock is obtained by dividing the clock source by 8.		

Transfer rate should be set slower than system clock (fs).

13.1.2 Block Diagram

■ Serial Interface 2 Block Diagram

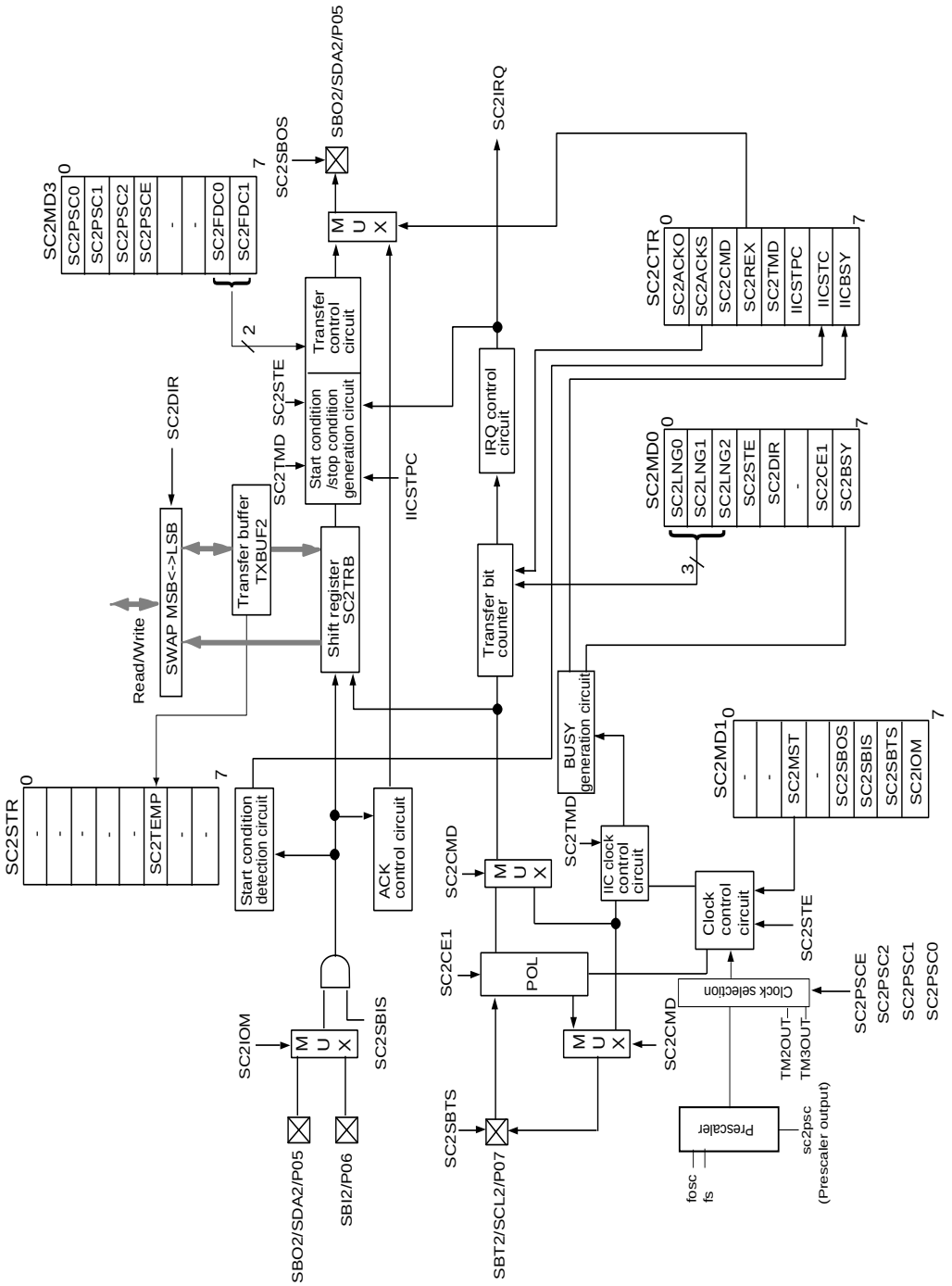


Figure:13.1.1 Serial Interface 2 Block Diagram

13.2 Control Registers

13.2.1 Registers List

Table:13.2.1 shows the registers that control serial interface 2.

Table:13.2.1 Serial Interface 2 Control Registers List

Register	Address	R/W	Function	Page
SC2MD0	0x03F96	R/W	Serial interface 2 mode register 0	XIII-7
SC2MD1	0x03F97	R/W	Serial interface 2 mode register 1	XIII-8
SC2MD3	0x03F98	R/W	Serial interface 2 mode register 3	XIII-9
SC2STR	0x03F99	R	Serial interface 2 status register	XIII-10
SC2TRB	0x03F9A	R	Serial interface 2 transmission/reception shift register	XIII-6
TXBUF2	0x03F9B	R/W	Serial interface 2 transmission data buffer	XIII-6
SC2CTR	0x03F9C	R/W	Serial interface 2 control register	XIII-11
P0ODC	0x03F1C	R/W	Port 0 N-ch open drain control register	IV-28
P0DIR	0x03F30	R/W	Port 0 direction control register	IV-28
P0PLU	0x03F40	R/W	Port 0 pull-up control register	IV-28
SC2ICR	0x03FF6	R/W	Serial interface 2 interrupt control register	III-33
SCCKSEL	0x03F8E	R/W	Serial interface Clock Cycle Switching Register	XIII-13

R /W : Readable / Writable

R : Readable

13.2.2 Data Buffer Register

Serial interface 2 has a 8-bit serial data buffer register for transmission.

■ Serial Interface 2 Transmission Data Buffer (TXBUF2: 0x03F9B)

bp	7	6	5	4	3	2	1	0
Flag	TXBUF27	TXBUF26	TXBUF25	TXBUF24	TXBUF23	TXBUF22	TXBUF21	TXBUF20
At reset	X	X	X	X	X	X	X	X
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

13.2.3 Data Register

Serial interface 2 has a 8-bit serial data register.

■ Serial Interface 2 Transmission / Reception Shift Register (SC2TRB: 0x03F9A)

bp	7	6	5	4	3	2	1	0
Flag	SC2TRB7	SC2TRB6	SC2TRB5	SC2TRB4	SC2TRB3	SC2TRB2	SC2TRB1	SC2TRB0
At reset	X	X	X	X	X	X	X	X
Access	R	R	R	R	R	R	R	R

13.2.4 Serial interface 2 Mode Register

■ Serial Interface 2 Mode Register 0 (SC2MD0: 0x03F96)

bp	7	6	5	4	3	2	1	0
Flag	SC2BSY	SC2CE1	-	SC2DIR	SC2STE	SC2LNG2	SC2LNG1	SC2LNG0
At reset	0	0	-	0	0	1	1	1
Access	R	R/W	-	R/W	R/W	R/W	R/W	R/W

bp	Flag	Description
7	SC2BSY	Serial bus status in clock synchronous communication 0: Other use 1: Serial transmission is in progress
6	SC2CE1	Transmission data output edge Reception data input edge 0: Falling Rising 1: Rising Falling
5	-	-
4	SC2DIR	First bit to be transferred 0: MSB first 1: LSB first
3	SC2STE	Start condition 0: Disable start condition 1: Enable start condition
2-0	SC2LNG2 SC2LNG1 SC2LNG0	Transfer bit count 000: 1 bit 001: 2 bit 010: 3 bit 011: 4 bit 100: 5 bit 101: 6 bit 110: 7 bit 111: 8 bit

■ Serial interface 2 Mode Register 1 (SC2MD1: 0x03F97)

bp	7	6	5	4	3	2	1	0
Flag	SC2IOM	SC2SBTS	SC2SBIS	SC2SBOS	-	SC2MST	-	-
At reset	0	0	0	0	-	0	-	-
Access	R/W	R/W	R/W	R/W	-	R/W	-	-

bp	Flag	Description
7	SC2IOM	Serial data input selection 0: Data input from SBI2 1: Data input from SBO2 (SDA2)
6	SC2SBTS	SBT2 pin function 0: Port 1: Transfer clock input / output
5	SC2SBIS	Serial input control 0: "1" input 1: Serial data input
4	SC2SBOS	SBO2(SDA2) pin function 0: Port 1: Serial data output
3	-	-
2	SC2MST	Clock master / slave selection 0: Slave 1: Master
1-0	-	-

■ Serial interface 2 Mode Register 3 (SC2MD03: 0x03F98)

bp	7	6	5	4	3	2	1	0
Flag	SC2FDC1	SC2FDC0	-	-	SC2PSCE	SC2PSC2	SC2PSC1	SC2PSC0
At reset	0	0	-	-	0	0	0	0
Access	R/W	R/W	-	-	R/W	R/W	R/W	R/W

bp	Flag	Description
7-6	SC2FDC1 SC2FDC0	SBO2 output selection after transfer of last data 00: Fixed to "1"(High) output 01: Hold last data 10: Fixed to "0"(Low) output 11: Reserved
5-4	-	-
3	SC2PSCE	Prescaler count control 0: Disable the count 1: Enable the count
2-0	SC2PSC2 SC2PSC1 SC2PSC0	Clock selection 000: fosc/2 (fosc/4, fosc/8)* 001: fosc/4 (fosc/8, fosc/16)* 010: fosc/16 (fosc/32, fosc/64)* 011: fosc/32 (fosc/64, fosc/128)* 100: fs/2 101: fs/4 110: timer 2 output 111: timer 3 output

* This depends on SCCKSEL5 flag and SCCKSEL4 flag of SCCKSEL register.
(refer to table 13.2.9 serial clock cycle switching control register)

■ Serial interface 2 Status Register (SC2STR: 0x03F99)

bp	7	6	5	4	3	2	1	0
Flag	-	-	SC2TEMP	-	-	-	-	-
At reset	-	-	0	-	-	-	-	-
Access	-	-	R	-	-	-	-	-

bp	Flag	Description
7-6	-	-
5	SC2TEMP	Transfer buffer empty flag 0: Empty 1: Full
4-0	-	-

■ Serial interface 2 Control Register (SC2CTR: 0x03F9C)

bp	7	6	5	4	3	2	1	0
Flag	IICBSY	IICSTC	IICSTPC	SC2TMD	SC2REX	SC2CMD	SC2ACKS	SC2ACK0
At reset	0	0	0	0	0	0	0	0
Access	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bp	Flag	Description
7	IICBSY	Serial bus status in IIC communication 0: Other use 1: Serial transmission is in progress
6	IICSTC	Start condition *1 0: Disable start condition 1: Enable start condition
5	IICSTPC	Stop condition detection flag in IIC communication *2 0: undetected 1: detected
4	SC2TMD	Communication mode 0: NORMAL mode 1: High-speed mode
3	SC2REX	Transmission / reception mode selection 0: Transmission 1: Reception
2	SC2CMD	Synchronous / IIC selection 0: Synchronous 1: IIC
1	SC2ACKS	ACK bit enable 0: Enable 1: Disable
0	SC2ACK0	ACK bit level selection *3 0: L level 1: H level

*1: “1“ is not writable.

*2: This is not writable when the emergency reset of communication is not cancelled.

*3: The written data is not readable before generation of the IIC communication.

■ Serial interface Clock Cycle Switching Register (SCCKSEL)

bp	7	6	5	4	3	2	1	0
Flag	SCCKSEL 7	SCCKSEL 6	SCCKSEL 5	SCCKSEL 4	-	-	-	-
At reset	0	0	0	0	-	-	-	-
Access	R/W	R/W	R/W	R/W	-	-	-	-

bp	Flag	Description
7-6	SCCKSEL7 SCCKSEL6	Serial 3 clock (fosc) cycle switching 00: fosc 01: fosc/2 10: fosc/4 11: Reserved
5-4	SCCKSEL5 SCCKSEL4	Serial 2 clock (fosc) cycle switching 00: fosc 01: fosc/2 10: fosc/4 11: Reserved
3-0	-	-

Table:13.2.2 Serial 2 clock (fosc) selection

SCCKSEL(bp5)	SCCKSEL(bp5)	SC3PSC2	SC3PSC1	SC3PSC0	
0	0	0	0	0	fosc/2
0	0	0	0	1	fosc/4
0	0	0	1	0	fosc/16
0	0	0	1	1	fosc/32
0	1	0	0	0	fosc/4
0	1	0	0	1	fosc/8
0	1	0	1	0	fosc/32
0	1	0	1	1	fosc/64
1	0	0	0	0	fosc/8
1	0	0	0	1	fosc/16
1	0	0	1	0	fosc/64
1	0	0	1	1	fosc/128

13.3 Operation

Serial interface 2 is used as both clock synchronous /single master IIC serial interface.

13.3.1 Clock Synchronous Serial Interface

■ Activation Factor for Communication

Table:13.3.1 shows the activation source for communication. At master, a transfer clock is generated by setting data to the transfer data buffer TXBUF2, or by enabling start condition. Signals input from SBT2 pin inside serial interface are masked to prevent operating errors by noise, except during communication. This mask is automatically released by setting data to TXBUF2 (access to the TXBUF2 register), or enabling start condition to the data input pin. Therefore, at slave communication, set data to TXBUF2 or input start condition before input external clock.

Wait more than 3.5 transfer clocks before input the external clock after the data set to TXBUF2. This wait time is used for data loading from TXBUF2 to internal shift register.

Table:13.3.1 Synchronous Serial Interface Activation Source

	Activation source	
	Transmission	Reception
Master communication	Set the transmission data	Set dummy data
		Input start condition
Slave communication	Input clock after the transmission data is set	Input clock after dummy data is set
		Input clock after start condition is input

■ Transfer Bit Count Setup

The transfer bit count can be selected from 1 bit to 8 bits. Set the SC2LNG 2 to 0 flag of the SC2MD0 register (at reset : 111). The SC2LNG 2 to 0 flag holds the previous value until other value is set.

The SBT2 pin is masked inside serial interface to prevent operating errors by noise, except during communication. At slave, set data to SC2TRB or input start condition before input clock to the TXBUF2 pin.

Wait more than 3.5 transfer clocks before input the external clock after the data set to TXBUF2. Otherwise, normal operation is not guaranteed.

■ Start Condition Setup

Enable or disable of start condition can be selected with the SC2STE flag of the SC2MD0 register.

Start condition is detected when the SC2CE1 flag of the SC2MD0 register is set to "0" and data line SBI2 pin (3 channels) or SBO2 pin (2 channels) changes from "H" to "L" while the clock line (SBT2 pin) is "H". It is also detected when the SC2CE1 flag of the SC2MD0 register is set to "1" and data line SBI2 pin (3 channels) or SBO2 pin (2 channels) changes from "H" to "L" while the clock line (SBT2 pin) is "L".

At the selection of the start condition "enable" and master transmission / reception, after the start condition output, start condition is input from the slave, then data transmission is generated.

■ First Transfer Bit Setup

The SC2DIR flag of the SC2MD0 register sets the first bit to be transferred. LSB or MSB can be selected.

■ Transmission / Reception Data Buffer

The transfer data buffer TXBUF2 is the spare buffer which stores data to be loaded to internal shift register. Set the data to be transferred to transfer data buffer TXBUF2, and the data is automatically loaded to internal shift register. The data loading takes more than 3.5 clock cycles. Data setting to TXBUF2 again during data loading may not be operated properly. You can determine whether or not data loanding is in progress by monitoring transfer buffer empty flag SC2TEMP of the SC2STR. SC2TEMP flag is set to "1"when data is set to TXBUF2 and cleared to "0" when data loading ends.

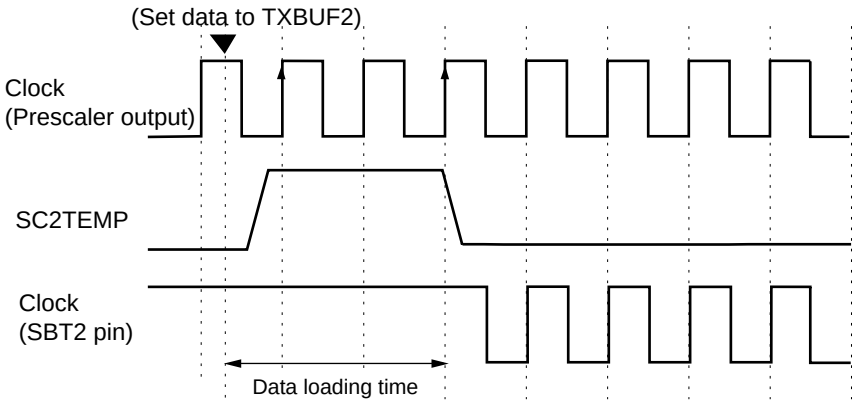


Figure:13.3.1

■ Reception Data Buffer

Use transmission / reception shift register SC2TRB as reception data buffer. The received data is stored to SC2TRB shifting by 1 bit.

If start condition is input for activation during communication again, the transmission data becomes invalid. To transmit the data, set it to TXBUF2 again.

SC2TRB is overwritten in every communication. In sequence reception, read out the data in SC2TRB before the next reception is started.

■ Transmission Bit Count and First Transfer Bit

When the transfer bit count is 1 to 7 bits, data storage to the transmission /reception shift register TXBUF2 depends on the first transfer bit. When MSB is the first bit to be transferred, the lower bits of TXBUF2 are used for storage. In Figure:13.3.2, if data "A" to "F" are stored to bp2 to bp7 of SC2TRB as the transfer bit count is 6 bits, data is transferred from "F" to "A". When LSB is the first bit to be transferred, use the lower bits of TXBUF2 for storage. In Figure:13.3.3, if data "A" to "F" are stored to bp0 to bp5 of TXBUF2, as the transfer bit count is 6 bits, data is transferred from "A" to "F".

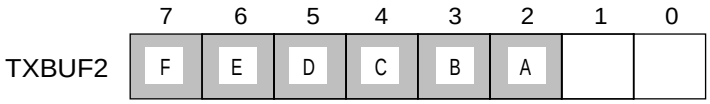


Figure:13.3.2 Transfer Bit Count and First Transfer Bit (MSB First)

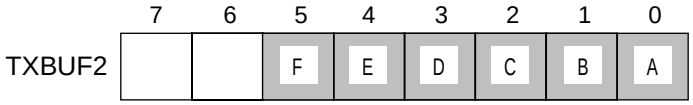


Figure:13.3.3 Transfer Bit Count and First Transfer Bit (LSB First)

■ Receive Bit Count and First Transfer Bit

When the transfer bit count is 1 to 7 bits, data storage to the transmit/receive shift register SC2TRB depends on the first transfer bit. When MSB is the first bit to be transferred, the lower bits of SC2TRB are used for storage. In Figure:13.3.4, as the transfer bit count is 6 bits, data "A" to "F" are stored to bp5 to bp0 of SC2TRB, and they are transferred from "F" to "A". When LSB is the first bit to be transferred, use the upper bits of SC2TRB for storage. In Figure:13.3.5, data "A" to "F" are stored to bp2 to bp7 of SC2TRB, as the transfer bit count is 6 bits, and they are transferred from "A" to "F".

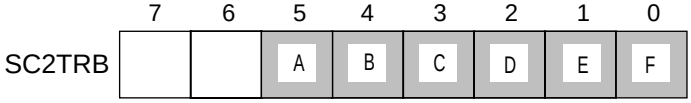


Figure:13.3.4 Receive Bit Count and First Transfer Bit (MSB First)

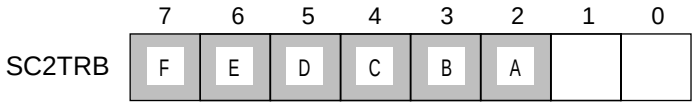


Figure:13.3.5 Receive Bit Count and First Transfer Bit (LSB First)

When the serial transfer bit is set between 1 to 7, the data except for received data of the specified transfer bit count is unknown. Use the received data after being masked by AND/ OR instruction.

■ Continuous Mode

Serial interface 2 is capable of continuous transmission. If data is set to transmission data buffer TXBUF2 during transmission, transmission buffer empty flag SC2TEMP is set and the set data is automatically transmit. Set data to TXBUF2 in the period that after data is loaded to internal shift register and before communication end interrupt SC2IRQ is generated. In master communication, communication blank from SC2IRQ generation to next transfer clock output is 4 transfer clock.

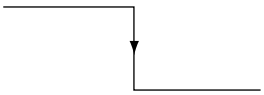
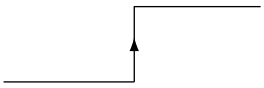
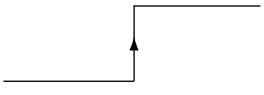
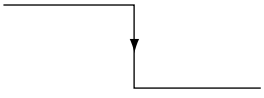
■ Automatic Continuous Transfer by ATC

ATC1, the automatic data transfer function built-in this LSI can activate Serial interface 2. It enables continuous transfer of data up to 255 byte. For activation using ATC1, refer to chapter 18 Automatic Transfer Controller, Transfer mode 8 to 9.

■ Input edge / output edge Setup

The SC2CE1 flag of the SC2MD0 register sets the output edge of the transmission data and the input edge of the received data. Data at transmission is output at the falling edge of clock as the SC2CE1 flag = "0", and at the rising edge of clock as the SC2CE1 = "1". Data at reception is input at the rising edge of clock as the SC2CE1 = "0", and at the falling edge of clock as the SC2CE1 flag = "1"

Table:13.3.2 Input Edge / Output Edge of Transmission and Reception Data

SC2CE1	Transmission data output edge	Received data input edge
0		
1		

■ Clock Setup

Clock source is selected from the dedicated prescaler and timers 2, 3 output (2 channels) with the SC2PSC2 to 0 of the SC2MD3 register. The dedicated prescaler is started by selecting "count enable" with the SC2PSCE of the SC2MD3 register. The SC2MST flag of the SC2MD1 register selects the internal clock (clock master), or the external clock (clock slave). Even if the external clock is selected, set the internal clock with same frequency to the external clock with the SC2MD3 register, as the interrupt flag SC2IRQ is generated by the internal clock. Table:13.3.3 shows the internal clock source which can be set with the SC2MD3 register.

Table:13.3.3 Synchronous Serial Interface Inside Clock Source

	Serial 2
Clock source (Internal clock)	fosc/2
	fosc/4
	fosc/8
	fosc/16
	fosc/32
	fosc/64
	fosc/128
	fs/2
	fs/4
	timer 2 output
	timer 3 output

Set "0" to the SC2SBIS and SC2SBOS flags of the SC2MD register before change the clock setup.

Set transfer clock frequency in slave reception in which start condition is to be smaller than that of the system clock.

■ Data Input Pin Setup

There are 2 communication modes to be selected : 3 channels (clock pin(SBT2 pin), data output pin (SBO2 pin), data input pin (SBI2 pin)), 2 channels (clock pin (SBT2 pin), data I/O pin (SBO2 pin)). The SBI2 pin can be used only for serial data input. The SBO2 pin can be used for serial data input and output. The SC2IOM flag of the SC2MD1 register selects either serial data is input from the SBI2 pin, or the SBO2 pin. When "data input from the SBO2 pin" is selected for communication with 2 channels, the P0DIR3 flag of the P0DIR register is used to switch the transmission / reception of the SBO2 pin. The SBI2 pin, not used at that time, can be used as a general port.

Maximum transfer speed should be under 5.0 MHz. If transfer clock exceeds 5.0 MHz, data may not be transferred properly.

In reception, you can use SBI2 pin as general port by setting SC2IOM of the SC2MD1 register to "1" to select "serial data input from SBO2 pin".

■ Transmission Buffer Empty Flag

If any data is set to TXBUF2 during communication (after setting data to TXBUF2 before generating the communication complete interrupt SC2IRQ), the transmission buffer empty flag SC2TEMP of the SC2STR register is set to "1". That indicates that the next transmission data is going to be loaded. Data is loaded to inside shift register from TXBUF2 by generation of SC2TIRQ, and the next transfer is started as SC2TEMP is cleared to "0".

■ BUSY flag

If data is set to the transmission/reception shift register TXBUF2, or start condition is enabled, the busy flag SC2BSY is set. That is cleared to "0" by the generation of the communication end interrupt SC2IRQ. The SC2BSY flag setup is maintained during continuous communication. If transmission buffer empty flag SC2TEMP is "0" when communication end interrupt SC2IRQ is generated, SC2BSY is cleared to "0".

■ Forced Reset

You can shut down the communication by setting both of the SC2SBOS flag and the SC2SBIS flag of the SC2MD1 register to "0" (the SBO2 pin function : port, input data : input "1"). When a forced reset is done, the status register (all flag of the SC2STR register) and SC2BSY flag of the SC2MD0 register are cleared, but other control registers hold their set values.

■ Last Bit of Transmission Data

Table:13.3.4 shows last bit data output holding time at transmission, and the minimum data input time of the last bit at reception. At slave, internal clock setup is necessary to reserve data holding time at data transmission.

Table:13.3.4 Last Bit Data Length of Transmission Data

	at transmission Last bit data holding period	at reception Last bit data input period
At master	1 bit data length	1 bit data length (min)
At slave	[1 bit data length of external clock × 1/2]+ [internal clock cycle × (1/2 to 3/2)]	

When start condition is disabled (SC2STE flag=0), SBO2 output after last bit data output hold time can be set with SC2FDC1-0 of the SC2MD3 register as shown in Table:13.3.5.

After reset release, output before serial transfer is "H" regardless of the set value of SC2FDC1-0 flags. When start condition is enabled (SC2STE flag =1), "H" is output regardless of the set value of SC2FDC1-0 flags.

Table:13.3.5 SBO2 Output after Last Bit Data Output Hold Time (without start condition)

SC2FDC1 flag	SC2FDC0 flag	SBO2 output after last bit data output hold time
0	0	Fixed to "1"(High) output
1	0	Fixed to "0"(Low) output
0	1	Hold last data
1	1	Reserved

■ Transmission Timing

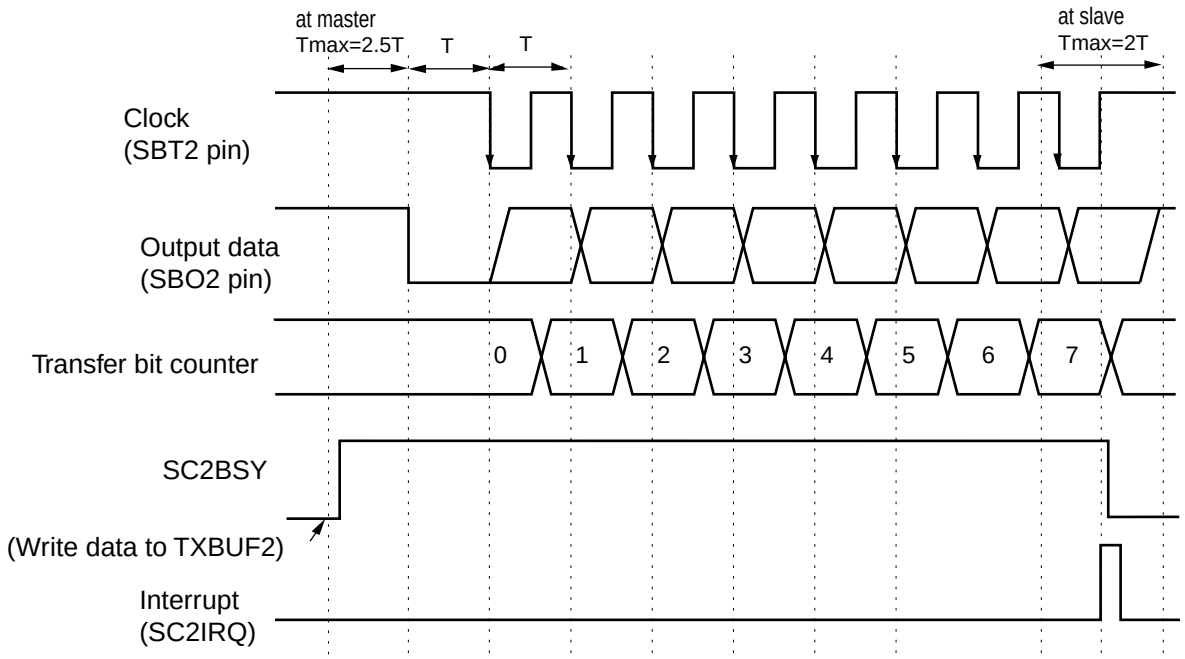


Figure:13.3.6 Transmission Timing (Falling edge, Start condition is enabled)

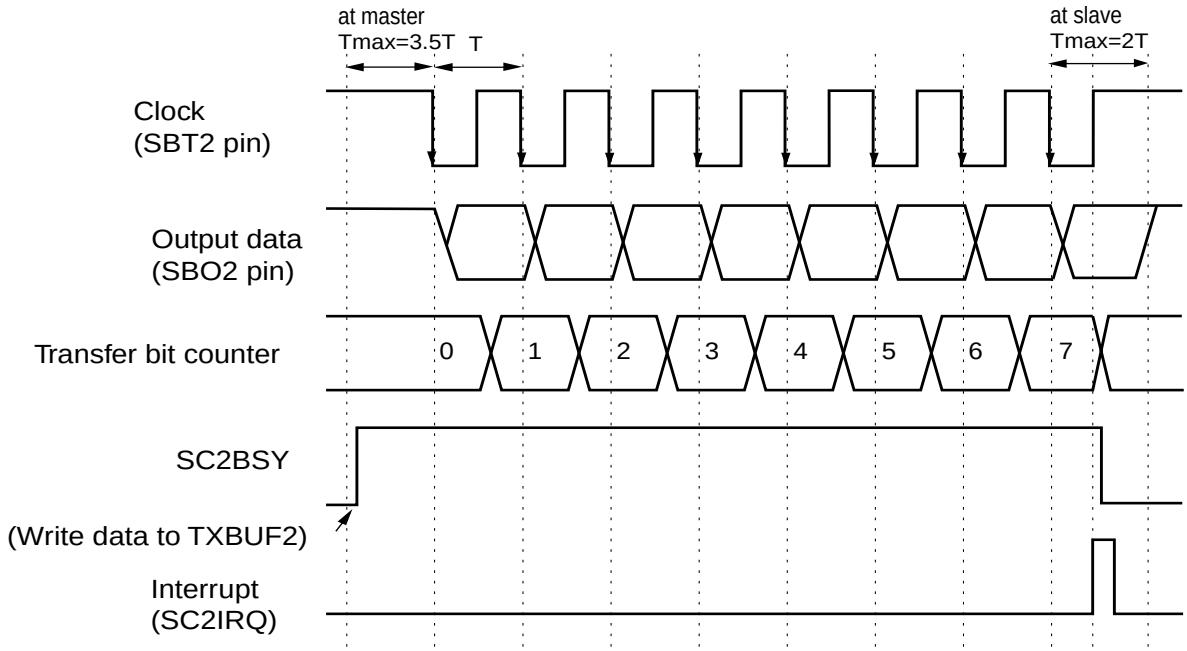


Figure:13.3.7 Transmission Timing (Falling edge, Start condition is disabled)

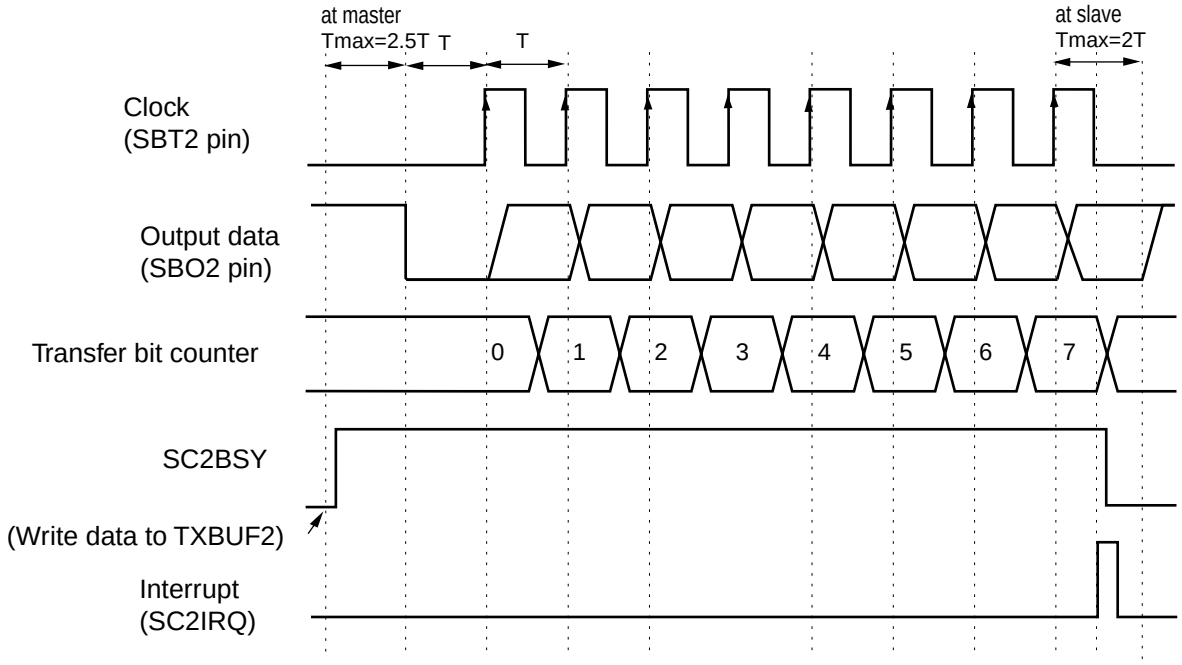


Figure:13.3.8 Transmission Timing (Rising edge, Start condition is enabled)

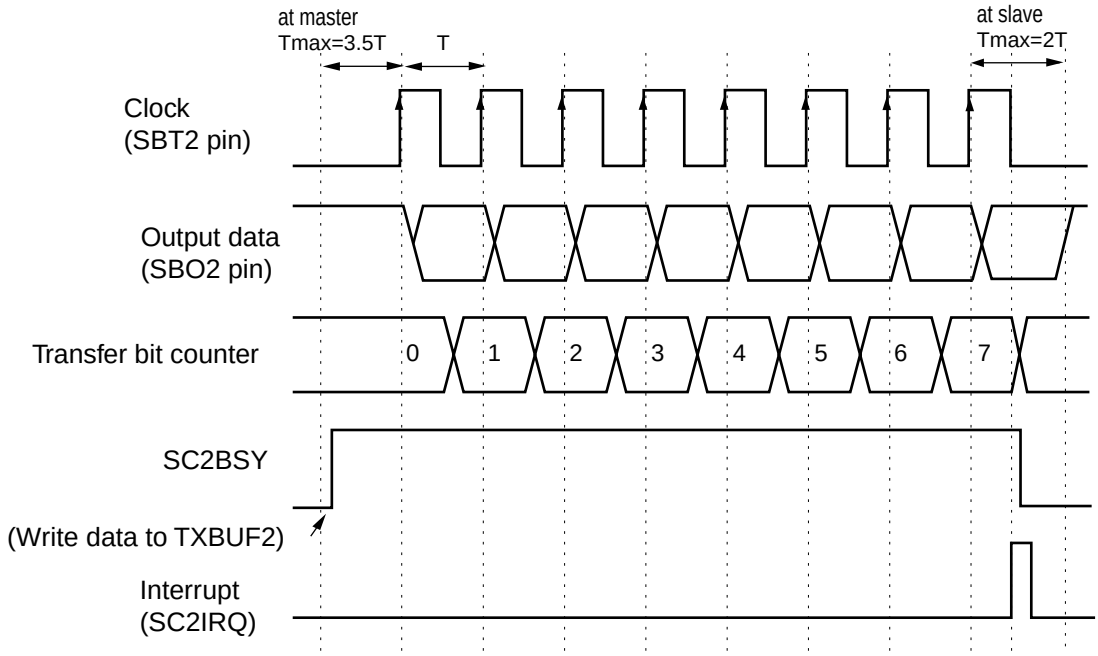


Figure:13.3.9 Transmission Timing (Rising edge, Start condition is disabled)

■ Reception Timing

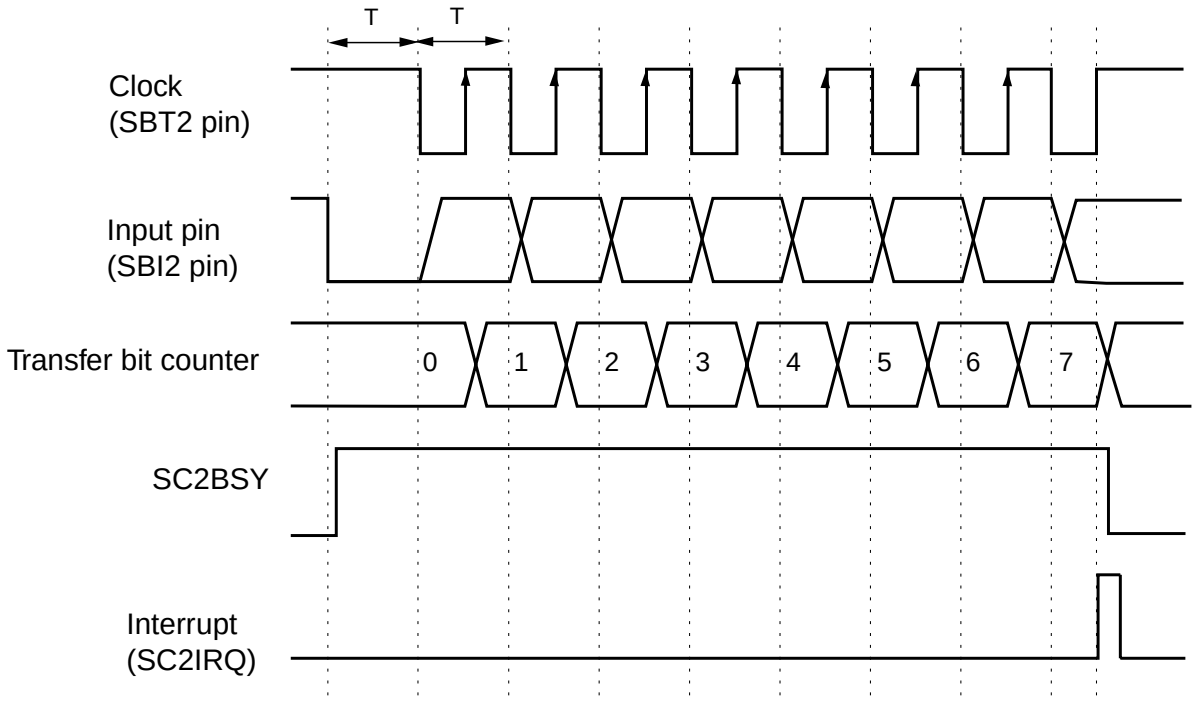


Figure:13.3.10 Reception Timing (Rising edge, Start condition is enabled)

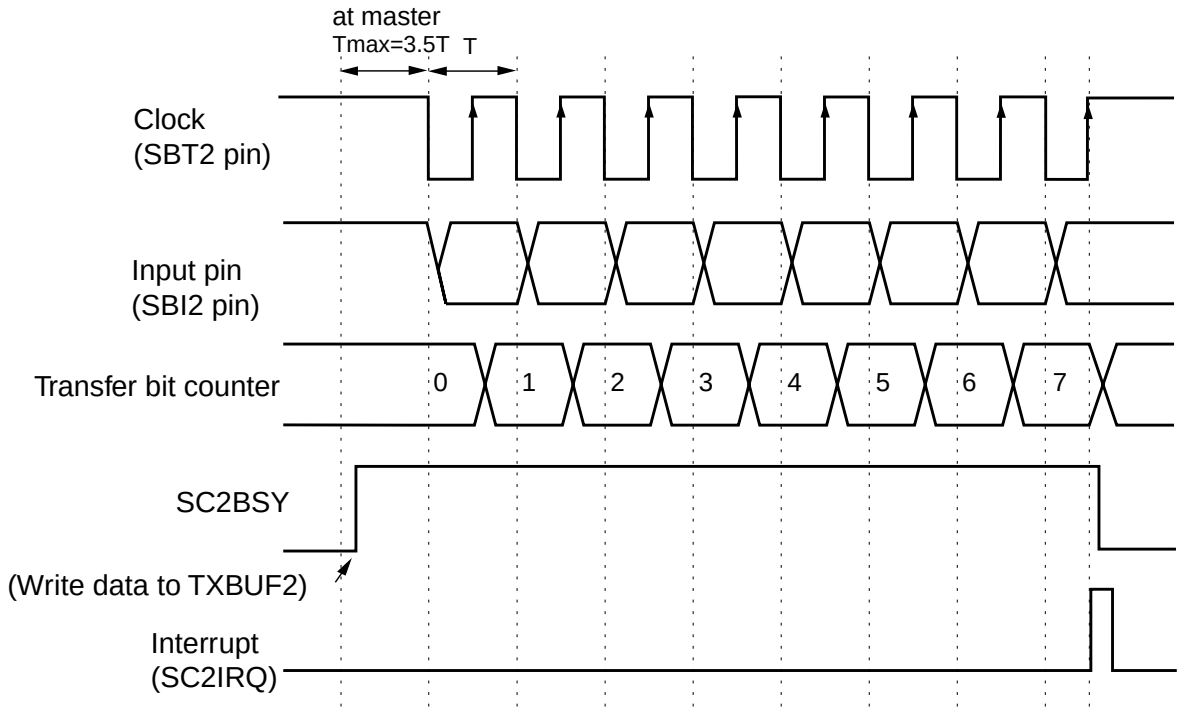


Figure:13.3.11 Reception Timing (Rising edge, Start condition is disabled)

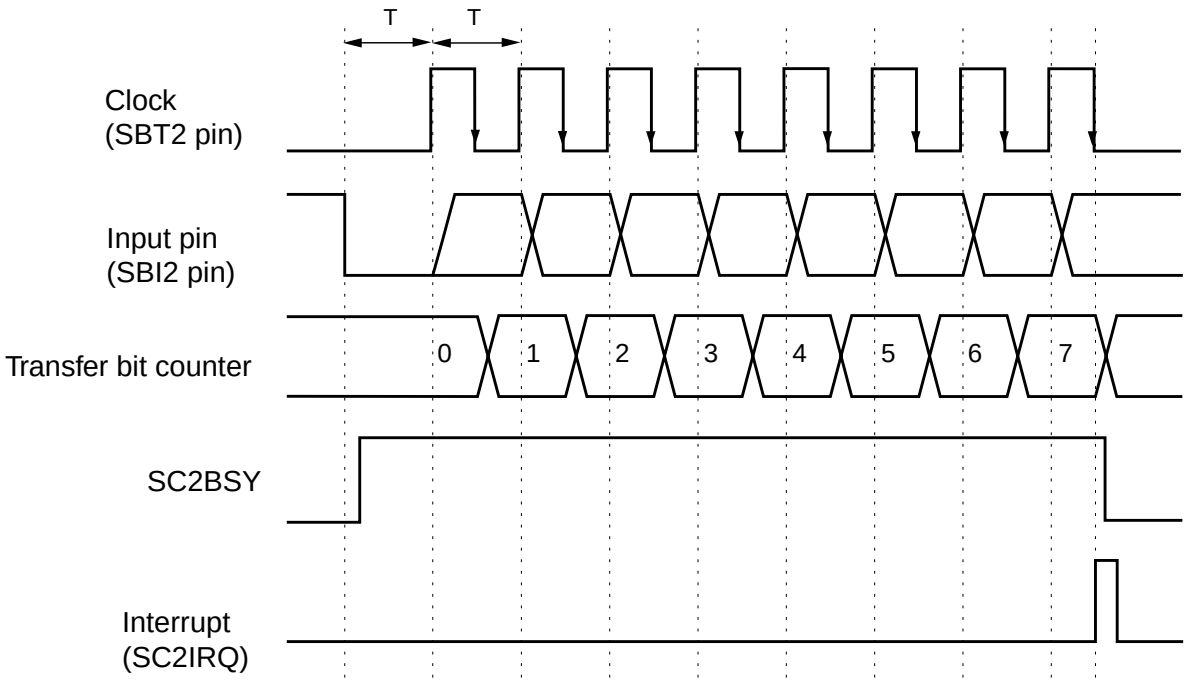


Figure:13.3.12 Reception Timing (Falling edge, Start condition is enabled)

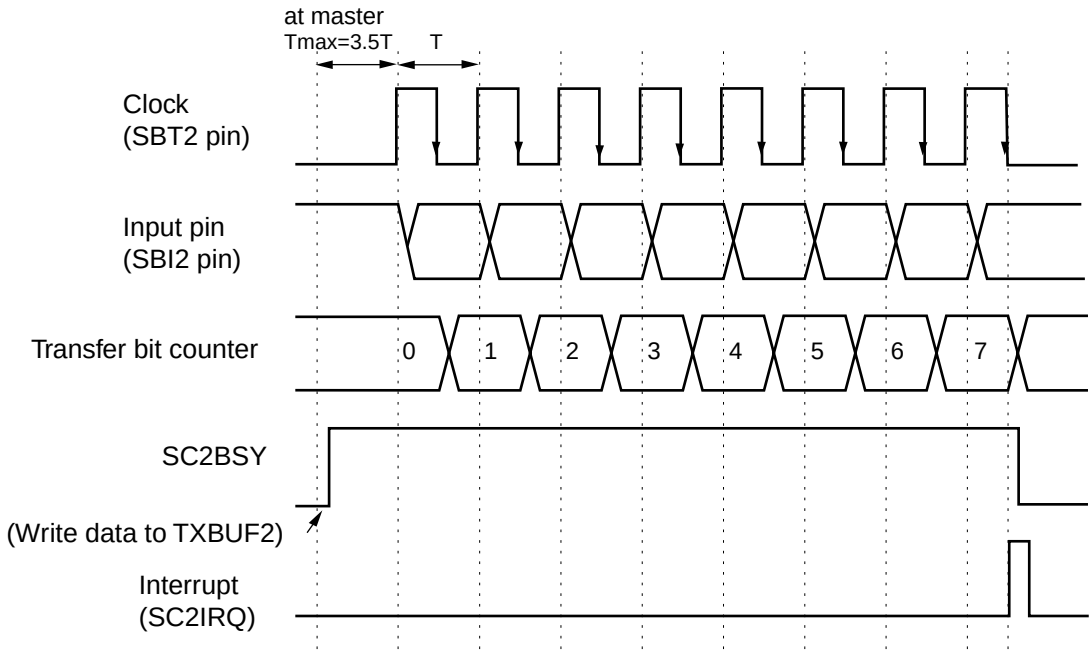


Figure:13.3.13 Reception Timing (Falling edge, Start condition is disabled)

■ Transmission / Reception

To operate transmission and reception at the same time, set the SC2CE1 flag of the SC2MD0 register to "0" or "1". As data is recieved at the opposite edge of the transmission clock, set the polarity of reception data input edge to opposite polarity of the transmission data output edge.

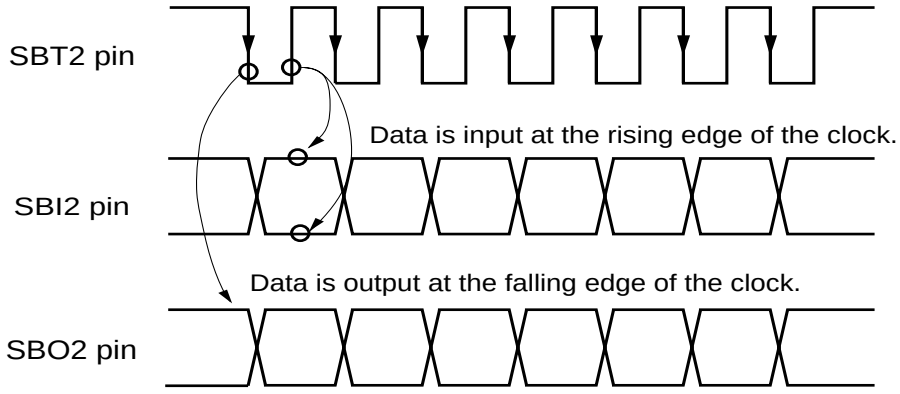


Figure:13.3.14 Transmission / Reception Timing (Reception : Rising edge, Transmission : Falling edge)

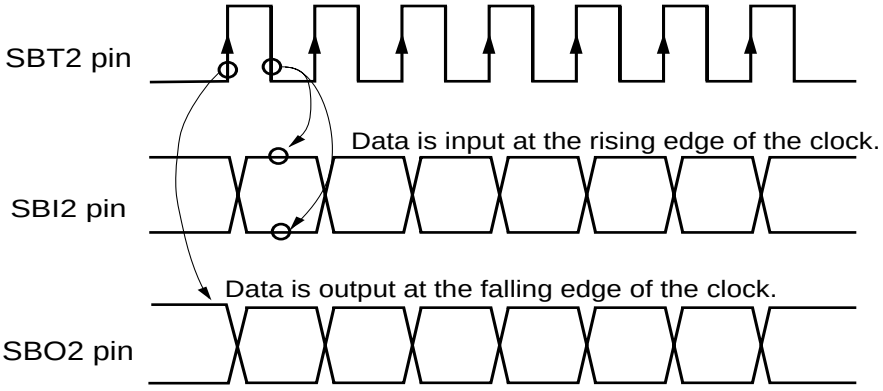


Figure:13.3.15 Transmission / Reception Timing (Reception : Falling edge, Transmission : Rising edge)

■ Communication in STANDBY mode

This serial interface is capable of slave reception in STANDBY mode. You can return the CPU operation from STANDBY mode to NORMAL mode using communication end interrupt SC2IRQ, which is generated after the slave reception.

(In STANDBY mode, continuous reception is desabled after data of transfer bit count set by SC2LNG2-0 flags of the SC2MD0 register is received. Read out the received data from transmission/reception shift register SC2TRB after returning to NORMAL mode.)

In STANDBY mode, reception with start condition is not available, thus, disable start condition. And set dummy data to tramsmission data buffer TXBUF2 before transition to STANDBY mode.

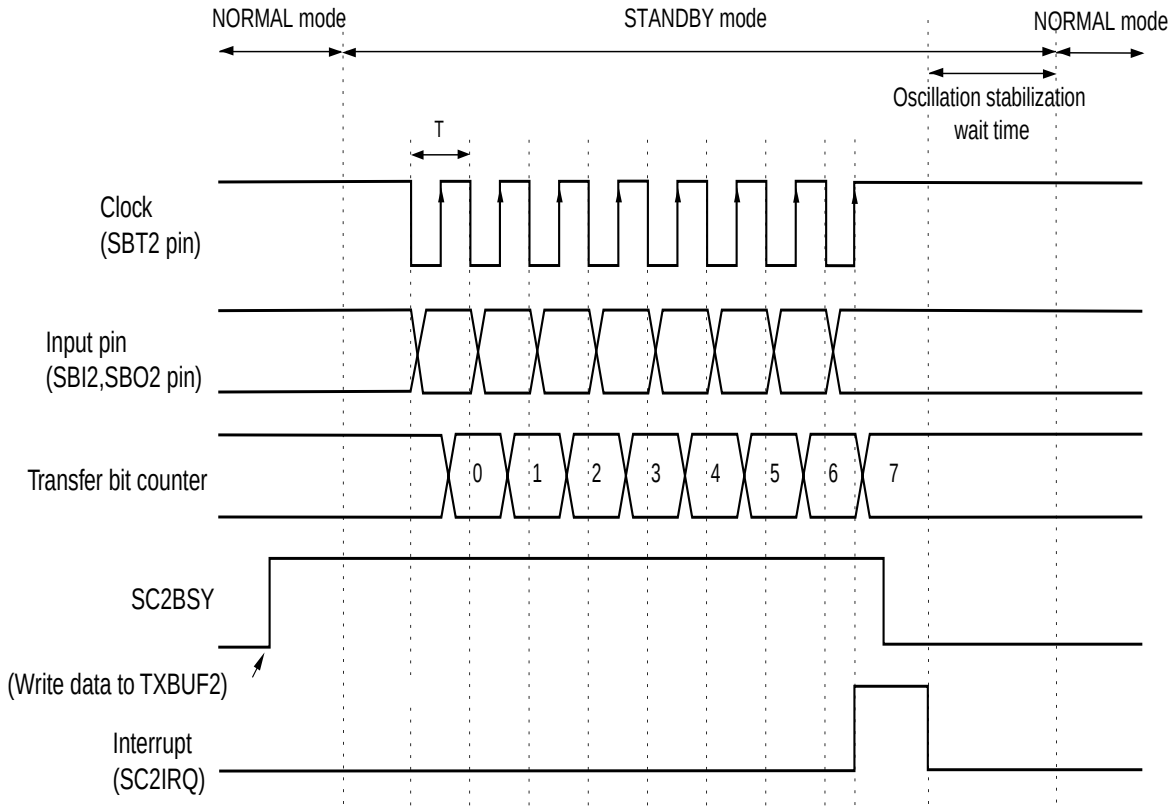


Figure:13.3.16 Reception Timing (Rising edge, Start condition is disabled)

■ Pins Setup (3 channels, at transmission)

Table:13.3.6 shows the pins setup at synchronous serial interface transmission with 3 channels (SBO2 pin, SBI2 pin, SBT2 pin).

Table:13.3.6 Synchronous Serial Interface Pins Setup (3 channels, at transmission)

Item	Data output pin	Data input pin	Clock I/O pin	
	SBO2 pin	SBI2 pin	SBT2 pin	
			Clock master	Clock slave
Pin	P03	P04	P05	
Serial data input selection	SBI2		-	
	SC2MD1(SC2IOM)			
Function	Serial data output	"1" input	Transfer clock I/O	Transfer clock I/O
	SC2MD1(SC2SBOS)	SC2MD1(SC2SBIS)	SC2MD1(SC2SBTS)	
Type	Push-pull/N-ch open-drain	-	Push-pull/N-ch open-drain	Push-pull/N-ch open-drain
	P0ODC(P0ODC3)		P0ODC(P0ODC5)	
I/O	Output mode	-	Output mode	Input mode
	P0DIR(P0DIR3)		P0DIR(P0DIR5)	
Pull-up	added / not added	-	added / not added	added / not added
	P0PLU(P0PLU3)		P0PLU(P0PLU5)	

■ Pins Setup (3 channels, at reception)

Table:13.3.7 shows the pins setup at synchronous serial interface reception with 3 channels (SBO2 pin, SBI2 pin, SBT2 pin).

Table:13.3.7 Synchronous Serial Interface Pins Setup (3 channels, at reception)

Item	Data output pin	Data input pin	Clock I/O pin	
	SBO2 pin	SBI2 pin	SBT2 pin	
			Clock master	Clock slave
Pin	P03	P04	P05	
Serial data input selection	SBI2		-	
	SC2MD1(SC2IOM)			
Function	Port	Serial data input	Transfer clock I/O	Transfer clock I/O
	SC2MD1(SC2SBOS)	SC2MD1(SC2SBIS)	SC2MD1(SC2SBTS)	
Type	-	-	Push-pull/N-ch open-drain	Push-pull/N-ch open-drain
			P0ODC(P0ODC5)	
I/O	-	Input mode	Output mode	Input mode
		P0DIR(P0DIR4)	P0DIR(P0DIR5)	
Pull-up	-	-	added / not added	added / not added
			P0PLU(P0PLU5)	

■ Pins Setup (3 channels, at reception / transmission)

Table:13.3.8 Synchronous Serial Interface Pins Setup (3 channels, at transmission / reception)

Item	Data output pin	Data input pin	Clock I/O pin	
	SBO2 pin	SBI2 pin	SBT2 pin	
			Clock master	Clock slave
Pin	P03	P04	P05	
Serial data input selection	SBI2		-	
	SC2MD1(SC2IOM)			
Function	Serial data output	Serial data output	Transfer clock I/O	Transfer clock I/O
	SC2MD1(SC2SBOS)	SC2MD1(SC2SBIS)	SC2MD1(SC2SBTS)	
Type	Push-pull/N-ch open-drain	-	Push-pull/N-ch open-drain	Push-pull/N-ch open-drain
	P0ODC(P0ODC3)		P0ODC(P0ODC5)	
I/O	Output mode	Input mode	Output mode	Input mode
	P0DIR(P0DIR3)	P0DIR(P0DIR4)	P0DIR(P0DIR5)	
Pull-up	added / not added	-	added / not added	added / not added
	P0PLU(P0PLU3)		P0PLU(P0PLU5)	

■ Pins Setup (2 channels, at transmission)

Table:13.3.9 shows the pins setup at synchronous serial interface transmission with 2 channels (SBO2pin, SBT2 pin). The SBI2 pin is not used, so that it can be used as a general port.

Table:13.3.9 Synchronous Serial Interface Pins Setup (2 channels, at transmission)

Item	Data output pin	Data input pin	Clock I/O pin	
	SBO2 pin	SBI2 pin	SBT2 pin	
			Clock master	Clock slave
Pin	P03	P04	P05	
Serial data input selection	SB02		-	
	SC2MD1(SC2IOM)			
Function	Serial data output	"1" input	Transfer clock I/O	Transfer clock I/O
	SC2MD1(SC2SBOS)	SC2MD1(SC2SBIS)	SC2MD1(SC2SBIS)	
Type	Push-pull/N-ch open-drain	-	Push-pull/N-ch open-drain	Push-pull/N-ch open-drain
	P0ODC(P0ODC3)		P0ODC(P0ODC5)	
I/O	Output mode	-	Output mode	Input mode
	P0DIR(P0DIR3)		P0DIR(P0DIR5)	
Pull-up	added / not added	-	added / not added	added / not added
	P0PLU(P0PLU3)		P0PLU(P0PLU5)	

■ Pins Setup (2 channels, at reception)

Table:13.3.10 shows the pins setup at synchronous serial interface reception with 2 channels (SBO2 pin, SBT2 pin). The SBI2 pin is not used, so that it can be used as a general port.

Table:13.3.10 Synchronous Serial Interface Pins Setup (2 channels, at reception)

Item	Data output pin	Data input pin	Clock I/O pin	
	SBO2 pin	SBI2 pin	SBT2 pin	
			Clock master	Clock slave
Pin	P03	P04	P05	
Serial data input selection	SB02		-	
	SC2MD1(SC2IOM)			
Function	Port	Serial input	Transfer clock I/O	Transfer clock I/O
	SC2MD1(SC2SBOS)	SC2MD1(SC2SBIS)	SC2MD1(SC2SBIS)	
Type	-	-	Push-pull/N-ch open-drain	Push-pull/N-ch open-drain
			P0ODC(P0ODC5)	
I/O	Input mode	-	Output mode	Input mode
	P0DIR(P0DIR3)		P0DIR(P0DIR5)	
Pull-up	-	-	added / not added	added / not added
			P0PLU(P0PLU5)	

13.3.2 Setup Example

■ Transmission / Reception Setup Example

Here is the setup example at transmission/reception with serial interface 2.Table:13.3.11 shows the conditions.

Table:13.3.11 Conditions for Synchronous Serial Interface at transmission / reception

Item	set to
Serial data input pin (SBI2/SBO2)	Independent (3 channels)
Transfer bit count	8 bits
Start condition	Disabled
First bit to be transferred	MSB
Input clock edge	Falling
Output clock edge	Rising
Clock	Clock master
Clock source	fs/2
SBT2/SB02 pin type	N-ch open-drain
SBT2 pull-up resistor	Added
SB02 pull-up resistor	Added
Serial interface 2 communication end interrupt	Enabled

An example setup procedure, with a description of each step is shown below.

Setup Procedure	Description
(1) Select prescaler operation. SC2MD3 (0x03F98) bp3 :SC2PSCE =1	(1) Set the SC2PSCE flag of the SC2MD3 register to "1" to select prescaler operation.
(2) Select the clock source. SC2MD3 (0x03F98) bp2-0 :SC2PSC2-0 =100	(2) Set the SC2PSC2-0 flag of the SC2MD3 register to "100" to select fs/2 for clock source.
(3) Control of pin type. P0ODC (0x03F1C) bp5 :P0ODC5 =1 bp3 :P0ODC3 =1 P0PLU (0x03F40) bp5 :P0PLU5 =1 bp3 :P0PLU3 =1	(3) Set the P0ODC5, P0ODC3 flags of the P0ODC register to "1, 1" to select N-ch open drain for the SBO2/SBT2 pin type. Set the P0ODC5, P0ODC3 flags of the P0PLU register to "1, 1" to add pull-up resistor.

Setup Procedure	Description
(4) Control of pin direction. P0DIR (0x03F30) bp5 :P0DIR5 =1 bp4 :P0DIR4 =0 bp3 :P0DIR3 =1	(4) Set the P0DIR5, P0DIR3 flags of the Port 0 pin control direction register (P0DIR) to "1, 1" and set P0DIR4 to "0" to set P05, P03 to output mode, to set P04 to input mode.
(5) Set the SC2MD0 register. Select the transfer bit count. SC2MD0 (0x03F96) bp2-0 :SC2LNG2-0 =111 Select the start condition. SC2MD0 (0x03F96) bp3 :SC2STE =0 Select the first bit to be transferred. SC2MD0 (0x03F96) bp4 :SC2DIR =0 Select the transfer edge. SC2MD0 (0x03F96) bp6 :SC2CE1 =1	(5) Set the SC2LNG2-0 flag of the serial 2 mode register 0 (SC2MD0) to "111" to set the transfer bit count to 8 bits. Set the SC2STE flag of the SC2MD0 register to "0" to disable start condition. Set the SC2DIR flag of the SC2MD0 register to "0" to set MSB as the first transfer bit. Set the SC2CE1 flag of the SC2MD0 register to "1" to set the transmission data output edge to "rising", and the received data input edge to "falling".
(6) Set the SC2CTR register. SC2CTR (0x03F9C) bp2 :SC2CMD =0	(6) Set the SC2CMD flag of the SC2CTR register to "0" to select serial data tansmission.
(7) Set the SC2MD1 register. Select the transfer clock. SC2MD1 (0x03F97) bp2 :SC2MST =1 Control of pin function. SC2MD1 (0x03F97) bp4 :SC2SBOS =1 bp5 :SC2SBIS =1 bp6 :SC2SBTS =1 bp7 :SC2IOM =0	(7) Set the SC2MST flag of the SC2MD1 register to "1" to select clock master (internal clock). Set the SC2SBOS, SC2SBIS, SC2SBTS flags of the SC2MD1 register to "1" to set the SBO2 pin to serial data output, the SBI2 pin to serial data input, and the SBT2 pin to transfer clock I/O. Set the SC2IOM flag to "0" to set "serial data input from the SBI2 pin".
(8) Set the interrupt level. SC2ICR (0x03FF6) bp7-6 :SC2LV1-0 =10	(8) Set the interrupt level by the SC2LV1-0 flag of the serial 2 interrupt control register (SC2ICR).
(9) Enable the interrupt. SC2ICR (0x03FF6) bp1 :SC2IE =1	(9) Enable the interrupt to by setting "1" to the SC2IE flag of the SC2ICR register. If the interrupt request flag (SC2IR of the SC2ICR register) is already set, clear SC2IR before enable interrupt.
(10) Start serial transmission. Transmission data → TXBUF2 (0x03F9B) Reception data → Input to SBI2 pin	(10) Set the transmission data to the serial transmission/ reception shift register TXBUF2. The internal clock is generated to start transmission/reception. After communication ends, the serial 2 interrupt SC2IRQ is generated.

Note : Procedures (1) to (2), (5), (6) and (7) can be set at once.

Note : Procedures (8) and (9) can be set at once.

For communication with 3 channels, set the SC2BIS of the SC2MD1 register to "0" to set the serial input to "1". The SBI2 pin can be used as a general port. For reception only, set the SC2SBOS of the SC2MD1 register to "0" to select port. The SBO2 pin can be used as a general port.

For communication with 2 channels, set the SBO2 pin to serial data I/O. The port direction control register P0DIR switches the I/O. For reception, set the SC2SBIS of the SC2MD1 register to "1" to select serial input. The SBO2 pin can be used as a general port.

You can shut down the communication by setting the SC2SBOS and the SC2SBIS of the SC2MD1 register to "0".

Set each flag in order of the setup procedures. Set all the control registers (refer to Table:13.2.1, except TXBUF2) before start communication.

Set the transfer rate of the transfer clock to under 5.0 MHz with the SC2MD3 register.

■ Transmission / Reception Setup Example (reception in STANDBY mode)

Here is the setup example at transmission/reception in STANDBY mode using serial interface 2. Table:13.3.12 shows the conditions.

Table:13.3.12 Conditions for Synchronous Serial Interface at transmission / reception (reception in STANDBY mode)

Item	set to
Serial data input pin(SBI2/SBO2)	Connection(2 channels)
Transfer bit count	8 bit
Start condition	Disabled
First bit to be transfered	MSB
Input clock edge	Falling
Clock	Clock slave
Operation mode	STOP mode
Clock source	fs/2
SBT2/SB02 pin type	Push-pull
SBT2 pull-up resistor	Not added
SBI2 pull-up resistor	Not added
Serial interface 2 communication end interrupt	Enabled

An example setup procedure, with a description of each step is shown below.

Setup Procedure	Description
(1) Select prescaler operation. SC2MD3 (0x03F98) bp3 :SC2PSCE =1	(1) Set the SC2PSCE flag of the SC2MD3 register to "1" to select prescaler operation.
(2) Select the clock source. SC2MD3 (0x03F98) bp2-0 :SC2PSC2-0 =100	(2) Set the SC2PSC2-0 flag of the SC2MD3 register to "100" to select fs/2 for clock source.
(3) Control of pin type. P0ODC (0x03F1C) bp7 :P0ODC5 =0 bp5 :P0ODC3 =0 P0PLU(0x03F40) bp7 :P0PLU5 =0 bp3 :P0PLU3 =0	(3) Set the P0ODC5, P0ODC3 flags of the P0ODC register to "0, 0" to select push-pull for the SBO2/SBT2 pin type. Set the P0PLU5, P0PLU3 flags of the P0PLU register to "0, 0" not to add pull-up resistor.
(4) Control of pin direction. P0DIR (0x03F30) bp7 :P0DIR5 =0 bp5 :P0DIR3 =0	(4) Set the P0DIR5, P0DIR3 flags of the Port 0 pin control direction register (P0DIR) to "0, 0" .04050304

Setup Procedure	Description
(5) Select the transfer bit count. SC2MD0 (0x03F96) bp2-0 :SC2LNG2-0 =111	(5) Set the SC2LNG2-0 flags of the serial 2 mode register (SC2MD0) to "111" to set the transfer bit count to 8 bits
(6) Select the start condition. SC2MD0 (0x03F96) bp3 :SC2STE =0	(6) Set the SC2STE flag of the SC2MD0 register to "0" to disable start condition.
(7) Select the first bit to be transferred. SC2MD0 (0x03F96) bp4 :SC2DIR =0	(7) Set the SC2DIR flag of the SC2MD0 register to "0" to set MSB as the first transfer bit.
(8) Select the transfer edge. SC2MD0 (0x03F96) bp6 :SC2CE1 =1	(8) Set the SC2CE1 flag of the SC2MD0 register to "1" to set the reception data input edge to "falling".
(9) Select the communication style . SC2CTR (0x03F9C) bp2 :SC2CMD =0	(9) Set the SC2CMD flag of the SC2CTR register to "0" to select synchronous serial interface.
(10) Select the transfer clock. SC2MD1 (0x03F97) bp2 :SC2MST =0	(10) Set the SC2MST flag of the SC2MD1 register to "0" to select clock slave (external clock).
(11) Control of pin function. SC2MD1(0x03F97) bp4 :SC2SBOS =0 bp5 :SC2SBIS =1 bp6 :SC2SBTS =1 bp7 :SC2IOM =0	(11) Set the SC2SBOS, SC2SBIS, SC2SBTS flags of the SC2MD1 register to "1" to set the SBO2 pin to general port, the SBI2 pin to serial data input, and the SBT2 pin to transfer clock I/O. Set the SC2IOM flag to "0" to set "serial data input from the SBI2 pin".
(12) Set the interrupt level SC2ICR (0x03FF6) bp7-6 :SC2LV1-0 =10	(12) Set the interrupt level (to level 2) by the SC2LV1-0 flags of the serial 2 interrupt control register (SC2ICR).
(13) Enable the interrupt. SC2ICR (0x03FF6) bp1 :SC2IE =1	(13) Enable the interrupt by setting "1" to the SC2IE flag of the SC2ICR register. If the interrupt request flag (SC2IR of the SC2ICR register) is already set, clear SC2IR before the interrupt is enabled. [Chapter 3 3.1.4. Interrupt Flag Setup]
(14) Set the activation source of serial communication. Dummy data → TXBUF2 (0x03F9B)	(14) Set dummy data to the serial transmission data buffer TXBUF2.
(15) Transition to STOP mode. CPUM (0x03F00) bp3:STOP =1	(15) Set the STOP flag of the CPUM register to "1" for transition to STOP mode.
(16) Start serial reception. Transfer clock → Input to SBT2 pin Reception data → Input to SBI2 pin	(16) Set the transfer clock to SBT2 pin and transfer data to SBI2 pin.

Setup Procedure	Description
(17) Return from STANDBY mode	(17) Serial 2 interrupt is generated at the same time with reception of 8 bits data, and then CPU returns from STOP mode to NORMAL mode after oscillation stabilization wait time.

Note : Procedures (5) to (8), (10) to (11), and (12) to (13) can be set at once.

For slave reception in STANDBY mode, disable the start condition. With other setup, normal reception is not guaranteed.

Set each flag in order of the setup procedures. Set all the control registers (refer toTable:13.2.1, except TXBUF2) before start communication.

13.3.3 Single Master IIC Serial Interface

Serial interface 2 is capable of IIC serial communication in single master. Communication of this IIC interface is based on the IIC-BUS data transfer format of Philips. Table:13.3.13 shows the functions of IIC serial interface.

Table:13.3.13 IIC Serial Interface Functions

Communication type	Single master IIC
Interrupt	SC2IRQ
Pins	SDA2,SCL2
Transfer bit count	1 to 8 bit
First transfer bit	O
ACK bit	O
ACK bit level	O
Clock source	fosc/2 fosc/4 fosc/8 fosc/16 fosc/32 fosc/64 fosc/128 fs/2 fs/4 timer 2 output timer 3 output
The transfer rate is the clock source divided by 8.	

Transfer rate needs to be set to slower rate than the system clock (fs).

■ Activation factor for Communication

Set data (at transmission) or dummy data (at reception) to the transmission/reception shift register TXBUF2. Start condition and transfer clock are generated to start communication, regardless of transmission/reception. This serial interface can not be used for slave communication.

■ Start Condition Setup

In IIC communication, enable start condition by the SC2STE flag of the SC2MD0 register at the first communication after reset release. From the second communication, the SC2STE flag of the SC2MD0 register can select if start condition is enabled or not.

If start condition is detected during data communication in which the start condition is enabled, the SC2STC flag of the SC2CTR register is set to "1", and the communication end interrupt SC2IRQ is generated to end the transmission. This means that the communication is not executed properly and needs to be re-executed. Clear the SC2STC flag by program. When data line (SDA2 pin) is changed from "H" to "L" while clock line (the SCL2 pin) is "H", start condition is generated.

■ Generation of Stop Condition

Stop condition is generated as the SDA2 line is changed from "L" to "H", while the SCL2 line is "H". Stop condition can be generated by setting the IICSTPC flag of the SC2CTR register to "0" by program.

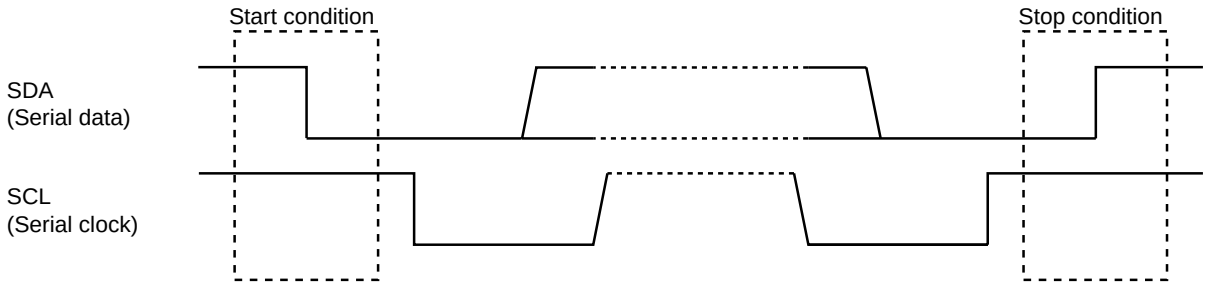


Figure:13.3.17 Start Condition and Stop Condition

■ Input Edge/Output Edge Setup

In IIC communication, data is always received at the falling edge of the clock. Even if the SC2CE1 flag is set to "0", the received data is stored in the falling edge of the clock.

■ Data I/O Pin Setup

The SDA2 pin (used as SBO2 pin, too) is used to input/output data. Set the SC2IOM flag of the SC2MD1 register to "1" to input serial data from the SBO2 pin. As the SBI2 pin is not used at that time, it can be used as a general port. But always set the SC2SBIS flag of the above register to "1" to set "input serial data".

To detect start condition, set the SC2SBIS flag of the SC2MD1 register to "input serial data", regardless of transmission/reception.

■ Reception of Confirming (ACK) Bit after Data Transmission

The SC2ACKS flag of the SC2CTR register selects if ACK bit is enabled or not. If ACK bit is enabled, ACK bit is received from the slave station after data (1 to 8 bits) is transferred. At reception of ACK bit, the SDA2 line is automatically released. To receive ACK bit, 1 clock is output to store ACK bit to the SC2ACK0 of the SC2CTR register. The transmission/reception shift register SC2TRB is not operated by the ACK bit reception clock. When the received ACK bit level is "L", the reception is normal at slave and the next data can be received. If the level is "H", the reception maybe completed at slave, so set the IICSTPC flag of the SC2CTR register to "0" to end communication.

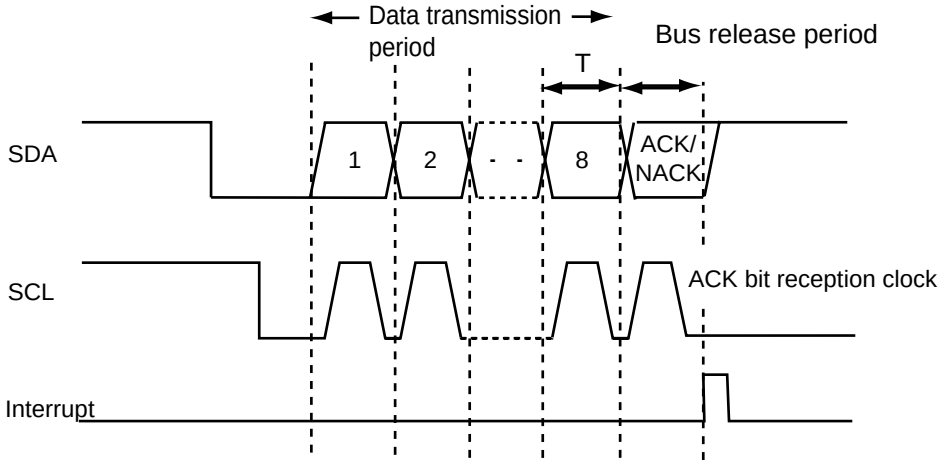


Figure:13.3.18 ACK Bit Reception Timing after Transmission of 8-Bit Data

■ Transmission of Confirming (ACK Bit) of Data Reception

Selection of enable/disable of ACK bit is same with at the transmission. When ACK bit is enabled, ACK bit and clock are output after data (1 to 8 bits) is received. When the reception is continued, ACK bit outputs "L". And when the reception is finished, it outputs "H". The SC2ACK0 of the SC2CTR register sets the output ACK bit level.

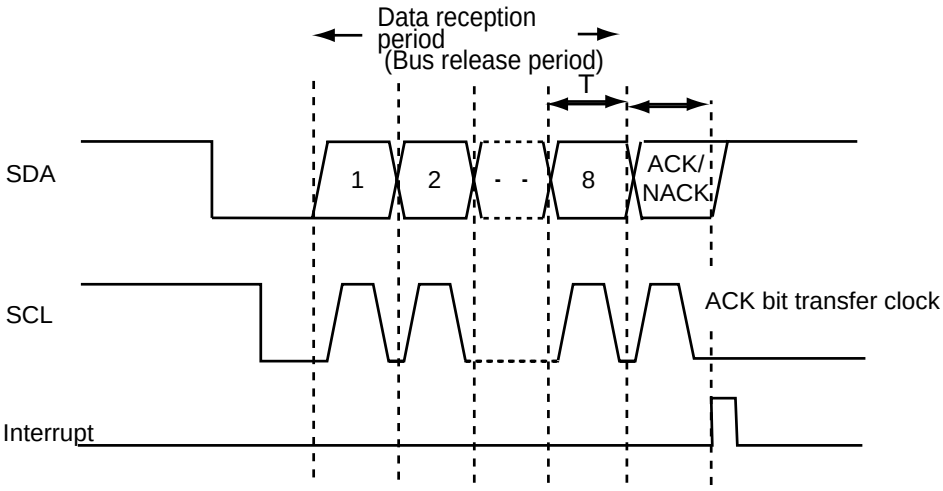


Figure:13.3.19 ACK Bit Transmission Timing after Reception of 8-Bit Data

■ Transfer Format

There are two transfer format used on IIC bus are : the addressing format that transmits/receives data after 1 byte data (address data) that consists of slave address (7 bits) and R/W bit (1 bit) is transferred after start condition, and the free data format that transmits data right after the start condition. The serial interface of this LSI supports 2 communication formats for only master transmission and master reception in IIC communication. Sequence of communication is shown below. The shaded part shows the data transferred from slave.

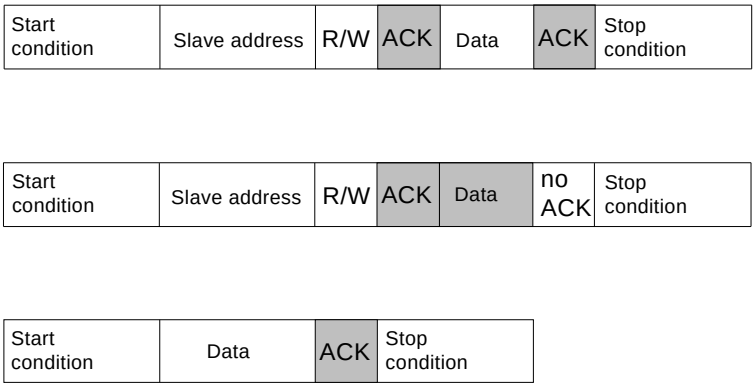


Figure:13.3.20 Communication Sequence on Each Transfer Format

[Figure:13.3.21 Master Transmission Timing, Figure:13.3.22 Master Reception Timing]

■ Clock Setup

The transfer clock for IIC communication is obtained by dividing clock source by 8 inside this serial. The clock source is selected from the dedicated prescaler, timer 2 or 3 output by the SC2MD3 register. The clock source should be set in such a way that the transfer rate is under 100 kHz in NORMAL mode, 400 kHz in high speed mode with the SC2MD3 register. The dedicated prescaler starts as this register selects "prescaler count enable". Set the SC2MST flag of the SC2MD1 register to "1" to select the internal clock (clock master). This IIC interface can not be used with external clock (clock slave).

Table:13.3.14 IIC Serial Interface Clock Sources

	Single master IIC
Clcok source (internal clock)	fosc/2
	fosc/4
	fosc/8
	fosc/16
	fosc/32
	fosc/64
	fosc/128
	fs/2
	fs/4
	timer 2 output
	timer 3 output

The transfer rate in IIC communication is obtained by dividing clock source by 8. The clock source should be set in such a way that the transfer rate is under 100 kHz in NORMAL mode, 400 kHz in high speed mode with the SC2MD3 register.

Set the SC2MST flag of the SC2MD1 register to "1" to select internal clock (clock master).

Set the SC2SBIS and SC2SBOS flags of the SC2MD1 register to "0" before change the clock setup.

■ Transmission/Reception Mode Setup and Operation

The SC2REX flag of the SC2CTR register selects the status of the transmission or the reception. The first data is always added start condition for communication. The start condition is output from this serial (master).

The start condition is not added over the second communication, select the start condition "none" at the first setting. And the start condition is added over the second communication, select the start condition "enable" at the first setting.

At addressing format, slave address and R/W bit are set to the first data after start condition for transmission. At master reception, switch to the reception mode at the interrupt transaction after the transmission of the first 1 byte data is finished, after the ACK signal from slave is confirmed. If the communication should be continued to other device without stop, transmit slave address and R/W bit again after start condition is generated again. At reception, the SDA line is automatically released to wait for reception. After the storage of data is finished, confirmation of the reception (ACK bit) is output.

[Figure:13.3.21 Master Transmission Timing, Figure:13.3.22 Master Reception Timing]

■ IIC BUSY Flag Operation

As data is set to the transmission/reception shift register TXBUF2, the IICBSY flag of the SC2CTR register is set to "1", then the IICBSY flag is cleared to "0" at transmission/reception end (communication with ACK) or at last bit communication end (communication without ACK). Setting "1" to the stop condition generation flag (IISTPC), sets IICBSY flag to "1". After stop condition ends, it is cleared to "0".

If start condition is detected during communication, the communication end interrupt SC2IRQ is generated and the IICBSY flag is automatically cleared.

■ Forced Reset

You can shut down the communication by setting both of the SC2SBOS flag and the SC2SBIS flag of the SC2MD1 register to "0" (the SBO2 pin function : port, input data : input "1"). When a forced reset is done, the status register (all flag of the SC2STR register) and SC2BSY flag of the SC2MD0 register are cleared, but other control registers hold their set values.

Forced reset is operated at IICBSY is "0". And generate the stop condition and end the communication.

- First Transfer Bit Setup

Refer to : XIII-15

- Transmission, Reception Data Buffer

Refer to : XIII-15

- Transfer Bit Count and First Transfer Bit

Refer to : XIII-16

- Continuous Communication

Refer to : XIII-17

- Automatic Continuous Transfer by ATC

Refer to : XIII-17

In communication, set Nch-open drain for pin type, as the hardware switches if bus is used/ released. In reception, set the SDA2 pin (the SBO2 pin) direction to "output".

■ Master Transmission Timing

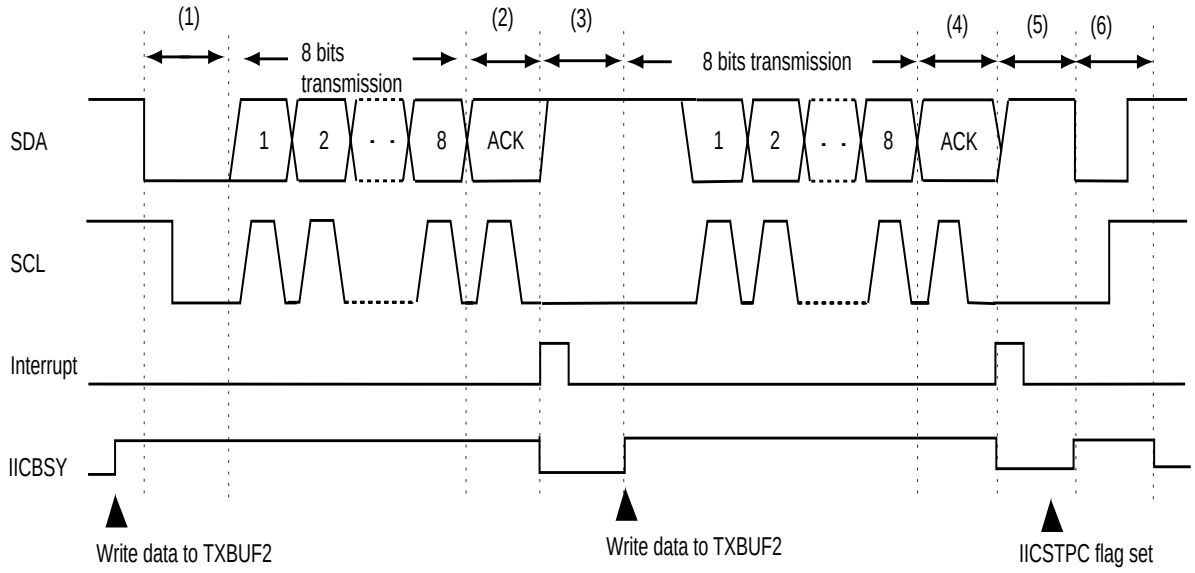


Figure:13.3.21 Master Transmission Timing

(1) Output start condition.

(2) Bus released period, ACK bit is received.

(3) Interrupt

Set data to TXBUF2

(4) Receive ACK bit.

(5) Interrupt

Communication ends : clear the IICBSY flag.

(6) Generates stop condition.

■ Master Reception Timing

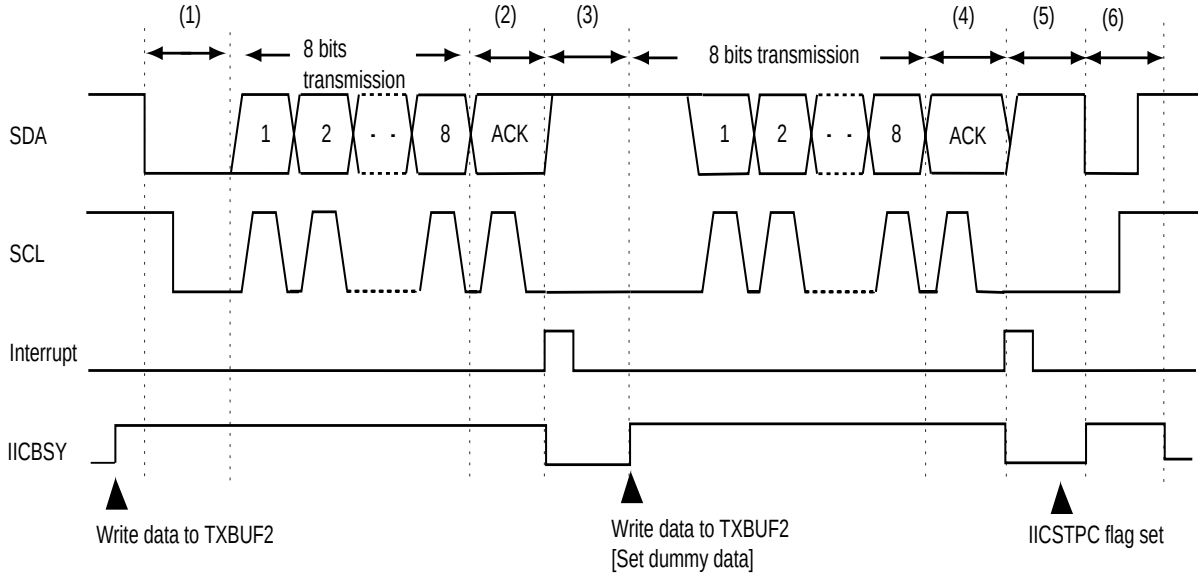


Figure:13.3.22 Master Reception Timing

(1) Output start condition.

(2) Bus released period, ACK bit is received.

(3) Interrupt

Set to reception mode : SC2REX = 0 → 1

Set data to TXBUF2

(4) Receive ACK bit.

(5) Interrupt

Communication ends : clear the IICBSY flag.

(6) Generates stop condition.

■ Pin Setup (2 channels, at transmission)

Table:13.3.15 shows the pins setup in IIC serial interface transmission with 2 channels (SDA2 pin, SCL2 pin).

Table:13.3.15 Pin Setup (2 channels, at transmission)

Item	Data I/O pin	Clock output pin
	SDA2 pin	SCL2 pin
Pin	P03	P05
SDA2/SCL2 pins	SBI2/SBO2 pin connection	-
	SC2MD1(SC2IOM)	
Function	Serial data output	Transfer clock output
	SC2MD1(SC2SBOS)	SC2MD1(SC2SBTS)
	Serial data input	-
	SC2MD1(SC2SBIS)	
Type	N-ch open-drain	N-ch open-drain
	P0ODC(P0ODC3)	P0ODC(P0ODC5)
I/O	output mode	output mode
	P0DIR(P0DIR3)	P0DIR(P0DIR5)
Pull-up	added	added
	P0PLU(P0PLU3)	P0PLU(P0PLU5)

■ Pin Setup (2 channels, at reception)

Table:13.3.16 shows the pins setup in IIC serial interface reception with 2 channels (SDA2 pin, SCL2 pin).

Table:13.3.16 Pin Setup (2 channels, at reception)

Item	Data I/O pin	Clock output pin
	SDA2 pin	SCL2 pin
Pin	P03	P05
SDA2/SCL2 pins	SBI2/SBO2 pin connection	-
	SC2MD1(SC2IOM)	
Function	Port	Transfer clock output
	SC2MD1(SC2SBOS)	SC2MD1(SC2SBTS)
	Serial data input	-
	SC2MD1(SC2SBIS)	
Type	N-ch open-drain	N-ch open-drain
	P0ODC(P0ODC3)	P0ODC(P0ODC5)
I/O	output mode	output mode
	P0DIR(P0DIR3)	P0DIR(P0DIR5)
Pull-up	added	added
	P0PLU(P0PLU3)	P0PLU(P0PLU5)

13.3.4 Setup Example

■ Master Transmission Setup Example

Here is the setup example of the transmission of several bytes data to the all the devices on IIC bus using IIC serial Interface 2. Table:13.3.17 shows the conditions.

Table:13.3.17 Conditions Single Master IIC Communication Setup

Item	Set to
SBI2/SBO2 pins	Connection (2 channels)
Transfer bit count	8 bits
Start condition	Enable (disable after second communication)
First transfer bit	MSB
ACK bit	Enable
IIC communication mode	NORMAL mode
Clock source	fosc/32
SCL2/SDA2 pin type	N-ch open-drain
SCL2 pull-up resistance	added
SDA2 pull-up resistance	added

An example setup procedure, with a description of each step is shown below.

Setup Procedure	Description
(1) Select prescaler operation. SC2MD3 (0x03F98) bp3: SC2PSCE =1	(1) Set the SC2PSCE flag of the SC2MD3 register to "1" to select prescaler operation.
(2) Select the clock source. SC2MD3 (0x03F98) bp2-0: SC2PSC2-0 =011	(2) SC2PSC2-0 flags of the SC2MD3 register to "011" to select fs/32 at clock source.
(3) Control of pin type. P0ODC (0x03F1C) bp2: P0ODC5 =1 bp0: P0ODC3 =1	(3) Set the P0ODC5, 3 flag of the P0ODC register to "1, 1" to select N-ch open drain for the SDA2/SCL2 pin type.
(4) Control of pin direction. P0DIR (0x03F30) bp2: P0ODC5 =1 bp0: P0ODC3 =1	(4) Set the P0DIR5, 3 flag of P0 pin control direction register (P0DIR) to "1, 1" to set P05, P03, to output mode.

Setup Procedure	Description
(5) Set ACK bit. SC2CTR (0x03F9C) bp0 :SC2ACKO =x bp1 :SC2ACKS =1	(5) Set the SC2ACKS flag of the serial 2 control register (SC2CTR) to "1" to select "receive ACK bit". ACK bit is received at transmission, and setup of the ACK bit level with the SC2ACKS flag is not necessary.
(6) Select the communication mode. SC2CTR (0x03F9C) bp4 :SC2TMD =0	(6) Set the SC2TMD flag of the serial 2 control register (SC2CTR) to "0" to select NORMAL mode.
(7) Select the communication type. SC2CTR (0x03F9C) bp2 :SC2CMD =1	(7) Set the SC2CMD flag of the serial 2 control register (SC2CTR) to "1" to select IIC.
(8) <Transmission setup> Selection of transmission/reception SC2CTR(0x03F9C) bp3 :SC2REX =0	(8) Set the SC2REX flag of the serial 2 control register (SC2CTR) to "0" to select the transmission mode.
(9) Initialize the monitor flag. SC2CTR (0x03F9C) bp6 :IICSTC =0	(9) Set the IICSTC flag of the serial 2 control register (SC2CTR) to "0, 0" to initialize the start condition detection flag.
(10) Set the SC2MD0 register. Select the transfer bit count. SC2MD0 (0x03F96) bp2-0 :SC2LNG2-0 =111 Select the start condition. SC2MD0 (0x03F96) bp3 :SC2STE =0 Select the first bit to be transferred. SC2MD0 (0x03F96) bp4 :SC2DIR =0 Select the IIC communication edge. SC2MD0(0x03F96) bp6 :SC2CE1 =1	(10) Set the SC2LNG2-0 flag of the serial 2 mode register (SC2MD0) to "111" to set the transfer bit count to 8 bits. Set the SC2STE flag of the SC2MD0 register to "0" to disable start condition. And start condition is not added over the second communication. Set the SC2DIR flag of the SC2MD0 register to "0" "to set MSB as the first bit to be transferred. In IIC communication, set the SC2CE1 flag of the SC2MD0 register to "1".
(11) Set the SC2MD1 register. Select the transfer clock. SC2MD1 (0x03F97) bp2 :SC2MST =1 Control of pin function. SC2MD1 (0x03F97) bp4 :SC2SBOS =1 bp5 :SC2SBIS =1 bp6 :SC2SBTS =1 bp7 :SC2IOM =1	(11) Set the SC2MST flag of the SC2MD1 register to "1" to select clock master (internal clock). In IIC communication, do not select external clock. Set the SC2SBOS, SC2SBIS, SC2SBTS flags of the SC2MD1 register to "1" to set the SDA2 pin (the SBO2 pin) to serial data output, the SBI2 pin to serial data input, and the SCL2 pin (the SBT2 pin) to serial clock I/O. Set the SC2IOM flag to "1" to set "serial data input from the SDA2 pin (the SBO2 pin)".
(12) Set the interrupt level. SC2ICR (0x03FF6) bp7-6 :SC2LV1-0 =10	(12) Set the interrupt level by the SC2LV1-0 flag of the serial 2 interrupt control register (SC2ICR).

Setup Procedure	Description
(13) Enable the interrupt. SC2ICR (0x03FF6) bp1 :SC2IE =1	(13) Set "1" to the SC2IE flag of the SC2ICR register to enable the interrupt. If the interrupt request flag (SC2IR of the SC2ICR register) is already set, clear SC2IR before the interrupt is enabled. [Chapter 3 3.1.4. Interrupt Flag Setup]
(14) <Start serial transmission.> Start serial transmission. Confirm that SCL2 (P05) is "H". Transmission data → TXBUF2 (0x03F9B)	(14) Set the transmission data to the transmission/reception shift register TXBUF2. Then the transfer clock is generated to start transmission. If the ACK bit is received after data transmission, the communication end interrupt SC2IRQ is generated.
(15) <Transmission ends.> <Setup of the next data transmission> Judge the monitor flag. SC2CTR (0x03F9C) bp6 :IICSTC	(15) Confirm the IICSTC flag of the serial 2 control register (SC2CTR). When the previous transmission is completed properly, IICSTC = "0". If IICSTC = "1", the communication should be re-executed.
(16) Judge the ACK bit level. SC2CTR (0x03F9C) bp0 :SC2ACKO	(16) Confirm the level of the ACK bit, received by the SC2ACKO flag of the serial 2 control register (SC2CTR). When SC2ACKO = 0, you can continue the transmission. When SC2ACKO = 1, the reception at slave may not be operated properly, so finish the communication.
(17) Set the SC2MD0 register. Select the transfer bit count. SC2MD0 (0x03F96) bp2-0 :SC2LNG2-0	(17) To change the transfer count bit, set the transfer count bit by the SC2LNG2-0 flag of the serial 2 mode register (SC2MD0).
(18) <Next data transmission is started.> Serial transmission is started. [→ (14)]	(18) Set the transmission data to TXBUF2 to start the transmission. [→ (14)]
(19) <Transmission ends.> <IIC communication end processing> Set the IICSTPC flag SC2CTR (0x03F9C) bp5 :IICSTPC =1	(19) Set the IICSTPC flag of the serial 2 control register (SC2CTR) to "1", so that the stop condition is automatically generated to finish the communication.

Note : Procedures (1) to (2) can be set at once.

Note : Procedures (5) to (9) can be set at once.

Note : Procedures (10) to (11) can be set at once.

Note : Procedures (12) to (13) can be set at once.

Set each flag in order of the setup procedures. Set all the control registers (refer toTable:13.2.1, except TXBUF2) before start communication.

Chapter 14 Serial Interface 3

14

14.1 Overview

This LSI contains a serial interface 3 that is capable of both clock synchronous / IIC (single master) serial communication.

14.1.1 Functions

Table:14.1.1 shows the serial interface 3 functions.

Table:14.1.1 Serial Interface 3 Functions

Communication style	Clock synchronous	IIC (single master)
Interrupt	SC3IRQ	SC3IRQ
Pins	SBO3,SBI3,SBT3	SDA3,SCL3
3 channels type	O	-
2 channels type	O (SBO3,SBT3)	O
Transfer bit count	1 to 8 bit	1 to 8 bit
Start condition	O	O
First transfer bit	O	O
Input edge / Output edge	O	-
SBO3 output control after transfer of last data	H/L/ last data hold	-
Function in STANDBY mode	Slave reception only	-
ACK bit	-	O
ACK bit level	-	O
Continuous operation (with ATC1)	O	-
Clock sources	fosc/2 fosc/4 fosc/16 fosc/32 fosc/64 fosc/128 fs/2 fs/4 external clock timer 3 output timer 5 output	fosc/2 fosc/4 fosc/16 fosc/32 fosc/64 fosc/128 fs/2 fs/4 timer 3 output timer 5 output

Maximum transfer rate	5.0 MHz	NORMAL mode: 100 kHz High speed mode: 400 kHz
fosc : machine clock (for high speed ocillation) fs : system clock In IIC communication, transfer clock is obtained by dividing the clock source by 8.		

Transfer rate should be set slower than system clock (fs).

14.1.2 Block Diagram

■ Serial Interface 3 Block Diagram

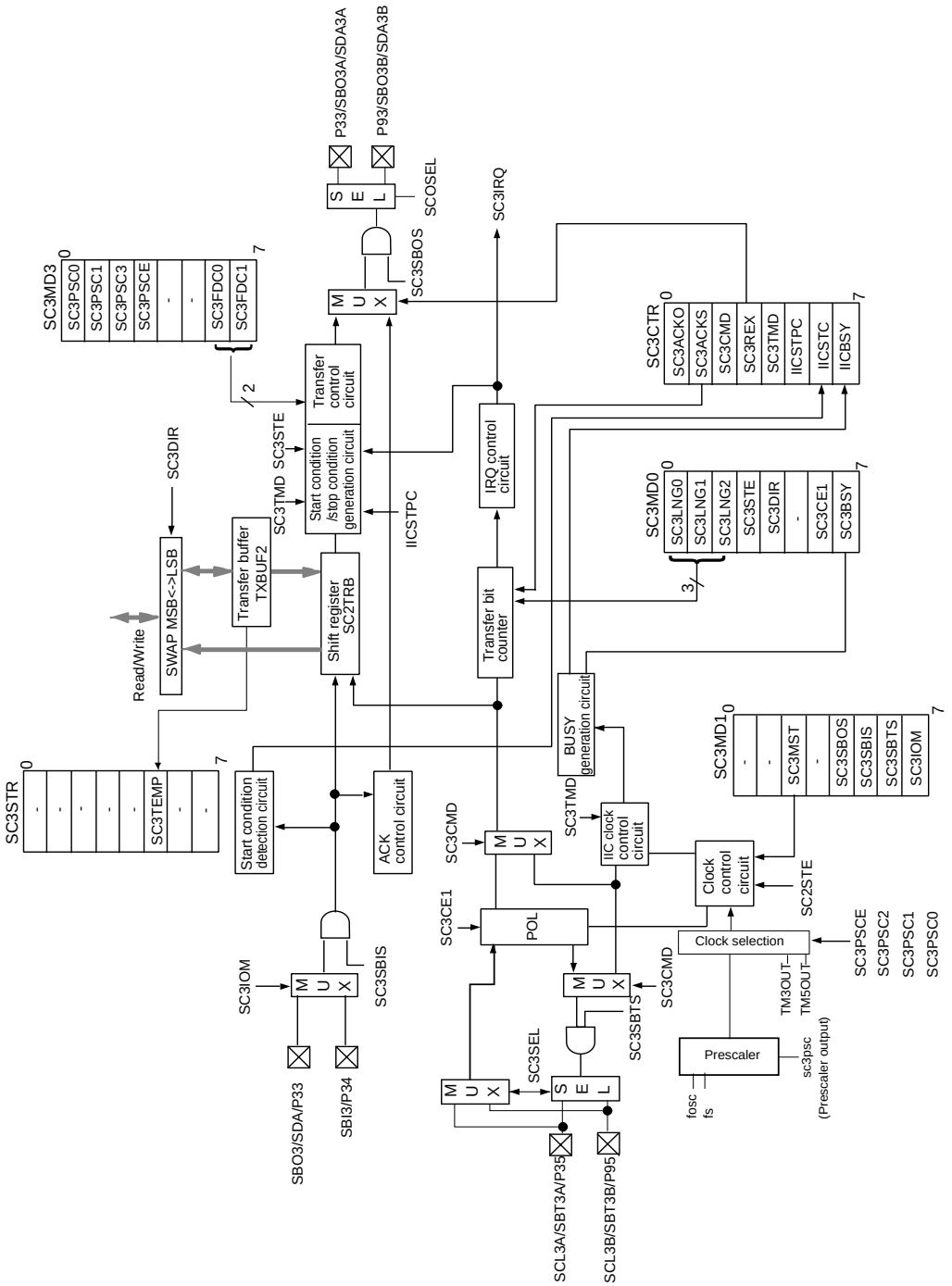


Figure:14.1.1 Serial Interface 3 Block Diagram

14.2 Control Registers

14.2.1 Registers List

Table:14.2.1 shows the registers that control serial interface 3.

Table:14.2.1 Serial Interface 3 Control Registers List

Register	Address	R/W	Function	Page
SC3MD0	0x03FA4	R/W	Serial interface 3 mode register 0	XIV-7
SC3MD1	0x03FA5	R/W	Serial interface 3 mode register 1	XIV-8
SC3MD3	0x03FA6	R/W	Serial interface 3 mode register 3	XIV-9
SC3STR	0x03FA7	R	Serial interface 3 status register	XIV-10
SC3TRB	0x03FA8	R	Serial interface 3 transmission/reception shift register	XIV-6
TXBUF3	0x03FA9	R/W	Serial interface 3 transmission data buffer	XIV-6
SC3CTR	0x03FAA	R/W	Serial interface 3 control register	XIV-11
SCSEL	0x03F4F	R/W	Serial I/O pin switching control register	XI-12
P3ODC	0x03F2C	R/W	Port 3 N-ch open drain control register	IV-37#
P3DIR	0x03F33	R/W	Port 3 direction control register	IV-36
P3PLU	0x03F49	R/W	Port 3 pull-up control register	IV-37
P9ODC	0x03F4C	R/W	Port 9 N-ch open drain control register	IV-92
P9DIR	0x03F39	R/W	Port 9 direction control register	IV-91
P9PLU	0x03F49	R/W	Port 9 pull-up control register	IV-92
SC3ICR	0x03FF7	R/W	Serial interface 3 interrupt control register	III-41
SCCKSEL	0x03F8E	R/W	Serial clock cycle switching control register	XIII-13

R /W : Readable / Writable

R : Readable

14.2.2 Data Buffer Register

Serial interface 3 has a 8-bit serial data buffer register for transmission.

■ Serial Interface 3 Transmission Data Buffer (TXBUF3: 0x03FA9)

bp	7	6	5	4	3	2	1	0
Flag	TXBUF37	TXBUF36	TXBUF35	TXBUF34	TXBUF33	TXBUF32	TXBUF31	TXBUF30
At reset	X	X	X	X	X	X	X	X
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

14.2.3 Data Register

Serial interface 3 has a 8-bit serial data register.

■ Serial Interface 3 Transmission / Reception Shift Register (SC3TRB: 0x03FA8)

bp	7	6	5	4	3	2	1	0
Flag	SC3TRB7	SC3TRB6	SC3TRB5	SC3TRB4	SC3TRB3	SC3TRB2	SC3TRB1	SC3TRB0
At reset	X	X	X	X	X	X	X	X
Access	R	R	R	R	R	R	R	R

14.2.4 Serial interface 3 Mode Register

■ Serial Interface 3 Mode Register 0 (SC3MD0: 0x03FA4)

bp	7	6	5	4	3	2	1	0
Flag	SC3BSY	SC3CE1	-	SC3DIR	SC3STE	SC3LNG2	SC3LNG1	SC3LNG0
At reset	0	0	-	0	0	1	1	1
Access	R	R/W	-	R/W	R/W	R/W	R/W	R/W

bp	Flag	Description
7	SC3BSY	Serial bus status in clock synchronous communication 0: Other use 1: Serial transmission is in progress
6	SC3CE1	Transmission data output edge Reception data input edge 0: Falling Rising 1: Rising Falling
5	-	-
4	SC3DIR	First bit to be transferred 0: MSB first 1: LSB first
3	SC3STE	Start condition 0: Disable start condition 1: Enable start condition
2-0	SC3LNG2 SC3LNG1 SC3LNG0	Transfer bit count 000: 1 bit 001: 2 bit 010: 3 bit 011: 4 bit 100: 5 bit 101: 6 bit 110: 7 bit 111: 8 bit

■ Serial interface 3 Mode Register 1 (SC3MD1: 0x03FA5)

bp	7	6	5	4	3	2	1	0
Flag	SC3IOM	SC3SBTS	SC3SBIS	SC3SBOS	-	SC3MST	-	-
At reset	0	0	0	0	-	0	-	-
Access	R/W	R/W	R/W	R/W	-	R/W	-	-

bp	Flag	Description
7	SC3IOM	Serial data input selection 0: Data input from SBI3 1: Data input from SBO3 (SDA3)
6	SC3SBTS	SBT3 pin function 0: Port 1: Transfer clock input / output
5	SC3SBIS	Serial input control 0: "1" input 1: Serial data input
4	SC3SBOS	SBO3(SDA3) pin function 0: Port 1: Serial data output
3	-	-
2	SC3MST	Clock master / slave selection 0: Slave 1: Master
1-0	-	-

■ Serial interface 3 Mode Register 3 (SC3MD03: 0x03FA6)

bp	7	6	5	4	3	2	1	0
Flag	SC3FDC1	SC3FDC0	-	-	SC3PSCE	SC3PSC3	SC3PSC1	SC3PSC0
At reset	0	0	-	-	0	0	0	0
Access	R/W	R/W	-	-	R/W	R/W	R/W	R/W

bp	Flag	Description
7-6	SC3FDC1 SC3FDC0	SBO3 output selection after transfer of last data 00: Fixed to "1"(High) output 01: Hold last data 10: Fixed to "0"(Low) output 11: Reserved
5-4	-	-
3	SC3PSCE	Prescaler count control 0: Disable the count 1: Enable the count
2-0	SC3PSC3 SC3PSC1 SC3PSC0	Clock selection 000: fosc/2 001: fosc/4 010: fosc/16 011: fosc/32 100: fs/2 101: fs/4 110: timer 3 output 111: timer 5 output

* This depends on SCCKSEL5 flag and SCCKSEL4 flag of SCCKSEL register.
(refer to table 13.2.9 serial clock cycle switching control register)

■ Serial interface 3 Status Register (SC3STR: 0x03FA7)

bp	7	6	5	4	3	2	1	0
Flag	-	-	SC3TEMP	-	-	-	-	-
At reset	-	-	0	-	-	-	-	-
Access	-	-	R	-	-	-	-	-

bp	Flag	Description
7-6	-	-
5	SC3TEMP	Transfer buffer empty flag 0: Empty 1: Full
4-0	-	-

■ Serial interface 3 Control Register (SC3CTR: 0x03FAA)

bp	7	6	5	4	3	2	1	0
Flag	IICBSY	IICSTC	IICSTPC	SC3TMD	SC3REX	SC3CMD	SC3ACKS	SC3ACK0
At reset	0	0	0	0	0	0	0	0
Access	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bp	Flag	Description
7	IICBSY	Serial bus status in IIC communication 0: Other use 1: Serial transmission is in progress
6	IICSTC	Start condition 0: Disable start condition 1: Enable start condition
5	IICSTPC	Stop condition detection flag in IIC communication 0: undetected 1: detected
4	SC3TMD	Communication mode 0: NORMAL mode 1: High-speed mode
3	SC3REX	Transmission / reception mode selection 0: Transmission 1: Reception
2	SC3CMD	Synchronous / IIC selection 0: Synchronous 1: IIC
1	SC3ACKS	ACK bit enable 0: Enable 1: Disable
0	SC3ACK0	ACK bit level selection 0: L level 1: H level

*1: “1“ is not writable.

*2: This is not writable when the emergency reset of communication is not cancelled.

*3: The written data is not readable before generation of the IIC communication.

■ Serial interface Clock Cycle Switching Register (SCCKSEL)

bp	7	6	5	4	3	2	1	0
Flag	SCCKSEL 7	SCCKSEL 6	SCCKSEL 5	SCCKSEL 4	-	-	-	-
At reset	0	0	0	0	-	-	-	-
Access	R/W	R/W	R/W	R/W	-	-	-	-

bp	Flag	Description
7-6	SCCKSEL7 SCCKSEL6	Serial 3 clock (fosc) cycle switching 00: fosc 01: fosc/2 10: fosc/4 11: Reserved
5-4	SCCKSEL5 SCCKSEL4	Serial 2 clock (fosc) cycle switching 00: fosc 01: fosc/2 10: fosc/4 11: Reserved
3-0	-	-

Table:14.2.2 Serial 2 clock (fosc) selection

SCCKSEL(bp5)	SCCKSEL(bp5)	SC3PSC2	SC3PSC1	SC3PSC0	
0	0	0	0	0	fosc/2
0	0	0	0	1	fosc/4
0	0	0	1	0	fosc/16
0	0	0	1	1	fosc/32
0	1	0	0	0	fosc/4
0	1	0	0	1	fosc/8
0	1	0	1	0	fosc/32
0	1	0	1	1	fosc/64
1	0	0	0	0	fosc/8
1	0	0	0	1	fosc/16
1	0	0	1	0	fosc/64
1	0	0	1	1	fosc/128

14.3 Operation

Serial interface 3 is used as both clock synchronous /single master IIC serial interface.

14.3.1 Clock Synchronous Serial Interface

■ Activation Factor for Communication

Table:14.3.1 shows the activation source for communication. At master, a transfer clock is generated by setting data to the transfer data buffer TXBUF3, or by enabling start condition. Signals input from SBT3 pin inside serial interface are masked to prevent operating errors by noise, except during communication. This mask is automatically released by setting data to TXBUF3 (access to the TXBUF3 register), or enabling start condition to the data input pin. Therefore, at slave communication, set data to TXBUF3 or input start condition before input external clock.

Wait more than 3.5 transfer clocks before input the external clock after the data set to TXBUF3. This wait time is used for data loading from TXBUF3 to internal shift register.

Table:14.3.1 Synchronous Serial Interface Activation Source

	Activation source	
	Transmission	Reception
Master communication	Set the transmission data	Set dummy data
		Input start condition
Slave communication	Input clock after the transmission data is set	Input clock after dummy data is set
		Input clock after start condition is input

■ Transfer Bit Count Setup

The transfer bit count can be selected from 1 bit to 8 bits. Set the SC3LNG 2 to 0 flag of the SC3MD0 register (at reset : 111). The SC3LNG 2 to 0 flag holds the previous value until other value is set.

The SBT3 pin is masked inside serial interface to prevent operating errors by noise, except during communication. At slave, set data to SC3TRB or input start condition before input clock to the TXBUF3 pin.

Wait more than3.5 transfer clocks before input the external clock after the data set to TXBUF3. Otherwise, normal operation is not guaranteed.

■ Start Condition Setup

Enable or disable of start condition can be selected with the SC3STE flag of the SC3MD0 register.

Start condition is detected when the SC3CE1 flag of the SC3MD0 register is set to "0" and data line SBI3 pin (3 channels) or SBO3 pin (2 channels) changes from "H" to "L" while the clock line (SBT3 pin) is "H". It is also detected when the SC3CE1 flag of the SC3MD0 register is set to "1" and data line SBI3 pin (3 channels) or SBO3 pin (2 channels) changes from "H" to "L" while the clock line (SBT3 pin) is "L".

Set the SC3SB0S flag of the SC3MD1 register to "0" before change the start condition edge.

At the selection of the start condition "enable" and master transmission / reception, after the start condition output, start condition is input from the slave, then data transmission is generated.

■ First Transfer Bit Setup

The SC3DIR flag of the SC3MD0 register sets the first bit to be transferred. LSB or MSB can be selected.

■ Transmission / Reception Data Buffer

The transfer data buffer TXBUF3 is the spare buffer which stores data to be loaded to internal shift register. Set the data to be transferred to transfer data buffer TXBUF3, and the data is automatically loaded to internal shift register. The data loading takes more than 3 clock cycles. Data setting to TXBUF3 again during data loading may not be operated properly. You can determine whether or not data loanding is in progress by monitoring transfer buffer empty flag SC3TEMP of the SC3STR. SC3TEMP flag is set to "1"when data is set to TXBUF3 and cleared to "0" when data loading ends.

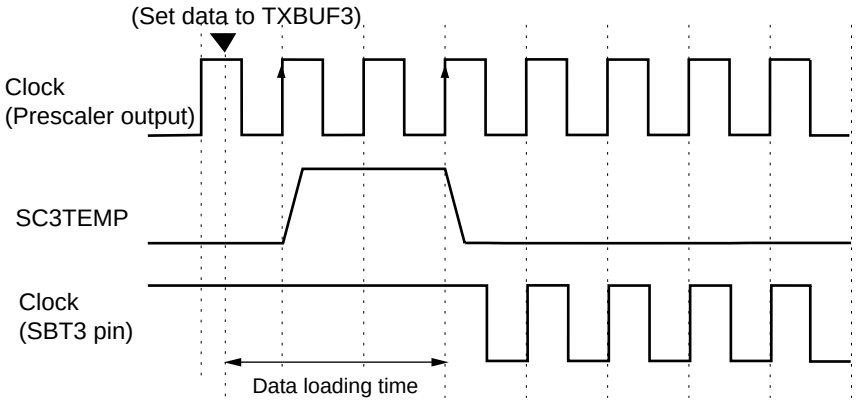


Figure:14.3.1

■ Reception Data Buffer

Use transmission / reception shift register SC3TRB as reception data buffer. The received data is stored to SC3TRB shifting by 1 bit.

If start condition is input for activation during communication again, the transmission data becomes invalid. To transmit the data, set it to TXBUF3 again.

SC3TRB is overwritten in every communication. In sequence reception, read out the data in SC3TRB before the next reception is started.

■ Transmission Bit Count and First Transfer Bit

When the transfer bit count is 1 to 7 bits, data storage to the transmission /reception shift register TXBUF3 depends on the first transfer bit. When MSB is the first bit to be transferred, the lower bits of TXBUF3 are used for storage. In Figure:14.3.2, if data "A" to "F" are stored to bp2 to bp7 of SC3TRB as the transfer bit count is 6 bits, data is transferred from "F" to "A". When LSB is the first bit to be transferred, use the lower bits of TXBUF3 for storage. In Figure:14.3.3, if data "A" to "F" are stored to bp0 to bp5 of TXBUF3, as the transfer bit count is 6 bits, data is transferred from "A" to "F".

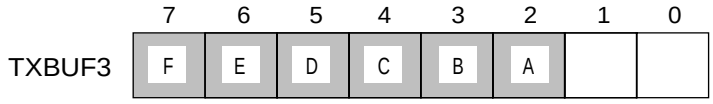


Figure:14.3.2 Transfer Bit Count and First Transfer Bit (MSB First)

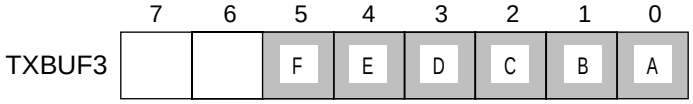


Figure:14.3.3 Transfer Bit Count and First Transfer Bit (LSB First)

■ Receive Bit Count and First Transfer Bit

When the transfer bit count is 1 to 7 bits, data storage to the transmit/receive shift register SC3TRB depends on the first transfer bit. When MSB is the first bit to be transferred, the lower bits of SC3TRB are used for storage. In Figure:14.3.4, as the transfer bit count is 6 bits, data "A" to "F" are stored to bp5 to bp0 of SC3TRB, and they are transferred from "F" to "A". When LSB is the first bit to be transferred, use the upper bits of SC3TRB for storage. In Figure:14.3.5, data "A" to "F" are stored to bp2 to bp7 of SC3TRB, as the transfer bit count is 6 bits, and they are transferred from "A" to "F".

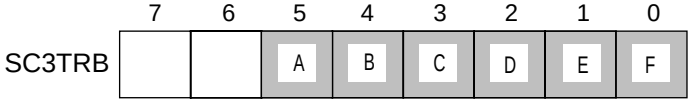


Figure:14.3.4 Receive Bit Count and First Transfer Bit (MSB First)

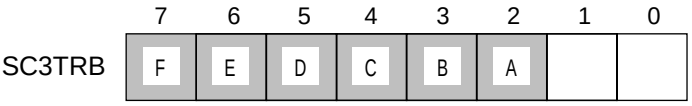


Figure:14.3.5 Receive Bit Count and First Transfer Bit (LSB First)

When the serial transfer bit is set between 1 to 7, the data except for received data of the specified transfer bit count is unknown. Use the received data after being masked by AND/ OR instruction.

■ Continuous Mode

Serial interface 3 is capable of continuous transmission. If data is set to transmission data buffer TXBUF3 during transmission, transmission buffer empty flag SC3TEMP is set and the set data is automatically transmit. Set data to TXBUF3 in the period that after data is loaded to internal shift register and before communication end interrupt SC3IRQ is generated. In master communication, communication blank from SC3IRQ generation to next transfer clock output is 4 transfer clock.

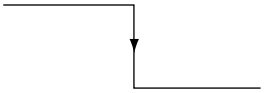
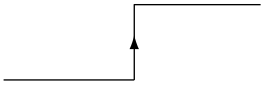
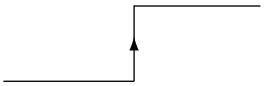
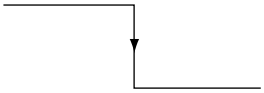
■ Automatic Continuous Transfer by ATC

ATC1, the automatic data transfer function built-in this LSI can activate Serial interface 3. It enables continuous transfer of data up to 255 byte. For activation using ATC1, refer to chapter 18 Automatic Transfer Controller, Transfer mode 8 to 9.

■ Input edge / output edge Setup

The SC3CE1 flag of the SC3MD0 register sets the output edge of the transmission data and the input edge of the received data. Data at transmission is output at the falling edge of clock as the SC3CE1 flag = "0", and at the rising edge of clock as the SC3CE1 = "1". Data at reception is input at the rising edge of clock as the SC3CE1 = "0", and at the falling edge of clock as the SC3CE1 flag = "1"

Table:14.3.2 Input Edge / Output Edge of Transmission and Reception Data

SC3CE1	Transmission data output edge	Received data input edge
0		
1		

■ Clock Setup

Clock source is selected from the dedicated prescaler and timers 3, 5 output (2 channels) with the SC3PSC3 to 0 of the SC3MD3 register. The dedicated prescaler is started by selecting "count enable" with the SC3PSCE of the SC3MD3 register. The SC3MST flag of the SC3MD1 register selects the internal clock (clock master), or the external clock (clock slave). Even if the external clock is selected, set the internal clock with same frequency to the external clock with the SC3MD3 register, as the interrupt flag SC3IRQ is generated by the internal clock. Table:14.3.3 shows the internal clock source which can be set with the SC3MD3 register.

Table:14.3.3 Synchronous Serial Interface Inside Clock Source

	Serial 3
Clock source (Internal clock)	fosc/2
	fosc/4
	fosc/8
	fosc/16
	fosc/32
	fosc/64
	fosc/128
	fs/2
	fs/4
	timer 3 output
	timer 5 output

Set "0" to the SC3SBIS and SC3SBOS flags of the SC3MD register before change the clock setup.

Set transfer clock frequency in slave reception in which start condition is to be smaller than that of the system clock.

■ Switch the used pins

Switch the used pins to A(SBO3A, SBI3A, SBT3A) or B(SBO3B, SBI3B, SBT3B) by SC3SEL flag of SCSEL register.

■ Data Input Pin Setup

There are 2 communication modes to be selected : 3 channels (clock pin(SBT3 pin), data output pin (SBO3 pin), data input pin (SBI3 pin)), 2 channels (clock pin (SBT3 pin), data I/O pin (SBO3 pin)). The SBI3 pin can be used only for serial data input. The SBO3 pin can be used for serial data input and output. The SC3IOM flag of the SC3MD1 register selects either serial data is input from the SBI3 pin, or the SBO3 pin. When "data input from the SBO3 pin" is selected for communication with 2 channels, the P3DIR3 flag of the P3DIR register is used to switch the transmission / reception of the SBO3 pin. The SBI3 pin, not used at that time, can be used as a general port.

Maximum transfer speed should be under 5.0 MHz. If transfer clock exceeds 5.0 MHz, data may not be transferred properly.

In reception, you can use SBI3 pin as general port by setting SC3IOM of the SC3MD1 register to "1" to select "serial data input from SBO3 pin".

■ Transmission Buffer Empty Flag

If any data is set to TXBUF3 during communication (after setting data to TXBUF3 before generating the communication complete interrupt SC3IRQ), the transmission buffer empty flag SC3TEMP of the SC3STR register is set to "1". That indicates that the next transmission data is going to be loaded. Data is loaded to inside shift register from TXBUF3 by generation of SC3TIRQ, and the next transfer is started as SC3TEMP is cleared to "0".

■ BUSY flag

If data is set to the transmission/reception shift register TXBUF3, or start condition is enabled, the busy flag SC3BSY is set. That is cleared to "0" by the generation of the communication end interrupt SC3IRQ. The SC3BSY flag setup is maintained during continuous communication. If transmission buffer empty flag SC3TEMP is "0" when communication end interrupt SC3IRQ is generated, SC3BSY is cleared to "0".

■ Forced Reset

You can shut down the communication by setting both of the SC3SBOS flag and the SC3SBIS flag of the SC3MD1 register to "0" (the SBO3 pin function : port, input data : input "1"). When a forced reset is done, the SC3BSY flag of the SC3MD0 register is cleared, but other control registers hold their set values.

■ Last Bit of Transmission Data

Table:14.3.4 shows last bit data output holding time at transmission, and the minimum data input time of the last bit at reception. At slave, internal clock setup is necessary to reserve data holding time at data transmission.

Table:14.3.4 Last Bit Data Length of Transmission Data

	at transmission Last bit data holding period	at reception Last bit data input period
At master	1 bit data length	1 bit data length (min)
At slave	[1 bit data length of external clock × 1/2]+ [internal clock cycle × (1/2 to 3/2)]	

When start condition is disabled (SC3STE flag=0), SBO3 output after last bit data output hold time can be set with SC3FDC1-0 of the SC3MD3 register as shown in Table:14.3.5.

After reset release, output before serial transfer is "H" regardless of the set value of SC3FDC1-0 flags. When start condition is enabled (SC3STE flag =1), "H" is output regardless of the set value of SC3FDC1-0 flags.

Table:14.3.5 SBO3 Output after Last Bit Data Output Hold Time (without start condition)

SC3FDC1 flag	SC3FDC0 flag	SBO3 output after last bit data output hold time
0	0	Fixed to "1"(High) output
1	0	Fixed to "0"(Low) output
0	1	Hold last data
1	1	Reserved

■ Transmission Timing

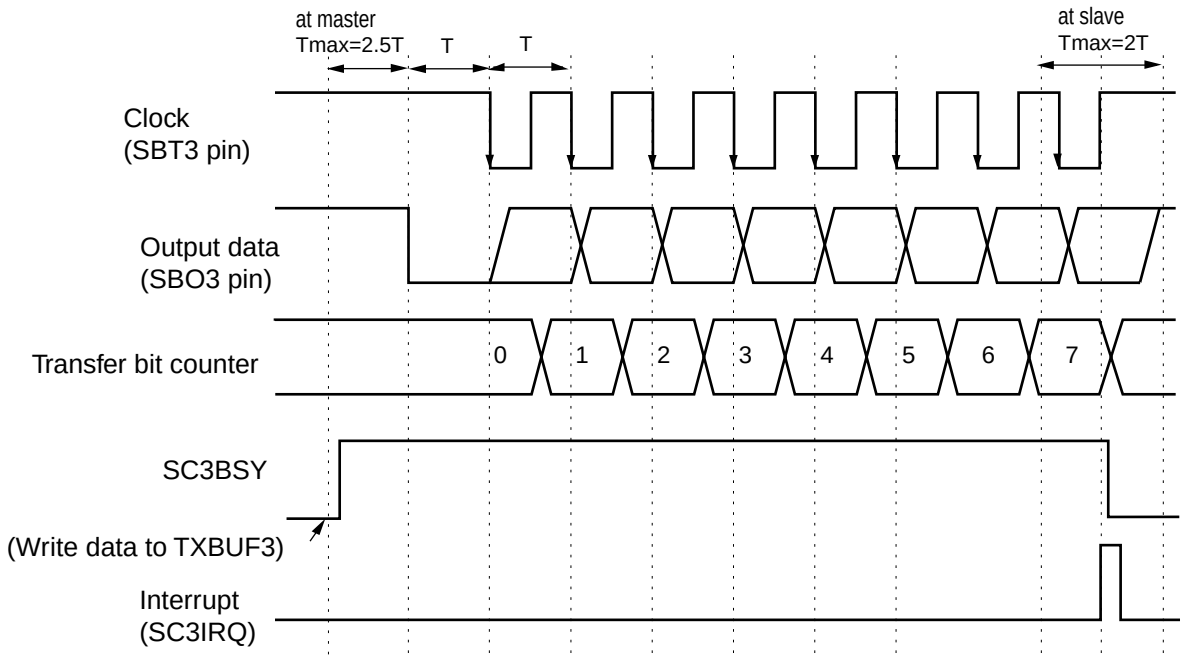


Figure:14.3.6 Transmission Timing (Falling edge, Start condition is enabled)

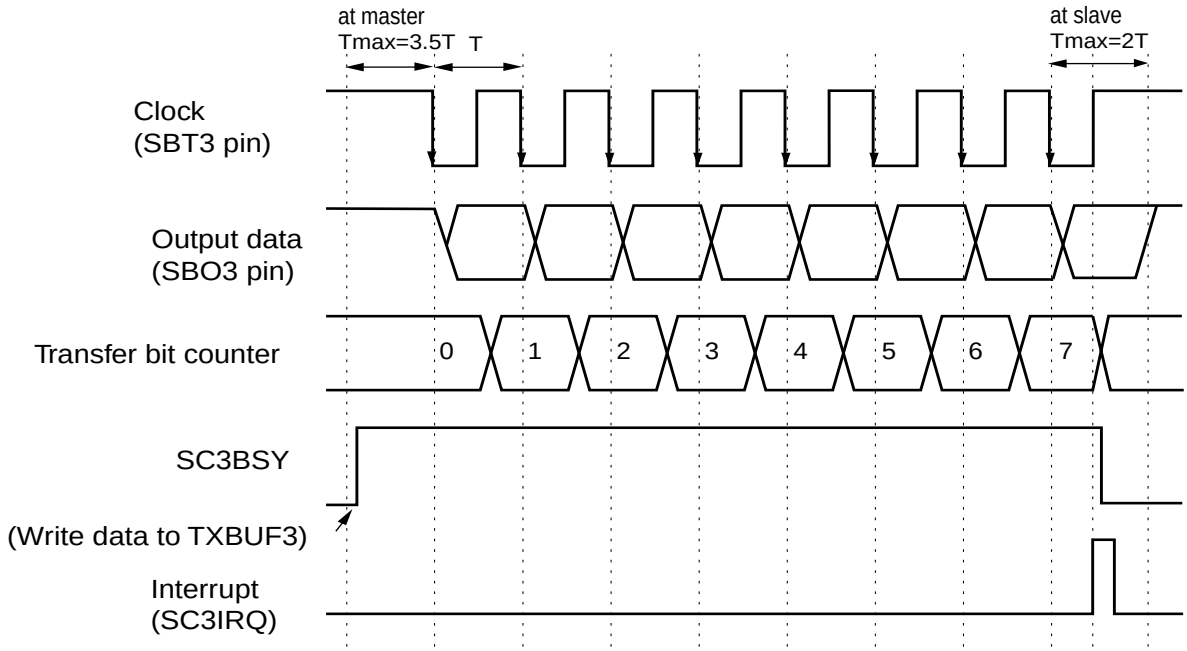


Figure:14.3.7 Transmission Timing (Falling edge, Start condition is disabled)

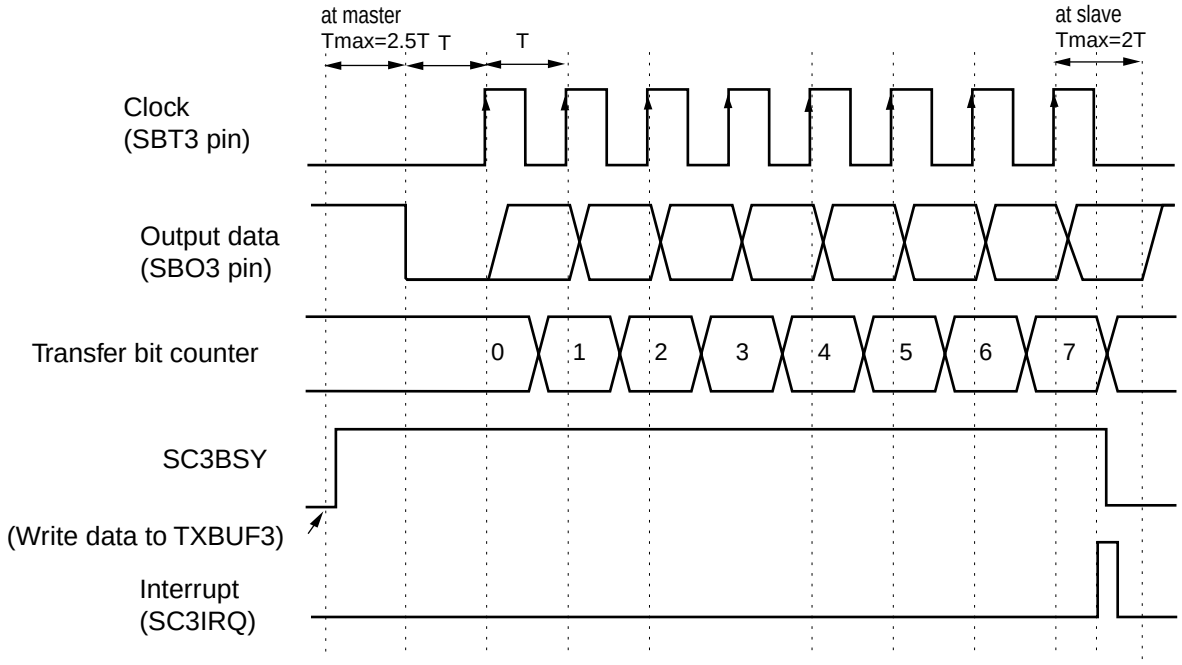


Figure:14.3.8 Transmission Timing (Rising edge, Start condition is enabled)

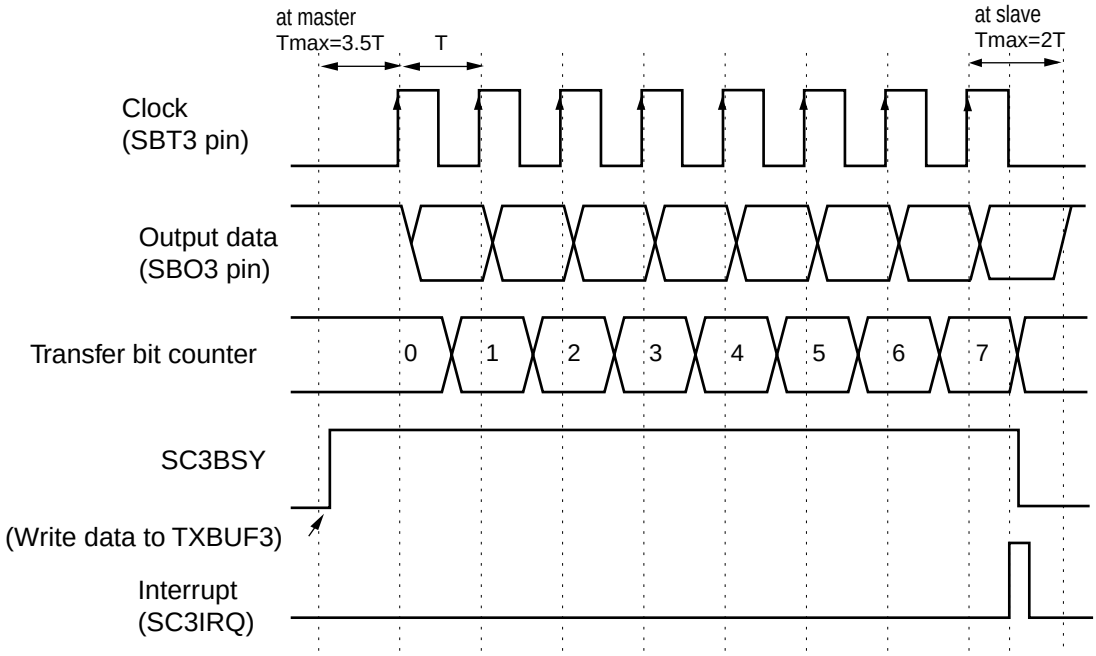


Figure:14.3.9 Transmission Timing (Rising edge, Start condition is disabled)

■ Reception Timing

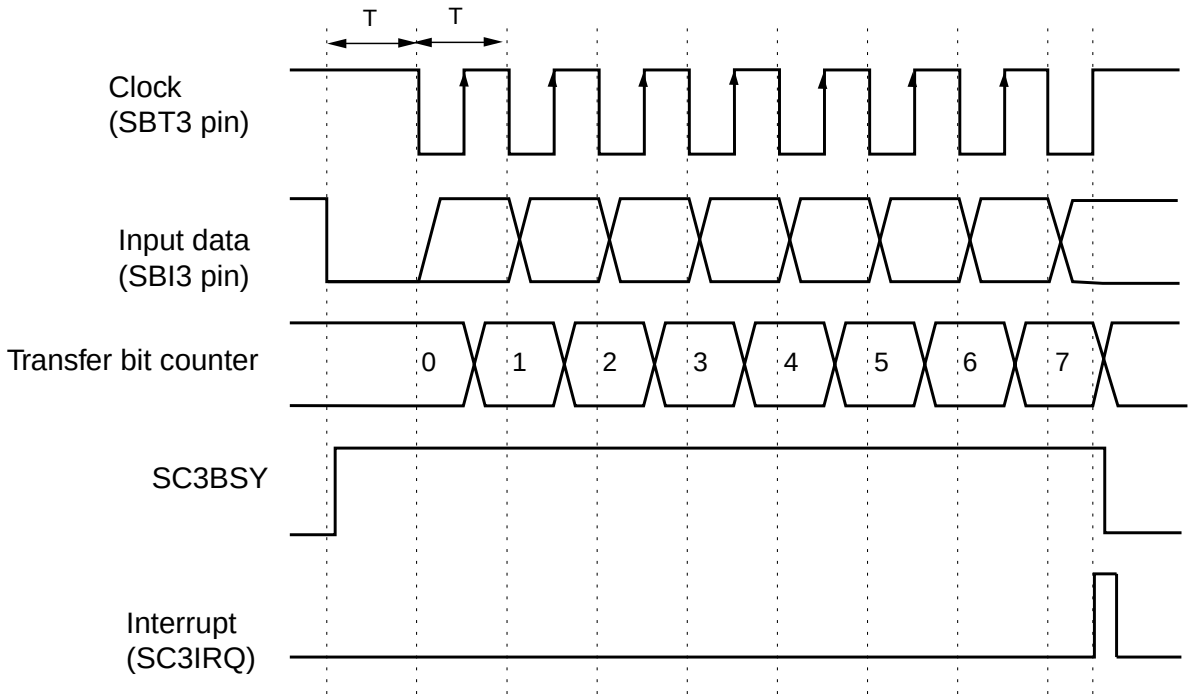


Figure:14.3.10 Reception Timing (Rising edge, Start condition is enabled)

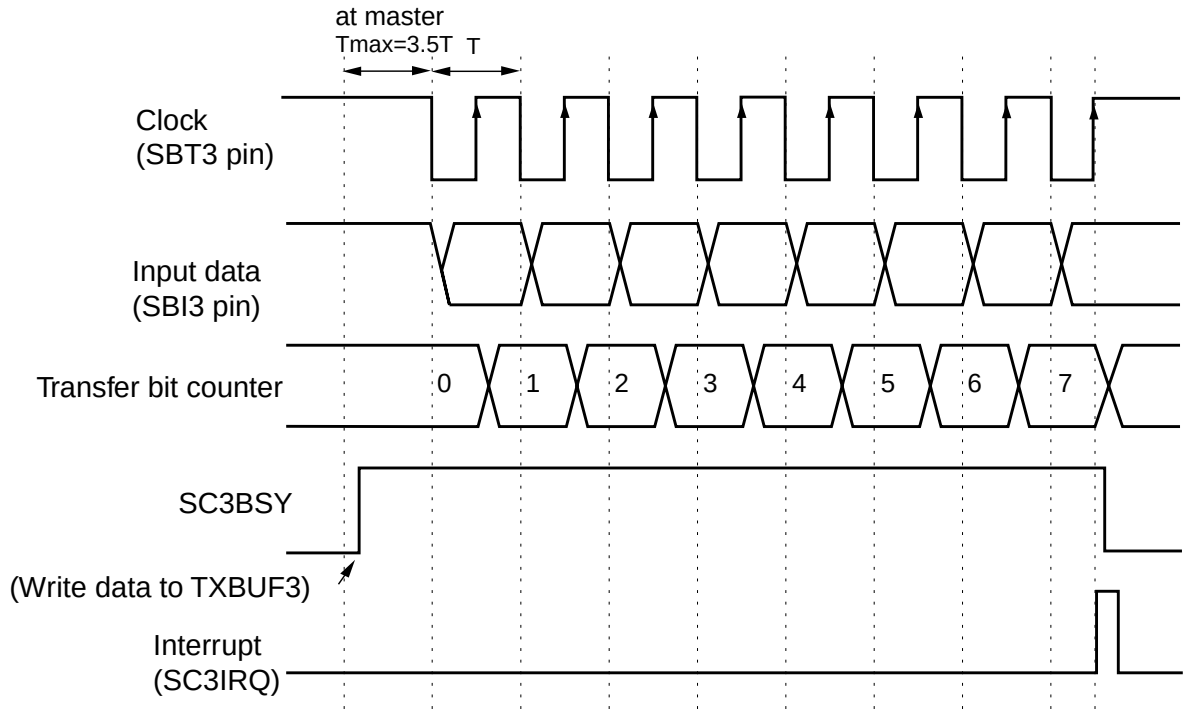


Figure:14.3.11 Reception Timing (Rising edge, Start condition is disabled)

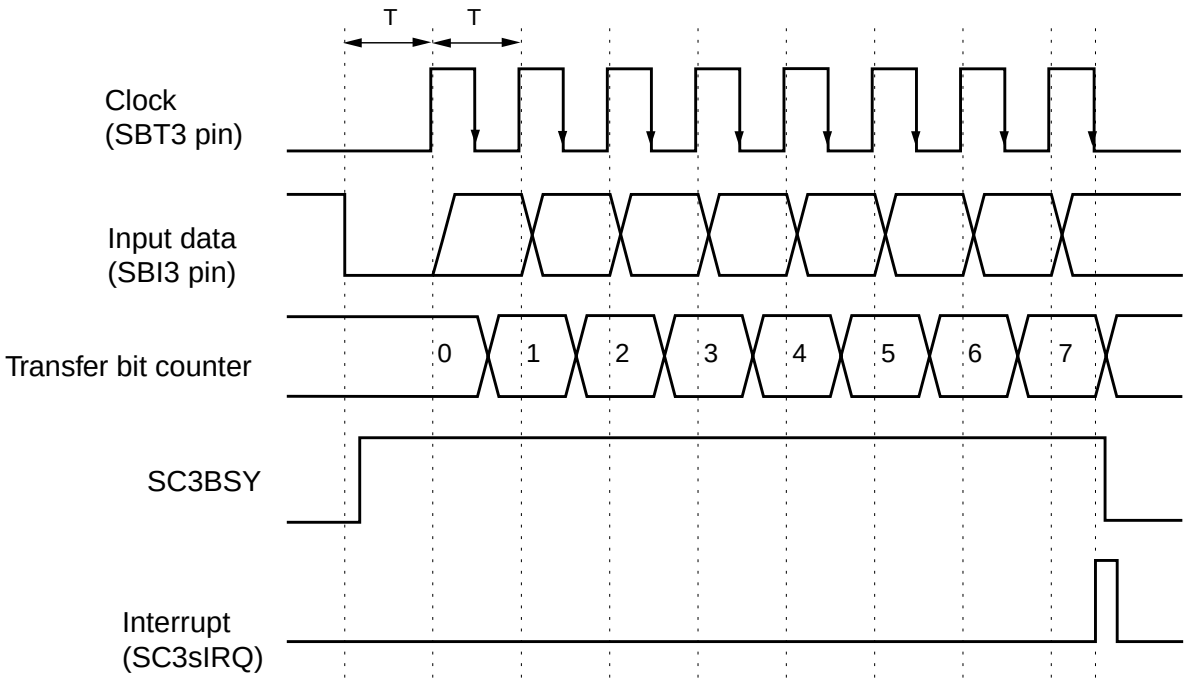


Figure:14.3.12 Reception Timing (Falling edge, Start condition is enabled)

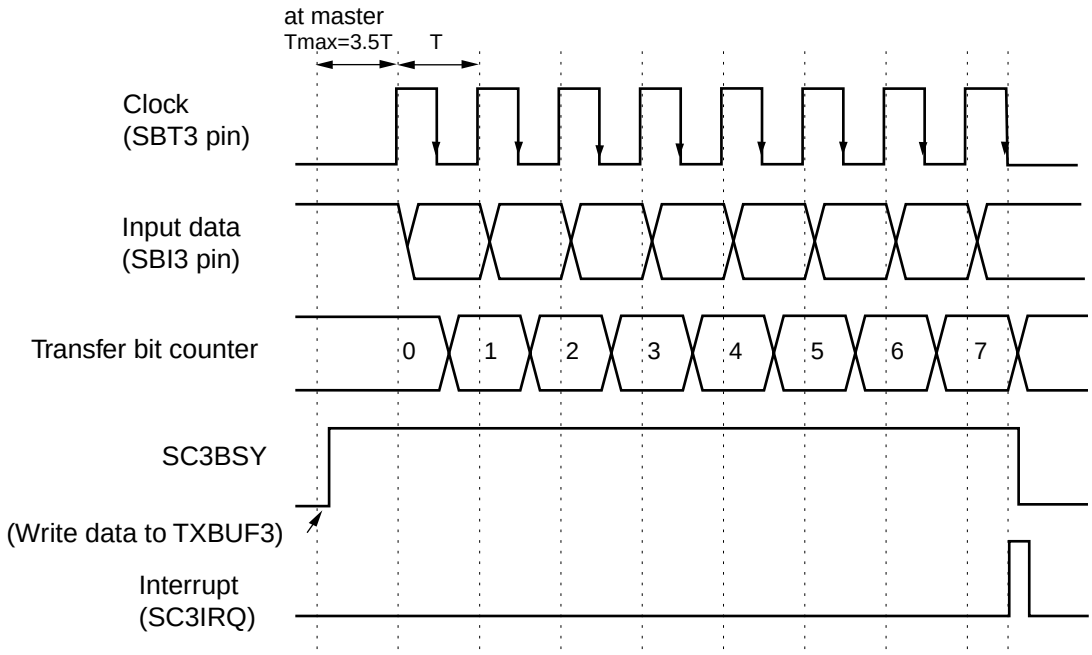


Figure:14.3.13 Reception Timing (Falling edge, Start condition is disabled)

■ Transmission / Reception

To operate transmission and reception at the same time, set the SC3CE1 flag of the SC3MD0 register to "0" or "1". As data is recieved at the opposite edge of the transmission clock, set the polarity of reception data input edge to opposite polarity of the transmission data output edge.

On the transmission / reception at the start condition enable, transmitter / receiver should transmit / receive at the start condition enable.

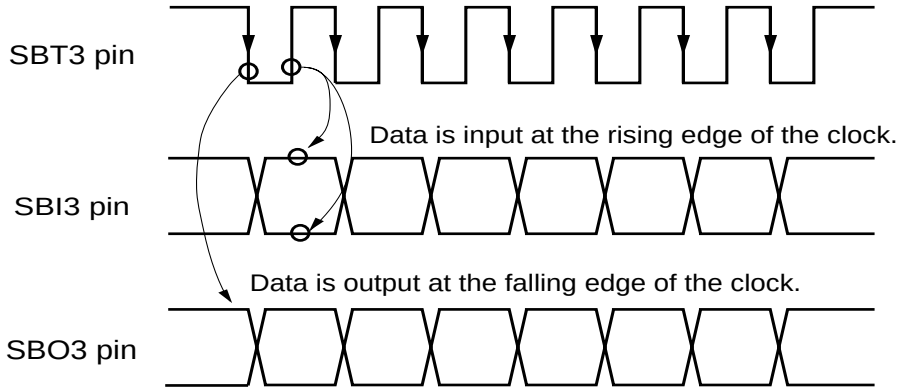


Figure:14.3.14 Transmission / Reception Timing (Reception : Rising edge, Transmission : Falling edge)

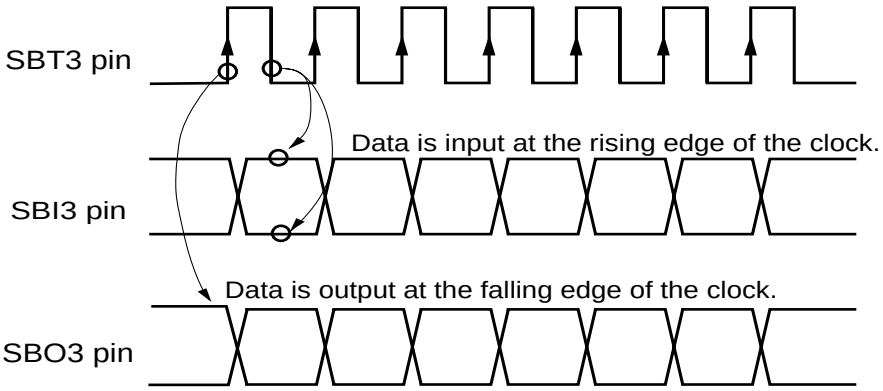


Figure:14.3.15 Transmission / Reception Timing (Reception : Falling edge, Transmission : Rising edge)

■ Communication in STANDBY mode

This serial interface is capable of slave reception in STANDBY mode. You can return the CPU operation from STANDBY mode to NORMAL mode using communication end interrupt SC3IRQ, which is generated after the slave reception.

(In STANDBY mode, continuous reception is desabled after data of transfer bit count set by SC3LNG2-0 flags of the SC3MD0 register is received. Read out the received data from transmission/reception shift register SC3TRB after returning to NORMAL mode.)

In STANDBY mode, reception with start condition is not available, thus, disable start condition. And set dummy data to tramsmission data buffer TXBUF3 before transition to STANDBY mode.

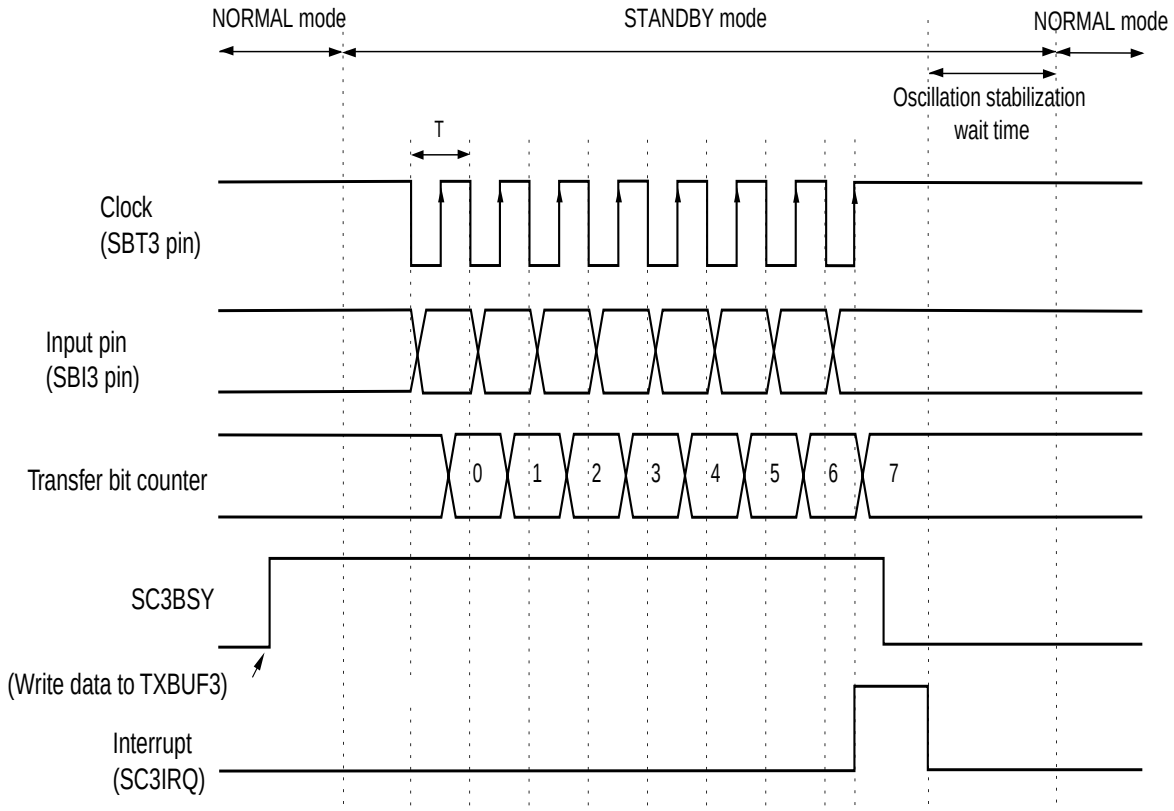


Figure:14.3.16 Reception Timing (Rising edge, Start condition is disabled)

■ Pins Setup (3 channels, at transmission)

Table:14.3.6 shows the pins setup at synchronous serial interface transmission with 3 channels (SBO3 pin, SBI3 pin, SBT3 pin).

Table:14.3.6 Synchronous Serial Interface Pins Setup (3 channels, at transmission)

Item	Data output pin	Data input pin	Clock I/O pin	
	SBO3A pin / SBO3B pin	SBI3A pin / SBI3B pin	SBT3A pin / SBT3B pin	
			Clock master	Clock slave
			SC3MD1(SC3MST)	
Pin	P33 / P93	P34 / P94	P35 / P95	
Port pin selection	Select the used pin (A, B)			
	SCSEL(SC3SEL)			
SBI3 / SBO3 pin selection	SBI3 / SBO3 independent		-	
	SC3MD1(SC3IOM)			
Function	Serial data output	"1" input	Transfer clock I/O	Transfer clock I/O
	SC3MD1(SC3SBOS)	SC3MD1(SC3SBIS)	SC3MD1(SC3SBTS)	
Type	Push-pull/N-ch open-drain	-	Push-pull/N-ch open-drain	Push-pull/N-ch open-drain
	P3ODC(P3ODC3) / P9ODC(P9ODC3)		P3ODC(P3ODC5) / P9ODC(P9ODC5)	
I/O	Output mode	-	Output mode	Input mode
	P3DIR(P3DIR3) / P9DIR(P9DIR3)		P3DIR(P3DIR5) / P9DIR(P9DIR5)	
Pull-up	added / not added	-	added / not added	added / not added
	P3PLU(P3PLU3) / P9PLU(P9PLU3)		P3PLU(P3PLU5) / P9PLU(P9PLU5)	

■ Pins Setup (3 channels, at reception)

Table:14.3.7 shows the pins setup at synchronous serial interface reception with 3 channels (SBO3 pin, SBI3 pin, SBT3 pin).

Table:14.3.7 Synchronous Serial Interface Pins Setup (3 channels, at reception)

Item	Data output pin	Data input pin	Clock I/O pin	
	SBO3A pin / SBO3B pin	SBI3A pin / SBI3B pin	SBT3A pin / SBT3B pin	
			Clock master	Clock slave
			SC3MD1(SC3MST)	
Pin	P33 / P93	P34 / P94	P35 / P95	
Port pin selection	Select the used pin (A, B)			
	SCSEL(SC3SEL)			
SBI3 / SBO3 pin selection	SBI3 / SBO3 independent		-	
	SC3MD1(SC3IOM)			
Function	Port	Serial data input	Transfer clock I/O	Transfer clock I/O
	SC3MD1(SC3SBOS)	SC3MD1(SC3SBIS)	SC3MD1(SC3SBTS)	
Type	-	-	Push-pull/N-ch open-drain	Push-pull/N-ch open-drain
			P3ODC(P3ODC5) / P9ODC(P9ODC5)	
I/O	-	Input mode	Output mode	Input mode
		P3DIR(P3DIR4) / P9DIR(P9DIR4)	P3DIR(P3DIR5) / P9DIR(P9DIR5)	
Pull-up	-	-	added / not added	added / not added
			P3PLU(P3PLU5) / P9PLU(P9PLU5)	

■ Pins Setup (3 channels, at reception / transmission)

Table:14.3.8 Synchronous Serial Interface Pins Setup (3 channels, at transmission / reception)

Item	Data output pin	Data input pin	Clock I/O pin	
	SBO3A pin / SBO3B pin	SBI3A pin / SBI3B pin	SBT3A pin / SBT3B pin	
			Clock master	Clock slave
			SC3MD1(SC3MST)	
Pin	P33 / P93	P34 / P94	P35 / P95	
Port pin selection	Select the used pin (A, B)			
	SCSEL(SC3SEL)			
SBI3 / SBO3 pin selection	SBI3 / SBO3 independent		-	
	SC3MD1(SC3IOM)			
Function	Serial data output	Serial data input	Transfer clock I/O	Transfer clock I/O
	SC3MD1(SC3SBOS)	SC3MD1(SC3SBIS)	SC3MD1(SC3SBTS)	
Type	Push-pull/N-ch open-drain	-	Push-pull/N-ch open-drain	Push-pull/N-ch open-drain
	P3ODC(P3ODC3) / P9ODC(P9ODC3)		P3ODC(P3ODC5) / P9ODC(P9ODC5)	
I/O	Output mode	Input mode	Output mode	Input mode
	P3DIR(P3DIR3) / P9DIR(P9DIR3)	P3DIR(P3DIR4) / P9DIR(P9DIR4)	P3DIR(P3DIR5) / P9DIR(P9DIR5)	
Pull-up	added / not added	-	added / not added	added / not added
	P3PLU(P3PLU3) / P9PLU(P9PLU3)		P3PLU(P3PLU5) / P9PLU(P9PLU5)	

■ Pins Setup (2 channels, at transmission)

Table:14.3.9 shows the pins setup at synchronous serial interface transmission with 2 channels (SBO3pin, SBT3 pin). The SBI3 pin is not used, so that it can be used as a general port.

Table:14.3.9 Synchronous Serial Interface Pins Setup (2 channels, at transmission)

Item	Data output pin	Data input pin	Clock I/O pin	
	SBO3A pin / SBO3B pin	SBI3A pin / SBI3B pin	SBT3A pin / SBT3B pin	
			Clock master	Clock slave
			SC3MD1(SC3MST)	
Pin	P33 / P93	P34 / P94	P35 / P95	
Port pin selection	Select the used pin (A, B)			
	SCSEL(SC3SEL)			
SBI3 / SBO3 pin selection	SBI3 / SBO3 independent		-	
	SC3MD1(SC3IOM)			
Function	Serial data output	"1" input	Transfer clock I/O	Transfer clock I/O
	SC3MD1(SC3SBOS)	SC3MD1(SC3SBIS)	SC3MD1(SC3SBIS)	
Type	Push-pull/N-ch open-drain	-	Push-pull/N-ch open-drain	Push-pull/N-ch open-drain
	P3ODC(P3ODC3) P9ODC(P9ODC3)		P3ODC(P3ODC5) / P9ODC(P9ODC5)	
I/O	Output mode	-	Output mode	Input mode
	P3DIR(P3DIR3) P9DIR(P9DIR3)		P3DIR(P3DIR5) / P9DIR(P9DIR5)	
Pull-up	added / not added	-	added / not added	added / not added
	P3PLU(P3PLU3) / P9PLU(P9PLU3)		P3PLU(P3PLU5) / P9PLU(P9PLU5)	

■ Pins Setup (2 channels, at reception)

Table:14.3.10 shows the pins setup at synchronous serial interface reception with 2 channels (SBO3 pin, SBT3 pin). The SBI3 pin is not used, so that it can be used as a general port.

Table:14.3.10 Synchronous Serial Interface Pins Setup (2 channels, at reception)

Item	Data output pin	Data input pin	Clock I/O pin	
	SBO3A pin / SBO3B pin	SBI3A pin / SBI3B pin	SBT3A pin / SBT3B pin	
			Clock master	Clock slave
			SC3MD1(SC3MST)	
Pin	P33 / P93	P34 / P94	P35 / P95	
Port pin selection	Select the used pin (A, B)			
	SCSEL(SC3SEL)			
SBI3 / SBO3 pin selection	SBI3 / SBO3 independent		-	
	SC3MD1(SC3IOM)			
Function	Port	Serial input	Transfer clock I/O	Transfer clock I/O
	SC3MD1(SC3SBOS)	SC3MD1(SC3SBIS)	SC3MD1(SC3SBIS)	
Type	-	-	Push-pull/N-ch open-drain	Push-pull/N-ch open-drain
			P3ODC(P3ODC5)	
I/O	Input mode	-	Output mode	Input mode
	P3DIR(P3DIR3) / P9DIR(P9DIR3)		P3DIR(P3DIR5) / P9DIR(P9DIR5)	
Pull-up	-	-	added / not added	added / not added
			P3PLU(P3PLU5) / P9PLU(P9PLU5)	

14.3.2 Setup Example

■ Transmission / Reception Setup Example

Here is the setup example at transmission/reception with serial interface 3.Table:14.3.11 shows the conditions.

Table:14.3.11 Conditions for Synchronous Serial Interface at transmission / reception

Item	set to
SBI3 / SBO2 pin selection	Independent (3 channels)
Transfer bit count	8 bits
Start condition	Disabled
First bit to be transferred	MSB
Input clock edge	Falling
Output clock edge	Rising
Clock	Clock master
Clock source	fs/2
Used pins selection	A (port 3)
SBT3/SB02 pin type	N-ch open-drain
SBT3 pull-up resistor	Added
SB02 pull-up resistor	Added
Serial interface 3 communication end interrupt	Enabled

An example setup procedure, with a description of each step is shown below.

Setup Procedure	Description
(1) Select prescaler operation. SC3MD3 (0x03FA6) bp3 :SC3PSCE =1	(1) Set the SC3PSCE flag of the SC3MD3 register to "1" to select prescaler operation.
(2) Select the clock source. SC3MD3 (0x03FA6) bp2-0 :SC3PSC2-0 =100	(2) Set the SC3PSC2-0 flag of the SC3MD3 register to "100" to select fs/2 for clock source.
(3) Select the used pins. SCSEL (0x03F4F) bp3 :SC3SEL =0	(3) Set the SC3SEL flag of SCSEL register to “0“ to select I/O pin to A(port 3)
(4) Control of pin type. P3ODC (0x03F2C) bp5, 3 :P3ODC5, 3 =1,1 P3PLU (0x03F49) bp5, 3 :P3PLU5, 3 =1,1	(4) Set the P3ODC5, P3ODC3 flags of the P3ODC register to "1, 1" to select N-ch open drain for the SBO3/SBT3 pin type. Set the P3ODC5, P3ODC3 flags of the P3PLU register to "1, 1" to add pull-up resistor.

Setup Procedure	Description
(5) Control of pin direction. P3DIR (0x03F33) bp5-3 :P3DIR5-3 =101	(5) Set the P3DIR5, P3DIR3 flags of the Port 0 pin control direction register (P3DIR) to "1, 1" and set P3DIR4 to "101" to set P35, P33 to output mode, to set P34 to input mode.
(6) Set the SC3MD0 register. Select the transfer bit count. SC3MD0 (0x03FA8) bp2-0 :SC3LNG2-0 =111 Select the start condition. SC3MD0 (0x03FA8) bp3 :SC3STE =0 Select the first bit to be transferred. SC3MD0 (0x03FA4) bp4 :SC3DIR =0 Select the transfer edge. SC3MD0 (0x03FA8) bp6 :SC3CE1 =1	(6) Set the SC3LNG2-0 flag of the serial 3 mode register (SC3MD0) to "111" to set the transfer bit count to 8 bits. Set the SC3STE flag of the SC3MD0 register to "0" to disable start condition. Set the SC3DIR flag of the SC3MD0 register to "0" to set MSB as the first transfer bit. Set the SC3CE1 flag of the SC3MD0 register to "1" to set the transmission data output edge to "rising", and the received data input edge to "falling".
(7) Set the SC3CTR register. SC3CTR (0x03FAA) bp2 :SC3CMD =0	(7) Set the SC3CMD flag of the SC3CTR register to "0" to select serial data tansmission.
(8) Set the SC3MD1 register. Select the transfer clock. SC3MD1 (0x03FA9) bp2 :SC3MST =1 Control of pin function. SC3MD1 (0x03FA5) bp4 :SC3SBOS =1 bp5 :SC3SBIS =1 bp6 :SC3SBTS =1 bp7 :SC3IOM =0	(8) Set the SC3MST flag of the SC3MD1 register to "1" to select clock master (internal clock). Set the SC3SBOS, SC3SBIS, SC3SBTS flags of the SC3MD1 register to "1" to set the SBO3 pin to serial data output, the SBI3 pin to serial data input, and the SBT3 pin to serial clock I/O. Set the SC3IOM flag to "0" to set "serial data input from the SBI3 pin".
(9) Set the interrupt level. SC3ICR (0x03FF7) bp7-6 :SC3LV1-0 =10	(9) Set the interrupt level by the SC3LV1-0 flag of the serial 3 interrupt control register (SC3ICR).
(10) Enable the interrupt. SC3ICR (0x03FF7) bp1 :SC3IE =1	(10) Enable the interrupt to by setting "1" to the SC3IE flag of the SC3ICR register. If the interrupt request flag (SC3IR of the SC3ICR register) is already set, clear SC3IR before enable interrupt.
(11) Start serial transmission. Transmission data → TXBUF3 (0x03FA8) Reception data → Input to SBI3 pin	(11) Set the transmission data to the serial transmission data buffer TXBUF3. The internal clock is generated to start transmission/reception. After communication ends, the serial 3 interrupt SC3IRQ is generated.

Note : Procedures (1) to (2), (6), (7) and (8) can be set at once.

Note : Procedures (9) and (10) can be set at once.

For communication with 3 channels, set the SC3BIS of the SC3MD1 register to "0" to set the serial input to "1". The SBI3 pin can be used as a general port. For reception only, set the SC3SBOS of the SC3MD1 register to "0" to select port. The SBO3 pin can be used as a general port.

For communication with 2 channels, set the SBO3 pin to serial data I/O. The port direction control register P3DIR switches the I/O. For reception, set the SC3SBIS of the SC3MD1 register to "1" to select serial input. The SBO3 pin can be used as a general port.

You can shut down the communication by setting the SC3SBOS and the SC3SBIS of the SC3MD1 register to "0".

Set each flag in order of the setup procedures. Set all the control registers (refer to Table:14.2.1, except TXBUF3) before start communication.

Set the transfer rate of the transfer clock to under 5.0 MHz with the SC3MD3 register.

■ Transmission / Reception Setup Example (reception in STANDBY mode)

Here is the setup example at transmission/reception in STANDBY mode using serial interface 3. Table:14.3.12 shows the conditions.

Table:14.3.12 Conditions for Synchronous Serial Interface at transmission / reception (reception in STANDBY mode)

Item	set to
SBI3 / SBO3 pin selection	Connect (2 channels)
Transfer bit count	8 bit
Start condition	Disabled
First bit to be transfered	MSB
Input clock edge	Falling
Clock	Clock slave
Operation mode	STOP mode
Clock source	fs/2
Used pins selection	A (port3)
SBT3/SB03 pin type	Push-pull
SBT3 pull-up resistor	Not added
SBI3 pull-up resistor	Not added
Serial interface 3 communication end interrupt	Enabled

An example setup procedure, with a description of each step is shown below.

Setup Procedure	Description
(1) Prescaler operation selection. SC3MD3 (0x03FA6) bp3 :SC3PSCE =1	(1) Set the SC3PSCE flag of the SC3MD3 register to "1" to select prescaler operation.
(2) Clock source selection. SC3MD3 (0x03FA6) bp2-0 :SC3PSC2-0 =100	(2) Set the SC3PSC2-0 flag of the SC3MD3 register to "100" to select fs/2 for clock source.
(3) Used pins selection. SC3MD3 (0x03F4F) bp3 :SC3SEL =0	(3) Set the SC3PSC2-0 flag of the SC3MD3 register to "100" to select fs/2 for clock source.
(4) Control of pin type. P3ODC (0x03F2C) bp5, 3 :P3ODC5, 3 =0, 0 P3PLU(0x03F43) bp5, 3 :P3PLU5, 3 =0, 0	(4) Set the P3ODC5, P3ODC3 flags of the P3ODC register to "0, 0" to select push-pull for the SBO3/SBT3 pin type. Set the P3PLU5, P3PLU3 flags of the P3PLU register to "0,0" not to add pull-up registor.

Setup Procedure	Description
(5) Control of pin direction. P3DIR (0x03F33) bp5, 3 :P3DIR5, 3 =0, 0	(5) Set the P3DIR5, P3DIR3 flags of the Port 0 pin control direction register (P3DIR) to "0, 0" and set to "0" to set P35, P33 to input mode.
(6) Transfer bit count selection. SC3MD0 (0x03FA4) bp2-0 :SC3LNG2-0 =111	(6) Set the SC3LNG2-0 flags of the serial 3 mode register (SC3MD0) to "111" to set the transfer bit count to 8 bits
(7) Start condition selection. SC3MD0 (0x03FA4) bp3 :SC3STE =0	(7) Set the SC3STE flag of the SC3MD0 register to "0" to disable start condition.
(8) Select the first bit to be transferred. SC3MD0 (0x03FA4) bp4 :SC3DIR =0	(8) Set the SC3DIR flag of the SC3MD0 register to "0" to set MSB as the first transfer bit.
(9) Select the transfer edge. SC3MD0 (0x03FA4) bp6 :SC3CE1 =1	(9) Set the SC3CE1 flag of the SC3MD0 register to "1" to set the reception data input edge to "falling".
(10) Select the communication type. SC3CTR (0x03FAA) bp2 :SC3CMD =0	(10) Set the SC3CMD flag of the SC3CTR register to "0" to select synchronous serial interface.
(11) Select the transfer clock. SC3MD1 (0x03FA5) bp2 :SC3MST =0	(11) Set the SC3MST flag of the SC3MD1 register to "0" to select clock slave (external clock).
(12) Control of pin function. SC3MD1(0x03FA5) bp4 :SC3SBOS =0 bp5 :SC3SBIS =1 bp6 :SC3SBTS =1 bp7 :SC3IOM =0	(12) Set the SC3SBOS flag of the SC3MD1 register to “0“ and the SC3SBIS and theSC3SBTS flags of the SC3MD1 register to "1" to set the SBO3 pin to general port, the SBI3 pin to serial data input, and the SBT3 pin to transfer clock I/O. Set the SC3IOM flag to "0" to set "serial data input from the SBI3 pin".
(13) Set the interrupt level SC3ICR (0x03FF7) bp7-6 :SC3LV1-0 =10	(13) Set the interrupt level (to level 2) by the SC3LV1-0 flags of the serial 2 interrupt control register (SC3ICR).
(14) Enable the interrupt. SC3ICR (0x03FF7) bp1 :SC3IE1-0 =10	(14) Enable the interrupt by setting "1" to the SC3IE flag of the SC3ICR register. If the interrupt request flag (SC3IR of the SC3ICR register) is already set, clear SC3IR before the interrupt is enabled. [Chapter 3 3.1.4. Interrupt Flag Setup]
(15) Set the activation source of serial communication. Dummy data → TXBUF3 (0x03FA9)	(15) Set dummy data to the serial transmission data buffer TXBUF3.
(16) Transition to STOP mode. CPUM (0x03F00) bp3:STOP =1	(16) Set the STOP flag of the CPUM register to "1" for transition to STOP mode.

Setup Procedure	Description
(17) Start serial reception. Transfer clock → Input to SBT3 pin Reception data → Input to SBI3 pin	(17) Set the transfer clock to SBT3 pin and transfer data to SBI3 pin.
(18) Return from STANDBY mode	(18) Serial 3 interrupt is generated at the same time with reception of 8 bits data, and then CPU returns from STOP mode to NORMAL mode after oscillation stabilization wait time.

Note : Procedures (6) - (9), (11) - (12), and (13) to (14) can be set at once.

For slave reception in STANDBY mode, disable the start condition. With other setup, normal reception is not guaranteed.

Set each flag in order of the setup procedures. Set all the control registers (refer toTable:14.2.1, except TXBUF3) before start communication.

14.3.3 Single Master IIC Serial Interface

Serial interface 3 is capable of IIC serial communication in single master. Communication of this IIC interface is based on the IIC-BUS data transfer format of Philips. Table:14.3.13 shows the functions of IIC serial interface.

Table:14.3.13 IIC Serial Interface Functions

Communication type	Single master IIC
Interrupt	SC3IRQ
Pins	SDA3,SCL3
Transfer bit count	1 to 8 bit
First transfer bit	O
ACK bit	O
ACK bit level	O
Clock source	fosc/2 fosc/4 fosc/8 fosc/16 fosc/32 fosc/64 fosc/128 fs/2 fs/4 timer 3 output timer 5 output
The transfer rate is the clock source divided by 8.	

■ Activation factor for Communication

Set data (at transmission) or dummy data (at reception) to the transmission/reception shift register TXBUF3. Start condition and transfer clock are generated to start communication, regardless of transmission/reception. This serial interface can not be used for slave communication.

■ Start Condition Setup

In IIC communication, enable start condition by the SC3STE flag of the SC3MD0 register at the first communication after reset release. From the second communication, the SC3STE flag of the SC3MD0 register can select if start condition is enabled or not.

If start condition is detected during data communication in which the start condition is enabled, the SC3STC flag of the SC3CTR register is set to "1", and the communication end interrupt SC3IRQ is generated to end the transmission. This means that the communication is not executed properly and needs to be re-executed. Clear the SC3STC flag by program. When data line (SDA3 pin) is changed from "H" to "L" while clock line (the SCL3 pin) is "H", start condition is generated.

■ Generation of Stop Condition

Stop condition is generated as the SDA3 line is changed from "L" to "H", while the SCL3 line is "H". Stop condition can be generated by setting the IICSTPC flag of the SC3CTR register to "0" by program.

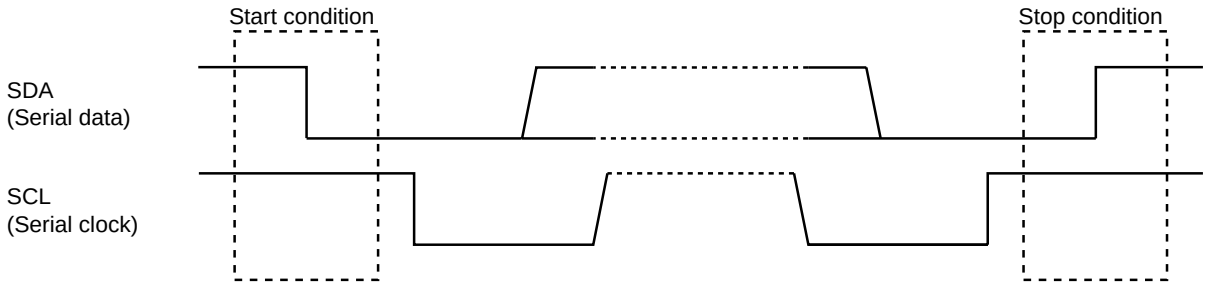


Figure:14.3.17 Start Condition and Stop Condition

■ Input Edge/Output Edge Setup

In IIC communication, data is always received at the falling edge of the clock. Even if the SC3CE1 flag is set to "0", the received data is stored in the falling edge of the clock.

■ Switch the used pin

Switch the used pins to A(SDA3A, SCL3A) or B(SDA3B, SCL3B) by SC3SEL flag of SCSEL register.

■ Data I/O Pin Setup

The SDA3 pin (used as SBO3 pin, too) is used to input/output data. Set the SC3IOM flag of the SC3MD1 register to "1" to input serial data from the SBO3 pin. As the SBI3 pin is not used at that time, it can be used as a general port. But always set the SC3SBIS flag of the above register to "1" to set "input serial data".

To detect start condition, set the SC3SBIS flag of the SC3MD1 register to "input serial data", regardless of transmission/reception.

■ Reception of Confirming (ACK) Bit after Data Transmission

The SC3ACKS flag of the SC3CTR register selects if ACK bit is enabled or not. If ACK bit is enabled, ACK bit is received from the slave station after data (1 to 8 bits) is transferred. At reception of ACK bit, the SDA3 line is automatically released. To receive ACK bit, 1 clock is output to store ACK bit to the SC3ACK0 of the SC3CTR register. The transmission/reception shift register SC3TRB is not operated by the ACK bit reception clock. When the received ACK bit level is "L", the reception is normal at slave and the next data can be received. If the level is "H", the reception maybe completed at slave, so set the IICSTPC flag of the SC3CTR register to "0" to end communication.

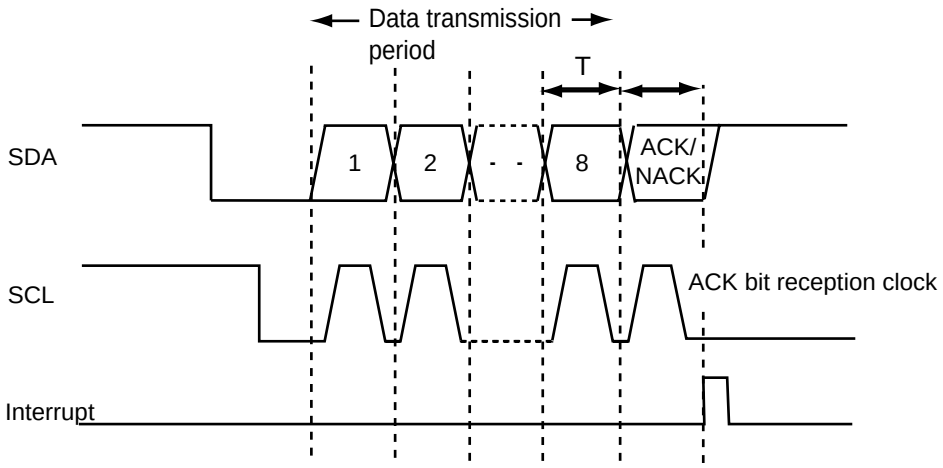


Figure:14.3.18 ACK Bit Reception Timing after Transmission of 8-Bit Data

■ Transmission of Confirming (ACK Bit) of Data Reception

Selection of enable/disable of ACK bit is same with at the transmission. When ACK bit is enabled, ACK bit and clock are output after data (1 to 8 bits) is received. When the reception is continued, ACK bit outputs "L". And when the reception is finished, it outputs "H". The SC3ACK0 of the SC3CTR register sets the output ACK bit level.

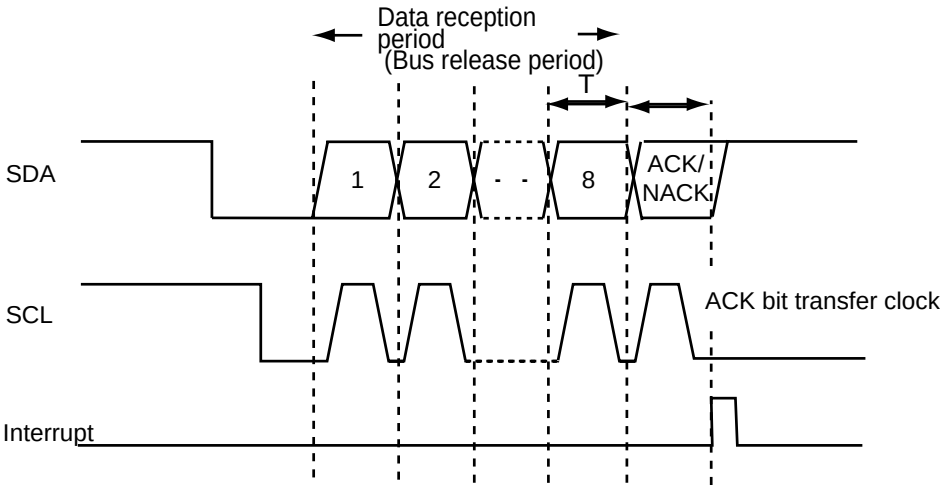


Figure:14.3.19 ACK Bit Transmission Timing after Reception of 8-Bit Data

■ Transfer Format

There are two transfer format used on IIC bus are : the addressing format that transmits/receives data after 1 byte data (address data) that consists of slave address (7 bits) and R/W bit (1 bit) is transferred after start condition, and the free data format that transmits data right after the start condition. The serial interface of this LSI supports 2 communication formats for only master transmission and master reception in IIC communication. Sequence of communication is shown below. The shaded part shows the data transferred from slave.

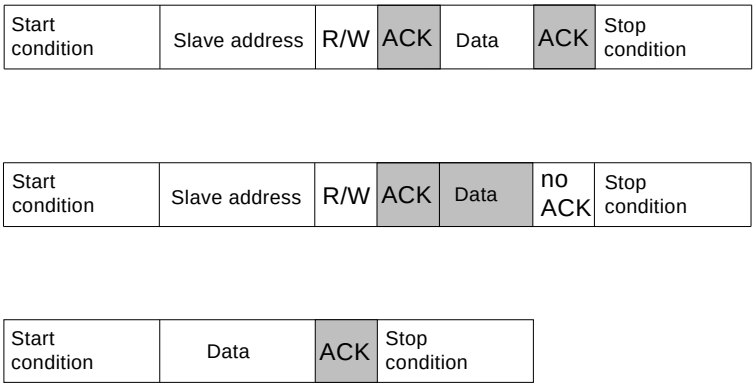


Figure:14.3.20 Communication Sequence on Each Transfer Format

[Figure:14.3.21 Master Transmission Timing, Figure:14.3.22 Master Reception Timing]

■ Clock Setup

The transfer clock for IIC communication is obtained by dividing clock source by 8 inside this serial. The clock source is selected from the dedicated prescaler, timer 3 or 5 output by the SC3MD3 register. The clock source should be set in such a way that the transfer rate is under 100 kHz in NORMAL mode, 400 kHz in high speed mode with the SC3MD3 register. The dedicated prescaler starts as this register selects "prescaler operation". Set the SC3MST flag of the SC3MD1 register to "1" to select the internal clock (clock master). This IIC interface can not be used with external clock (clock slave).

Table:14.3.14 IIC Serial Interface Clock Sources

	Single master IIC
Clcok source (internal clock)	fosc/2
	fosc/4
	fosc/16
	fosc/32
	fs/2
	fs/4
	timer 3 output
	timer 5 output

The transfer rate in IIC communication is obtained by dividing clock source by 8. The clock source should be set in such a way that the transfer rate is under 100 kHz in NORMAL mode, 400 kHz in high speed mode with the SC3MD3 register.

Set the SC3MST flag of the SC3MD1 register to "1" to select internal clock (clock master).

Set the SC3SBIS and SC3SBOS flags of the SC3MD1 register to "0" before change the clock setup.

■ Transmission/Reception Mode Setup and Operation

The SC3REX flag of the SC3CTR register selects the status of the transmission or the reception. The first data is always added start condition for communication regardless of the value of the SC2STE flag. The start condition is output from this serial (master).

The start condition is not added over the second communication, select the start condition "none" at the first setting. And the start condition is added over the second communication, select the start condition "enable" at the first setting.

At addressing format, slave address and R/W bit are set to the first data after start condition for transmission. At master reception, switch to the reception mode at the interrupt transaction after the transmission of the first 1 byte data is finished, after the ACK signal from slave is confirmed. If the communication should be continued to other device without stop, transmit slave address and R/W bit again after start condition is generated again. At reception, the SDA line is automatically released to wait for reception. After the storage of data is finished, confirmation of the reception (ACK bit) is output.

[Figure:14.3.21 Master Transmission Timing, Figure:14.3.22 Master Reception Timing]

■ IIC BUSY Flag Operation

As data is set to the transmission/reception shift register TXBUF3, the IICBSY flag of the SC3CTR register is set to "1", then the IICBSY flag is cleared to "0" at transmission/reception end (communication with ACK) or at last bit communication end (communication without ACK). Setting "1" to the stop condition generation flag (IISTPC), sets IICBSY flag to "1". After stop condition ends, it is cleared to "0".

If start condition is detected during communication, the communication end interrupt SC3IRQ is generated and the IICBSY flag is automatically cleared.

■ Forced Reset

You can shut down the communication by setting both of the SC0SBOS flag and the SC0SBIS flag of the SC0MD1 register to "0" (the SBO0 pin function : port, input data : input "1"). When a forced reset is done, the status register (all flag of the SC2STR register) and SC2BSY flag of the SC2MD0 register are cleared, but other control registers hold their set values.

Forced reset is operated at IICBSY is "0". And generate the stop condition and end the communication.

- First Transfer Bit Setup

Refer to : XIV-15

- Transmission, Reception Data Buffer

Refer to : XIV-15

- Transfer Bit Count and First Transfer Bit

Refer to : XIV-16

- Continuous Communication

Refer to : XIV-17

- Auto Continuous Transfer By ATC

Refer to : XIV-17

In communication, set Nch-open drain for pin type, as the hardware switches if bus is used/ released. In reception, set the SDA3 pin (the SBO3 pin) direction to "output".

■ Master Transmission Timing

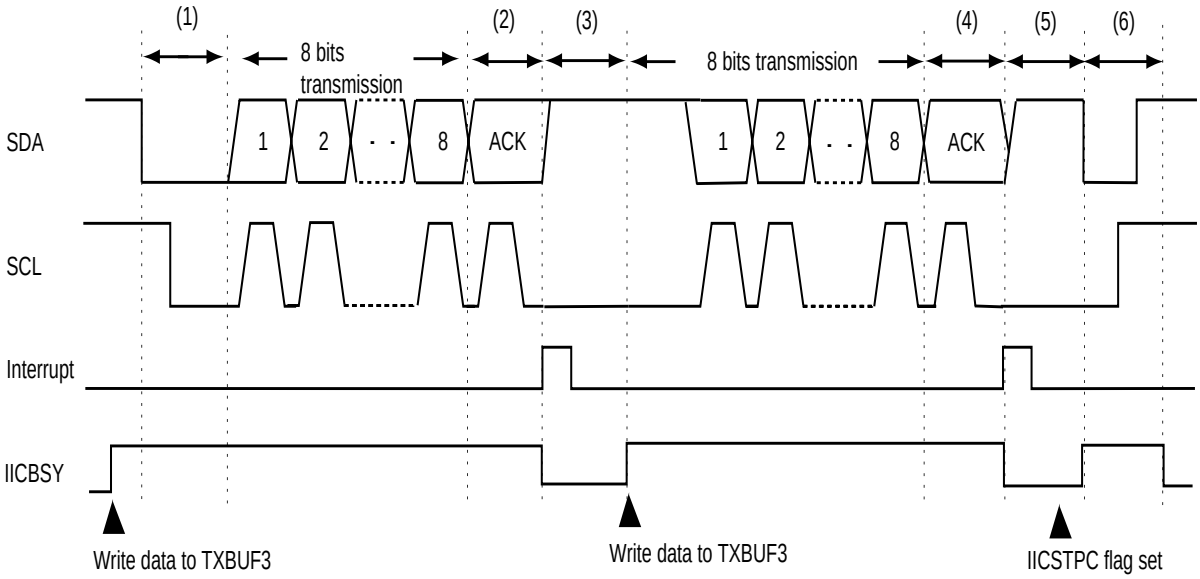


Figure:14.3.21 Master Transmission Timing

(1) Output start condition.

(2) Bus released period, ACK bit is received.

(3) Interrupt

Set data to TXBUF3

(4) Receive ACK bit.

(5) Interrupt

Communication ends : clear the IICBSY flag.

(6) Generates stop condition.

■ Master Reception Timing

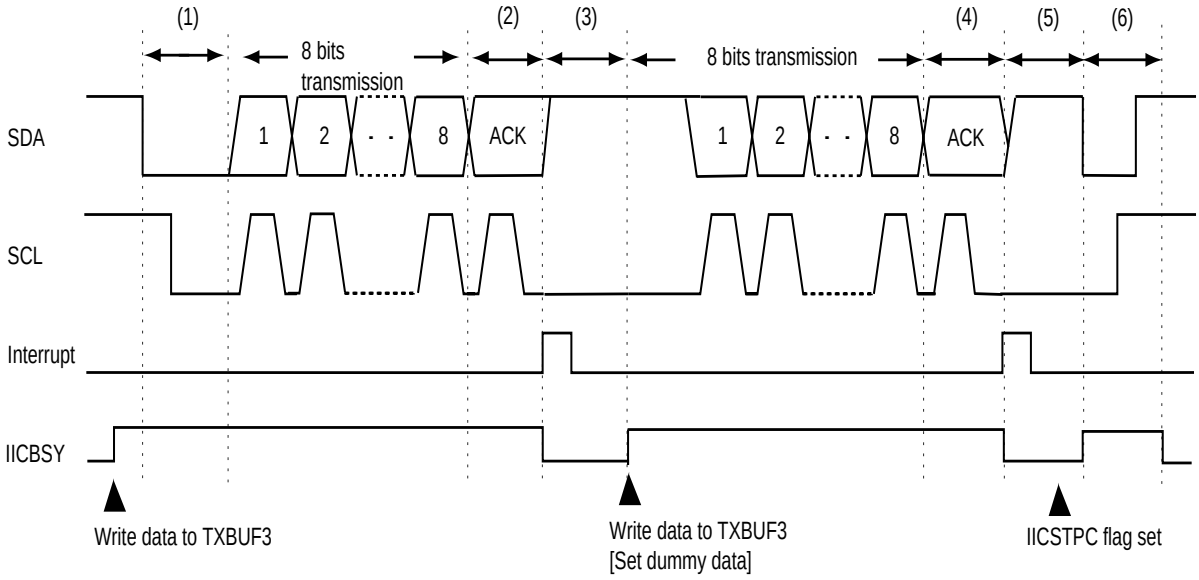


Figure:14.3.22 Master Reception Timing

(1) Output start condition.

(2) Bus released period, ACK bit is received.

(3) Interrupt

Set to reception mode : SC3REX = 0 → 1

Set data to TXBUF3

(4) Receive ACK bit.

(5) Interrupt

Communication ends : clear the IICBSY flag.

(6) Generates stop condition.

■ Pin Setup (2 channels, at transmission)

Table:14.3.15 shows the pins setup in IIC serial interface transmission with 2 channels (SDA3 pin, SCL3 pin).

Table:14.3.15 Pin Setup (2 channels, at transmission)

Item	Data I/O pin	Clock I/O pin
	SDA3A pin / SDA3B pin	SCL3A pin / SCL3B pin
		Clock master
		SC3MD1(SC3MS)
Pin	P33 / P93	P35 / P95
Port pin selection	Select the used pin(A, B)	
	SCSEL (SC3SEL)	
SDA3/SCL3 pins	SBI3/SDA3 pin connection	-
	SC3MD1(SC3IOM)	
Function	Serial data output	Transfer clock output
	SC3MD1(SC3SBOS)	SC3MD1(SC3SBTS)
	Serial data input	-
	SC3MD1(SC3SBIS)	
Type	N-ch open-drain	N-ch open-drain
	P3ODC(P3ODC3)	P3ODC(P3ODC5) / P9ODC(P9ODC5)
I/O	output mode	output mode
	P3DIR(P3DIR3) / P9DIR(P9DIR3)	P3DIR(P3DIR5) / P9DIR(P9DIR5)
Pull-up selection	added	added
	P3PLU(P3PLU3) / P9PLU(P9PLU3)	P3PLU(P3PLU5) / P9PLU(P9PLU5)

■ Pin Setup (2 channels, at reception)

Table:14.3.16 shows the pins setup in IIC serial interface reception with 2 channels (SDA3 pin, SCL3 pin).

Table:14.3.16 Pin Setup (2 channels, at reception)

Item	Data I/O pin	Clock I/O pin
	SDA3A pin / SDA3B pin	SCL3A pin / SCL3B pin
		Clock master
		SC3MD1(SC3MS)
Pin	P33 / P93	P35 / P95
Port pin selection	Select the used pin(A, B)	
	SCSEL (SC3SEL)	
SDA3/SCL3 pins	SBI3/SBO3 pin connection	-
	SC3MD1(SC3IOM)	
Function	Port	Serial data output
	SC3MD1(SC3SBOS)	SC3MD1(SC3SBTS)
	Serial data input	-
	SC3MD1(SC3SBIS)	
Type	N-ch open-drain	N-ch open-drain
	P3ODC(P3ODC3) / P9ODC(P9ODC3)	P3ODC(P3ODC5) / P9ODC(P9ODC5)
I/O	output mode	output mode
	P3DIR(P3DIR3) / P9DIR(P9DIR3)	P3DIR(P3DIR5) / P9DIR(P9DIR5)
Pull-up	added	added
	P3PLU(P3PLU3) / P9PLU(P9PLU3)	P3PLU(P3PLU5) / P9PLU(P9PLU5)

14.3.4 Setup Example

■ Master Transmission Setup Example

Here is the setup example of the transmission of several bytes data to the all the devices on IIC bus using IIC serial Interface 3. Table:14.3.17 shows the conditions.

Table:14.3.17 Conditions Single Master IIC Communication Setup

Item	Set to
SBI3/SBO3 pins	Connection (2 channels)
Transfer bit count	8 bits
Start condition	Enable (disable after second communication)
First transfer bit	MSB
ACK bit	Enable
IIC communication mode	NORMAL mode
Clock source	fosc/32
Used pins selection	A (port3)
SCL3/SDA3 pin type	N-ch open-drain
SCL3 pull-up resistance	added
SDA3 pull-up resistance	added

An example setup procedure, with a description of each step is shown below.

Setup Procedure	Description
(1) Select prescaler operation. SC3MD3 (0x03FA6) bp3: SC3PSCE =1	(1) Set the SC3PSCE flag of the SC3MD3 register to "1" to select prescaler operation.
(2) Select the clock source. SC3MD3 (0x03FA6) bp2-0: SC3PSC2-0 =011	(2) SC3PSC2-0 flags of the SC3MD3 register to "001" to select fs/32 at clock source.
(3) Used pins selection. SC3MD3 (0x03F4F) bp3 :SC3SEL =0	(3) Set the SC3PSC2-0 flag of the SC3MD3 register to "0" to select the used pin A (port 3).
(4) Control of pin type. P3ODC (0x03F2C) bp5, 3: P3ODC5, 3 =1, 1	(4) Set the P3ODC5, 3 flag of the P3ODC register to "1, 1" to select N-ch open drain for the SDA3/SCL3 pin type.
(5) Control of pin direction. P3DIR (0x03F03) bp5, 3: P3DIR5, 3 =1, 1	(5) Set the P3DIR5, 3 flag of P0 pin control direction register (P3DIR) to "1, 1" to set P35, P33, to output mode.

Setup Procedure	Description
(6) Set ACK bit. SC3CTR (0x03F9C) bp0 :SC3ACKO =x bp1 :SC3ACKS =1	(6) Set the SC3ACKS flag of the serial 3 control register (SC3CTR) to "1" to select "receive ACK bit". ACK bit is received at transmission, and setup of the ACK bit level with the SC3ACKS flag is not necessary.
(7) Select the communication mode. SC3CTR (0x03F9C) bp4 :SC3TMD =0	(7) Set the SC3TMD flag of the serial 3 control register (SC3CTR) to "0" to select NORMAL mode.
(8) Select the communication type. SC3CTR (0x03FAA) bp2 :SC3CMD =1	(8) Set the SC3CMD flag of the serial 3 control register (SC3CTR) to "1" to select IIC.
(9) <Transmission setup> Selection of transmission/reception SC3CTR(0x03FAA) bp3 :SC3REX =0	(9) Set the SC3REX flag of the serial 3 control register (SC3CTR) to "0" to select the transmission mode.
(10) Initialize the monitor flag. SC3CTR (0x03FAA) bp6 :IICSTC =0	(10) Set the IICSTC flag of the serial 3 control register (SC3CTR) to "0, 0" to initialize the start condition detection flag.
(11) Set the SC3MD0 register. Select the transfer bit count. SC3MD0 (0x03FA4) bp2-0 :SC3LNG2-0 =111 Select the start condition. SC3MD0 (0x03FA4) bp3 :SC3STE =1 Select the first bit to be transferred. SC3MD0 (0x03FA4) bp4 :SC3DIR =0 Select the IIC communication edge. SC3MD0(0x03FA4) bp6 :SC3CE1 =1	(11) Set the SC3LNG2-0 flag of the serial 3 mode register (SC3MD0) to "111" to set the transfer bit count to 8 bits. Set the SC3STE flag of the SC3MD0 register to "1" to disable start condition.And start condition is not added over the second communication. Set the SC3DIR flag of the SC3MD0 register to "0" "to set MSB as the first bit to be transferred. In IIC communication, set the SC3CE1 flag of the SC3MD0 register to "1".
(12) Set the SC3MD1 register. Select the transfer clock. SC3MD1 (0x03FA5) bp2 :SC3MST =1 Control of pin function. SC3MD1 (0x03FA5) bp4 :SC3SBOS =1 bp5 :SC3SBIS =1 bp6 :SC3SBTS =1 bp7 :SC3IOM =1	(12) Set the SC3MST flag of the SC3MD1 register to "1" to select clock master (internal clock). In IIC communication, do not select external clock. Set the SC3SBOS, SC3SBIS, SC3SBTS flags of the SC3MD1 register to "1" to set the SDA3 pin (the SBO3 pin) to serial data output, the SBI3 pin to serial data input, and the SCL3 pin (the SBT3 pin) to serial clock I/O. Set the SC3IOM flag to "1" to set "serial data input from the SDA3 pin (the SBO3 pin)".
(13) Set the interrupt level. SC3ICR (0x03FF7) bp7-6 :SC3LV1-0 =10	(13) Set the interrupt level by the SC3LV1-0 flag of the serial 3 interrupt control register (SC3ICR).

Setup Procedure	Description
(14) Enable the interrupt. SC3ICR (0x03FF7) bp1 :SC3IE =1	(14) Set "1" to the SC3IE flag of the SC3ICR register to enable the interrupt. If the interrupt request flag (SC3IR of the SC3ICR register) is already set, clear SC3IR before the interrupt is enabled. [Chapter 3 3.1.4. Interrupt Flag Setup]
(15) <Start serial transmission.> Start serial transmission. Confirm that SCL3 (P35) is "H". Transmission data → TXBUF3 (0x03FA8)	(15) Set the transmission data to the transmission/reception shift register TXBUF3. Then the transfer clock is generated to start transmission. If the ACK bit is received after data transmission, the communication end interrupt SC3IRQ is generated.
(16) <Transmission ends.> <Setup of the next data transmission> Judge the monitor flag. SC3CTR (0x03FAA) bp6 :IICSTC	(16) Confirm the IICSTC flag of the serial 3 control register (SC3CTR). When the previous transmission is completed properly, IICSTC = "0". If IICSTC = "1", the communication should be re-executed.
(17) Judge the ACK bit level. SC3CTR (0x03FAA) bp0 :SC3ACKO	(17) Confirm the level of the ACK bit, received by the SC3ACKO flag of the serial 3 control register (SC3CTR). When SC3ACKO = 0, you can continue the transmission. When SC3ACKO = 1, the reception at slave may not be operated properly, so finish the communication.
(18) Set the SC3MD0 register. Select the transfer bit count. SC3MD0 (0x03FA4) bp2-0 :SC3LNG2-0	(18) To change the transfer count bit, set the transfer count bit by the SC3LNG2-0 flag of the serial 3 mode register (SC3MD0).
(19) <Next data transmission is started.> Serial transmission is started. [→ (16)]	(19) Set the transmission data to TXBUF3 to start the transmission. [→ (16)]
(20) <Transmission ends.> <IIC communication end processing> Set the IICSTPC flag SC3CTR (0x03FAA) bp5 :IICSTPC =1	(20) Set the IICSTPC flag of the serial 3 control register (SC3CTR) to "1", so that the stop condition is automatically generated to finish the communication.

Note : Procedures (1) to (2) can be set at once.

Note : Procedures (6) to (10) can be set at once.

Note : Procedures (11) to (12) can be set at once.

Set each flag in order of the setup procedures. Set all the control registers (refer toTable:14.2.1, except TXBUF2) before start communication.

Chapter 15 Serial interface 4

15

15.1 Overview

This LSI contains a serial interface 4 that can be used for both communication types of clock synchronous and UART (full duplex).

15.1.1 Functions

Table:15.1.1 shows functions of serial interface 4.

Table:15.1.1 Serial Interface 4 functions

Communication style	Clock synchronous	UART (full duplex)
Interrupt	SC4TIRQ	SC4TIRQ(on transmission completion) SC4RIRQ(on reception completion)
Used pins	SBO4,SBI4,SBT4	TXD4,RXD4
3 channels type	O	-
2 channels type	O(SBO4,SBT4)	O
1 channel type	-	TXD4
Specification of transfer bit count/ Frame selection	1 to 8 bits	7 bit +1STOP 7 bit +2STOP 8 bit +1STOP 8 bit +2STOP
Selection of parity bit	-	O
Parity bit control	-	0 parity 1 parity odd parity even parity
Selection of start condition	O	Only "enable start condition" is available
Specify of the first transfer bit	O	O
Specify of input edge/ output edge	O	-
SBO4 output control after final data moved out	H/L/final data hold	-
At the standby mode	Only slave reception is available	-
Continuous operation	O	O
Internal clock 1/8 dividing	O	Only 1/8 dividing is available

Clock source	fosc/2 fosc/4 fosc/16 fosc/64 fs/2 fs/4 External clock Timer 2 output Timer 5 output	fosc/2 fosc/4 fosc/16 fosc/64 fs/2 fs/4 Timer 2 output Timer 5 output
Maximum transfer rate	5.0 MHz	300 kbps
fosc:Machine clock (High speed oscillation) fs:System clock		

Set the transfer rate slower than system clock (fs).

15.1.2 Block Diagram

■ Serial interface 4 Block Diagram

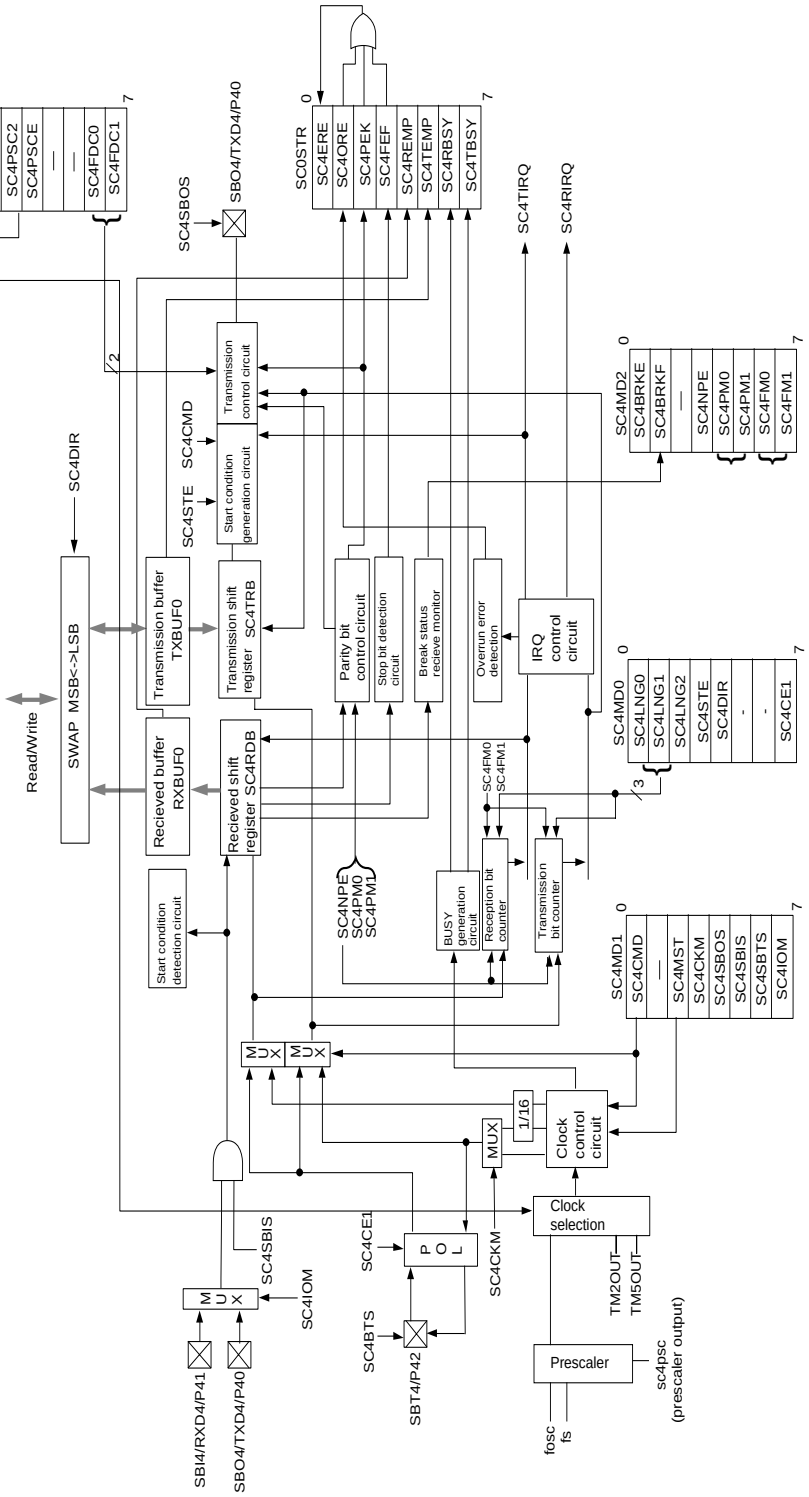


Figure:15.1.1 Serial interface 4 Block Diagram

15.2 Control Registers

15.2.1 Registers

Table:15.2.1 shows registers to control serial interface 4.

Table:15.2.1 Serial interface 4 Control Registers

Register	Address	R/W	Function	Page
SC4MD0	0x03FAB	R/W	Serial interface 4 mode register 0	XV-7
SC4MD1	0x03FAC	R/W	Serial interface 4 mode register 1	XV-8
SC4MD2	0x03FAD	R/W	Serial interface 4 mode register 2	XV-9
SC4MD3	0x03FAE	R/W	Serial interface 4 mode register 3	XV-10
SC4STR	0x03FAF	R	Serial interface 4 status register	XV-11
RXBUF4	0x03FB0	R	Serial interface 4 received data buffer	XV-6
TXBUF4	0x03FB1	R/W	Serial interface 4 transmission data buffer	XV-6
P4ODC	0x03F3C	R/W	Port 4 Nch open drain control register	IV-44
P4DIR	0x03F34	R/W	Port 4 direction control register	IV-43
P4PLU	0x03F44	R/W	Port 4 pull-up/pull-down control register	IV-44
SC4RICR	0x03FF8	R/W	Serial 4 UART reception interrupt control register	III-42
SC4TICR	0x03FF9	R/W	Serial 4 UART transmission interrupt control register	III-43

R/W:Readable/ Writable

R:Readable only

15.2.2 Data Buffer Registers

Serial interface 4 has each 8-bit data buffer register for transmission, and for reception.

■ Serial interface 4 Received Data Buffer (RXBUF4:0x03FB0)

bp	7	6	5	4	3	2	1	0
Flag	RXBUF47	RXBUF46	RXBUF45	RXBUF44	RXBUF43	RXBUF42	RXBUF41	RXBUF40
Reset	X	X	X	X	X	X	X	X
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

■ Serial interface 4 Transmission Data Buffer (TXBUF4:0x03FB1)

bp	7	6	5	4	3	2	1	0
Flag	TXBUF47	TXBUF46	TXBUF45	TXBUF44	TXBUF43	TXBUF42	TXBUF41	TXBUF40
Reset	X	X	X	X	X	X	X	X
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

15.2.3 Mode Registers

■ Serial interface 4 Mode Register 0 (SC4MD0:0x03FAB)

bp	7	6	5	4	3	2	1	0
Flag	SC4CE1	-	-	SC4DIR	SC4STE	SC4LNG2	SC4LNG1	SC4LNG0
Reset	0	-	-	0	0	1	1	1
Access	R/W	-	-	R/W	R/W	R/W	R/W	R/W

bp	Flag	Description
7	SC4CE1	Transmission data output edge 0:falling 1:rising Reception data input edge 0:rising 1:falling
6-5	-	-
4	SC4DIR	First bit to be transferred 0:MSB first 1:LSB first
3	SC4STE	Start condition selection 0:Disable start condition 1:Enable start condition
2-0	SC4LNG2 SC4LNG1 SC4LNG0	Transfer bit 000:1bit 001:2bit 010:3bit 011:4bit 100:5bit 101:6bit 110:7bit 111:8bit

■ Serial interface 4 Mode Register 1(SC4MD1:0x03FAC)

bp	7	6	5	4	3	2	1	0
Flag	SC4IOM	SC4SBTS	SC4SBIS	SC4SBOS	SC4CKM	SC4MST	-	SC4CMD
Reset	0	0	0	0	0	0	-	0
Access	R/W	R/W	R/W	R/W	-	R/W	-	R/W

bp	Flag	Description
7	SC4IOM	Serial data input selection 0:Data input from SBI4 (RXD4) 1:Data input from SBO4 (TXD4)
6	SC4SBTS	SBT4 pin function selection 0:Port 1:Transfer clock I/O
5	SC4SBIS	Serial input control selection 0:Input "1" 1:Input serial
4	SC4SBOS	SBO4(TXD4) pin function 0:Port 1:Output serial data
3	SC4CKM	1/8 dividing of transfer clock selection 0:Not divided by 8 1:8 cycle
2	SC4MST	Clock master/ slave selection 0:Clock slave 1:Clock master
1	-	-
0	SC4CMD	Synchronous serial/ full duplex UART selection 0:Synchronous serial 1:Full duplex UART

■ Serial interface 4 Mode Register 2 (SC4MD2:0x03FAD)

bp	7	6	5	4	3	2	1	0
Flag	SC4FM1	SC4FM0	SC4PM1	SC4PM0	SC4NPE	-	SC4BRKF	SC4BRKE
Reset	0	0	0	0	0	-	0	0
Access	R/W	R/W	R/W	R/W	R/W	-	R	R/W

bp	Flag	Description
7-6	SC4FM1 SC4FM0	Frame mode specification 00:7 data bit + 1 stop bit 01:7 data bit + 2 stop bit 10:8 data bit + 1 stop bit 11:8 data bit + 2 stop bit
5-4	SC4PM1 SC4PM0	Added bit specification Transmission Reception 00:Add "0" Check for 0 01:Add "1" Check for 1 10:Add odd parity Check for odd parity 11:Add even parity Check for even parity
3	SC4NPE	Parity enable 0:Enable parity bit 1:Disable parity bit
2	-	-
1	SC4BRKF	Break status receive monitor 0:Data reception 1:Break reception
0	SC4BRKE	Break status transmit control 0:Data transmission 1:Break transmission

■ Serial interface 4 Mode Register 3 (SC4MD3:0x03FAE)

bp	7	6	5	4	3	2	1	0
Flag	SC4FDC1	SC4FDC0	-	-	SC4PSCE	SC4PSC2	SC4PSC1	SC4PSC4
Reset	0	0	-	-	0	0	0	0
Access	R/W	R/W	-	-	R/W	R/W	R/W	R/W

bp	Flag	Description
7-6	SC4FDC1 SC4FDC0	Output selection after SBO4 final data transmit 00:Fix at "1" (High) output 01:Final data hold 10:Fix at "0" (Low) output 11:Reserved
5-4	-	-
3	SC4PSCE	Prescaler count control 0:Count is forbidden 1:Count is allowed
2-0	SC4PSC2 SC4PSC1 SC4PSC4	Selection clock 000:fosc/2 001:fosc/4 010:fosc/16 011:fosc/64 100:fs/2 101:fs/4 110:Timer 2 output 111:Timer 5 output

■ Serial interface 4 Status Register (SC4STR:0x03FAF)

bp	7	6	5	4	3	2	1	0
Flag	SC4TBSY	SC4RBSY	SC4TEMP	SC4REMP	SC4FEF	SC4PEK	SC4ORE	SC4ERE
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R

bp	Flag	Description
7	SC4TBSY	Serial bus status 0:Other use 1:Serial transmission in progress
6	SC4RBSY	Serial bus status 0:Other use 1:Serial reception in progress
5	SC4TEMP	Transfer buffer empty flag 0:Empty 1:Full
4	SC4REMP	Receive buffer empty flag 0:Empty 1:Full
3	SC4FEF	Framing error detection 0:No error 1:Error
2	SC4PEK	Parity error detection 0:No error 1:Error
1	SC4ORE	Overrun error detection 0:No error 1:Error
0	SC4ERE	Error monitor flag 0:No error 1:Error

15.3 Operation

Serial interface 4 can be used for both clock synchronous and full duplex UART.

15.3.1 Clock Synchronous Serial Interface

■ Activation Factor for Communication

Table:15.3.1 shows activation factors for communication. At master communication, the transfer clock is generated by setting data to the transmission data buffer TXBUF4, or by receiving a start condition. Except during communication, the input signal from SBT4 pin is masked to prevent errors by noise or so.This mask can be released automatically by setting a data to TXBUF4 (access to the TXBUF4 register), or by inputting a start condition to the data input pin. Therefore, at slave communication, set data to TXBUF4, or input an external clock after a start condition is input.

However, the external clock should be input after more than 3.5 transfer clock interval after the data set to TXBUF4. This wait time is needed to load the data from TXBUF4 to the internal shift register.

Table:15.3.1 Synchronous Serial Interface Activation Factor

	Activation factor	
	Transmission	Reception
At master	Set transmission data	Set dummy data
		Input start condition
At slave	Input clock after transmission data is set	Input clock after dummy data is set
		Input clock after start condition is input

■ Transfer Bit Setup

The transfer bit count is selected from 1 to 8 bits. Set them by the SC4LNG 2 to 0 flag of the SC4MD0 register (at reset:111). The SC4LNG2 to 0 flag holds the former set value until it is set again.

Except during communication, SBT4 pin is masked to prevent errors by noise. At slave communication, set data to TXBUF4 or input a clock to SBT4 pin after a start condition is input.

To communicate properly, more than 3.5 transfer clock after the data set to TXBUF4 is needed to input the external clock.

■ Start Condition Setup

The SC4STE flag of the SC4MD0 register sets if a start condition is enabled or not.

The start condition is regarded that when SC4CE1 flag of SC4MD0 is set to "0" and a clock line (SBT4 pin) is "H", data line (SBI4 pin (with 3 lines) or SBO4 pin (with 2 lines)) is changed from "H" to "L". Also, it is regarded that when SC4CE1 flag is set to "0" and a clock line (SBT4 pin) is "L", data line (SBI4 pin (with 3 lines) or SBO4 pin (with 2 lines)) is changed from "H" to "L".

Both the SC4SBOS flag and the SC4SBIS flag of the SC4MD1 register should be set to "0", before the start condition setup is changed.

At the selection of the start condition "enable" and master transmission / reception, after the start condition output, start condition is input from the slave, then data transmission is generated.

■ First Transfer Bit Setup

The SC4DIR flag of the SC4MD0 register can set the transfer bit. MSB first or LSB first can be selected.

■ Transmission Data Buffer

The transmission data buffer, TXBUF4 is a buffer of reserve that stores data to load the internal shift register. Data to be transferred should be set to the transmission data buffer, TXBUF4, to be loaded to the internal shift register automatically. The data load time of 3.5 transfer clock is needed to load the data. On loading, setting the data to TXBUF4 again may cause error. On loading or not is determined by monitoring the transmission buffer empty flag of the SC4STR. When the data is set to TXBUF4, SC4TEMP flag is set to "1" and when loading is finished, it is cleared "0" automatically.

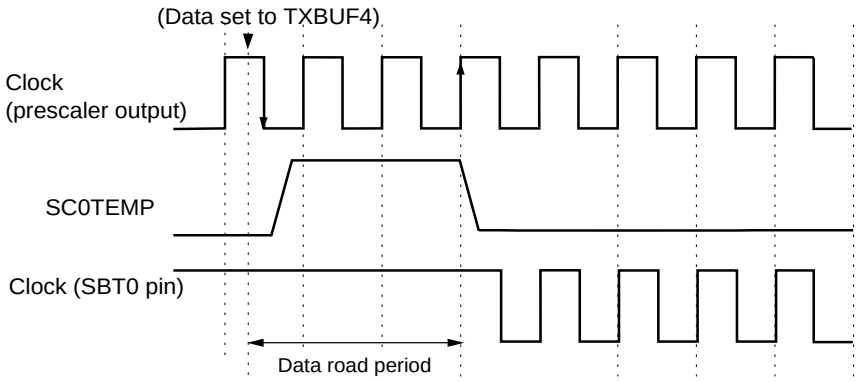


Figure:15.3.1

■ Received Date Buffer

The received data buffer RXBUF4 is a buffer of reserve that pushed the received data in the internal shift register. After the communication complete interrupt SC4TIRQ is generated, all data stored in the internal shift register are stored to the received data buffer RXBUF4 automatically. RXBUF4 can store data up to 1 byte. RXBUF4 is rewritten in every time when communication is completed, so read out data of RXBUF4 till the next receive is completed. The received data buffer empty flag SC4REMP is set to "1" at the same time SC4TIRQ is generated. SC4REMP is cleared to "0" after RXBUF4 is read out.

If a start condition is input to restart during communication, the transmission data is not valid. Set the transmission data to TXBUF4 again to operate the transmission again.

RXBUF4 is rewritten every time when communication is completed. At continuous communication, data of RXBUF4 should be read out until the next reception is completed.

■ Transfer Bit Count and First Transfer Bit

When the transfer bit is 1 bit to 7bit, the data storing method to the transmission data buffer TXBUF4 is different, depending on the first transfer bit selection. At MSB first, use the upper bits of TXBUF4 for storing. When there are 6 bits to be transferred, as shown on Figure:15.3.2, if data "A" to "F" are stored to bp2 to bp7 of TXBUF4, the transmission is operated from "F" to "A". At LSB first, use the lower bits of TXBUF4 for storing. When there are 6 bits to be transferred, as shown on Figure:15.3.3, if data "A" to "F" are stored to bp0 to bp5 of TXBUF4, the transmission is operated from "A" to "F".

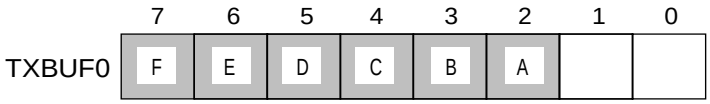


Figure:15.3.2 Transfer Bit Count and First Transfer Bit (starting with MSB)

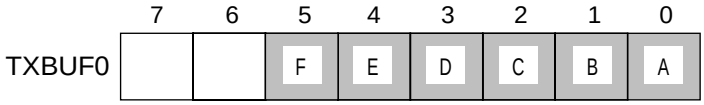


Figure:15.3.3 Transfer Bit Count and First Transfer Bit (starting with LSB)

■ Receive Bit Count and First Transfer Bit

When the transfer bit count is 1 bit to 7 bits, the data storing method to the received data buffer RXBUF4 is different depending on the first transfer bit. At MSB first, data are stored to the lower bits of RXBUF4. When there are 6 bits to be transferred, as shown on figure Figure:15.3.4, if data "A" to "F" are stored to bp0 to bp5 of RXBUF4, the transmission is operated from "F" to "A". At LSB first, data are stored to the upper bits of RXBUF4. When there are 6 bits to be transferred, as shown on Figure:15.3.5, if data "A" to "F" are stored to bp2 to bp7 of RXBUF4, the transmission is operated from "A" to "F".

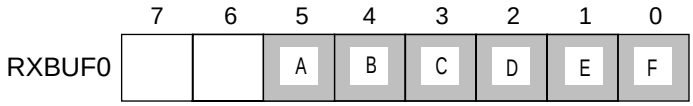


Figure:15.3.4 Receive Bit Count and Transfer First Bit (starting with MSB bit)

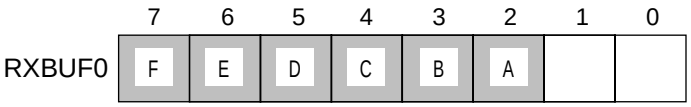


Figure:15.3.5 Receive Bit Count and Transfer First Bit (starting with LSB bit)

When the serial transfer bit is set between 1 to 7, the data except for received data of the specified transfer bit count is unknown. Use the received data after being masked by AND/ OR instruction.

■ Continuous Mode

This serial has a function for continuous communication. If data is set to the transmission data buffer TXBUF4 during communication, the transmission buffer empty flag SC4TEMP is automatically set to interrupt SC4TIRQ is generated after the former data is set. Data setup to TXBUF4 should be done till the communication complete interrupt SC4TIRQ is generated after the data is loaded to the internal shift register. At master communication, there is output after the pension of communication for 4 transfer clocks till the next transmission clock is output after the SC4TIRQ generation.

■ ATC Automatic Continuous Transfer

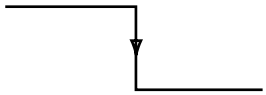
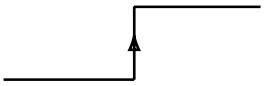
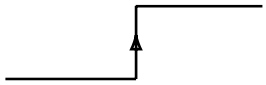
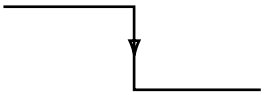
This serial enables the start-up by the data automatic transfer (ATC1). On start-up by ATC1, 255 bytes data transfer can be operated.

Refer to [chapter 18 Automatic Transfer Controller : overview : transfer mode 8 to 9 about the generation of ATC1.]

■ Input Edge/ Output Edge Setup

The SC4CE1 flag of the SC4MD0 register set an output edge of the transmission data, an input edge of the received data. As the SC4CE1 flag = "0", the transmission data is output at the falling edge, and as "1", output at the rising edge. As SC4CE1 = "0", the received data is received at the inversion edge to the output edge of transmission data, and as "1", stored at the same edge.

Table:15.3.2 Transmission Data Output Edge and Received Data Input Edge

SC4CE1	Transmission data output edge	Received data input edge
0		
1		

■ Clock Setup

The SC4PSC2 to 0 of the SC4MD3 register selects the clock source from the special prescaler and timer 2, timer 5 (2 lines) output. The special prescaler starts its operation after the SC4PSCE flag of the SC4MD1 register selects "enable count". The SC4MST flag of the SC4MD1 register can select the internal clock (clock master), or the external clock (clock slave). Even if the external clock is selected, set the internal clock that has the same clock cycle or lower to the external clock, by the SC4MD3 register.

Table:15.3.3 Synchronous Serial Interface Clock Source

	serial 4
Clock source (internal clock)	fosc/2
	fosc/4
	fosc/16
	fosc/64
	fs/2
	fs/4
	Timer 2 output
	Timer 5 output

When the clock setup is switched, the SC4SBIS flag and SC4SBOS flag of the SC4MD1 register should be set to "0".

When the slave reception is done with enabled start condition, set the speed of the transfer clock slower than the system clock.

■ Data Input Pin Setup

3 channels type (clock pin (SBT4 pin), data output pin (SBO4 pin), data input pin (SBI4 pin)) or 2 channels type (clock pin (SBT4 pin), data I/O pin (SBO4 pin)) can be selected as a communication mode. SBI4 pin can be used for only serial data input. SBO4 pin can select serial data input or output. The SC4IOM flag of the SC4MD1 register can select if the serial data is input to SBI4 pin or SBO4 pin. When "data input from SBO4 pin" is selected to set the 2 lines type, the P4DIR0 flag of the P4DIR register controls direction of SBO4 pin to switch transmission/ reception. At this time, SBI4 pin can be used as a general port, too.

The transfer speed should be up to 5.0 MHz. If the transfer clock is over 5.0 MHz, the transmission data may not be sent correctly.

At reception, if SC4IOM of the SC4MD1 register is set to "1" and "serial data input from SBO4" is selected, SBI4 pin can be used as a general port.

■ Reception Buffer Empty Flag

After reception is completed (SC4TIRQ is generated), data is automatically stored to RXBUF4 from the internal shift register. If data is stored to the shift register RXBUF4 when the SC4SBIS of the SC4MD1 register is set to "serial input", the reception buffer empty flag SC4REMP of the SC4STR register is set to "1". This indicates that the received data is going to read out. SC4REMP is cleared to "0" by reading out the data of RXBUF4.

■ Transmission Buffer Empty Flag

During the communication (after setting data to TXBUF4 and before the communication complete interrupt SC4TIRQ is generated) if any data is set to TXBUF4 again, the transmission buffer empty flag SC4REMP of the SC4STR register is set to "1". This indicates that the next transmission data is going to be loaded. Data is loaded to the inside shift register from TXBUF4 by generation of SC4TIRQ, and the next transfer is started as SC4TEMP is cleared to "0".

■ Overrun Error and Error Monitor Flag

After reception complete, if the next data has been already received before reading out of the data of the received data buffer RXBUF4, overrun error is generated and the SC4ORE flag of the SC4STR register is set to "1". At the same time, the error monitor flag SC4ERE is set to indicate that error is occurred on reception. The SC4ERE flag is not cleared till the next communication complete interrupt SC4TIRQ is generated after loading data of the RXBUF4. SC4ERE is cleared as SC4ORE flag is cleared. These error flags have no effect on communication operation.

■ Reception BUSY Flag

If the data is set to the TXBUF4 or recognized the start condition when the SC4SBIS flag of the SC4MD1 register is set to "serial data input", the BUSY flag SC4RBSY of the SC4STR register is set to "1". And, on the generation of the communication complete interrupt SC4TIRQ, the flag is cleared to "0". And, during continuous communication, the SC4RBSY flag is always set. If the transmission buffer empty flag SC4TEMP is cleared to "0" as the communication complete interrupt SC4TIRQ is generated, SC4RBSY is cleared to "0". If the SC4SBIS flag is set to "0" during communication, the SC4RBSY flag is cleared to "0".

■ Transmission BUSY Flag

Data is set to the TXBUF4 or recognized the start condition when the SC4SBOS flag of the SC4MD1 register is set to "serial data output", if the SC4SBOS flag of the SC4MD1 register is "1", SC4TBSY flag of the SC4STR register is set. And, on the generation of the communication complete interrupt SC4TIRQ, the flag is cleared "0". And, during continuous communication, the SC4TBSY flag is always set. If the transmission buffer empty flag SC4TEMP is cleared to "0" as the communication complete interrupt SC4TIRQ is generated,SC4TBSY is cleared to "0". If the SC4SBOS flag is set to "0" during communication, the SC4TBSy flag is cleared to "0".

■ Emergency Reset

This serial interface contains emergency reset for abnormal operation. For emergency reset, the SC4SBOS flag and the SC4SBIOS flag of the SC4MD1 register should be set to "0" (SBO4 pin:port, input data:"1" input).

At emergency reset, the status register (the SC4BRKF flag of the SC4MD2 register, all flags of the SC4STR register) are initialized as they are set at reset, but the control register holds the set value.

■ Last Bit of Transfer Data

Table:15.3.4 shows the data output holding period of the last bit at transmission, and the minimum data input period of the last bit at reception. The internal clock should be set up at slave to keep the data hold time at reception.

Table:15.3.4 Last Bit Data Length of Transfer Data

	The last bit data holding period at transmission	The last data input period at reception
At master	1 bit data length	1 bit data length (Minimum)
At slave	[1 bit data length of external clock × 1/2] + [internal clock cycle × (1/2-3/2)]	

In the case of disabled start condition (at SC4STE flag = 0), the SBO4 output after the data output holding period of the final bit can be set as Table:15.3.5 by the setting value of the SC4FDC1 to 0 flag of the SC4MD3 register.

After released the reset, despite of the setting value of the SC4FDC1 to 0 flag, output before the serial transfer is "H". In the case of the enabled start condition (at SC4STE flag = 1), "H" is output despite of the setting value of the SC4FDC1 to 0.

Table:15.3.5 SBO4 Output after the Data Output Holding Period of the Last Bit (without start condition)

SC4FDC1 flag	SC4FDC0 flag	SBO4 output after the data output holding period of the last bit
0	0	"1"(High) output fix
1	0	Last data holding
0	1	"0"(Low) output fix
1	1	Reserved

■ Other Control Flag Setup

Table:15.3.6 shows flags that are not used at clock synchronous communication. So, they are not needed to set or monitor.

Table:15.3.6 Other Control Flag

Register	Flag	Detail
SC4MD2	SC4BRKE	Break status transmission control
	SC4BRKF	Break status reception monitor
	SC4NPE	Parity enable
	SC4PM1 to 0	Added mode specification
	SC4FM1 to 0	Frame mode specification
SC4STR	SC4PEK	Parity error detection
	SC4FEF	Frame error detection

■ Transmission Timing

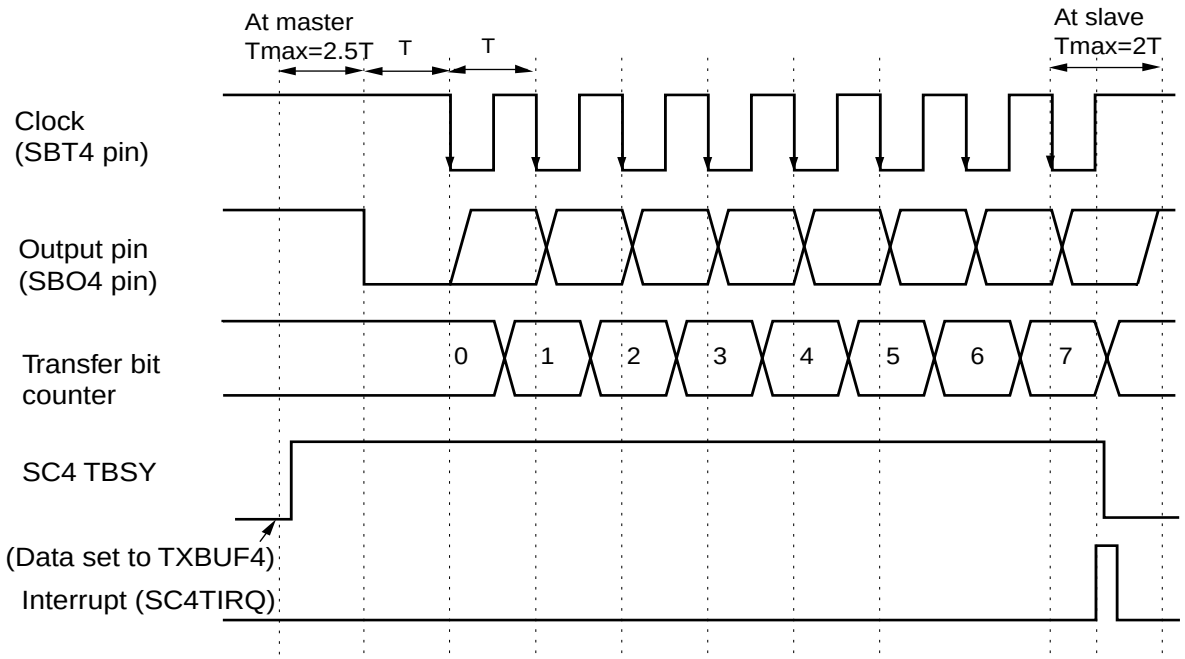


Figure:15.3.6 Transmission Timing (at falling edge, start condition is enabled)

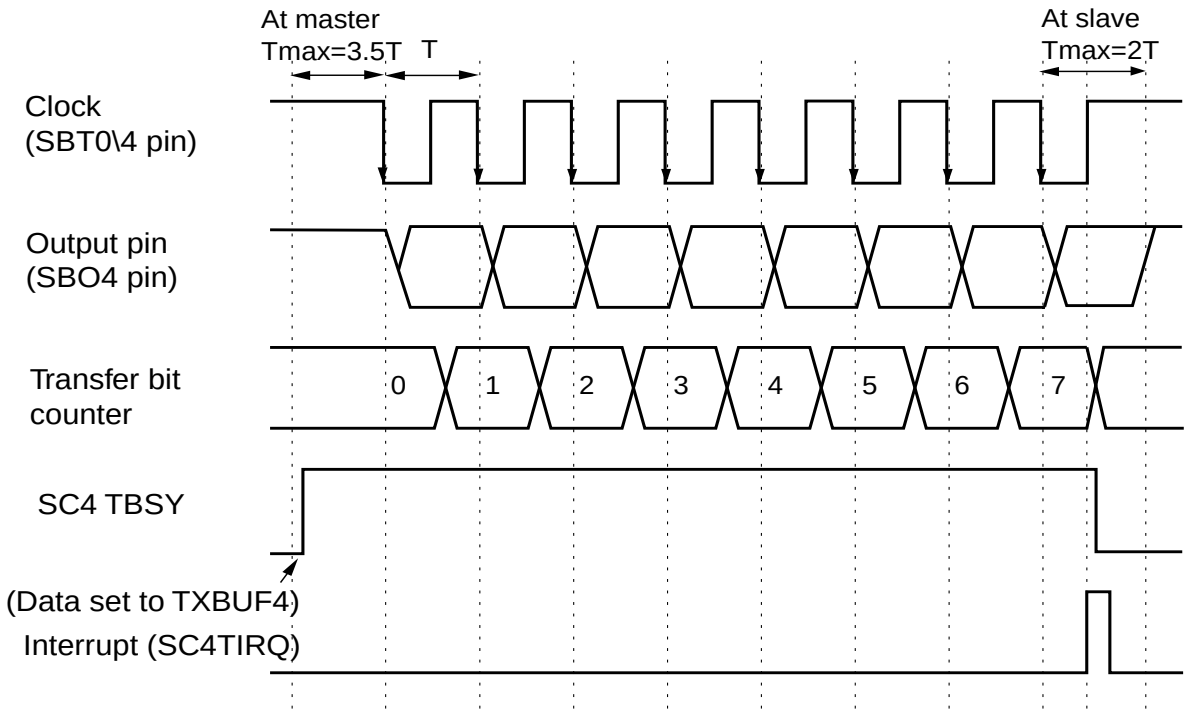


Figure:15.3.7 Transmission Timing (at falling edge, start condition is disabled)

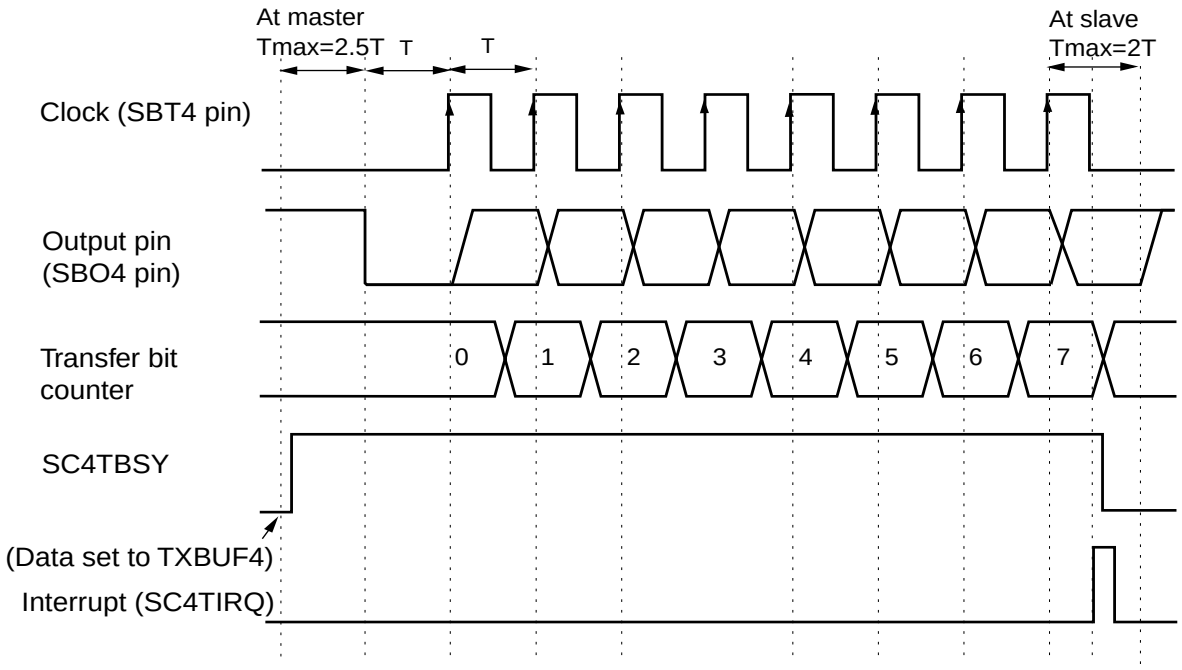


Figure:15.3.8 Transmission Timing (at rising edge, start condition is enabled)

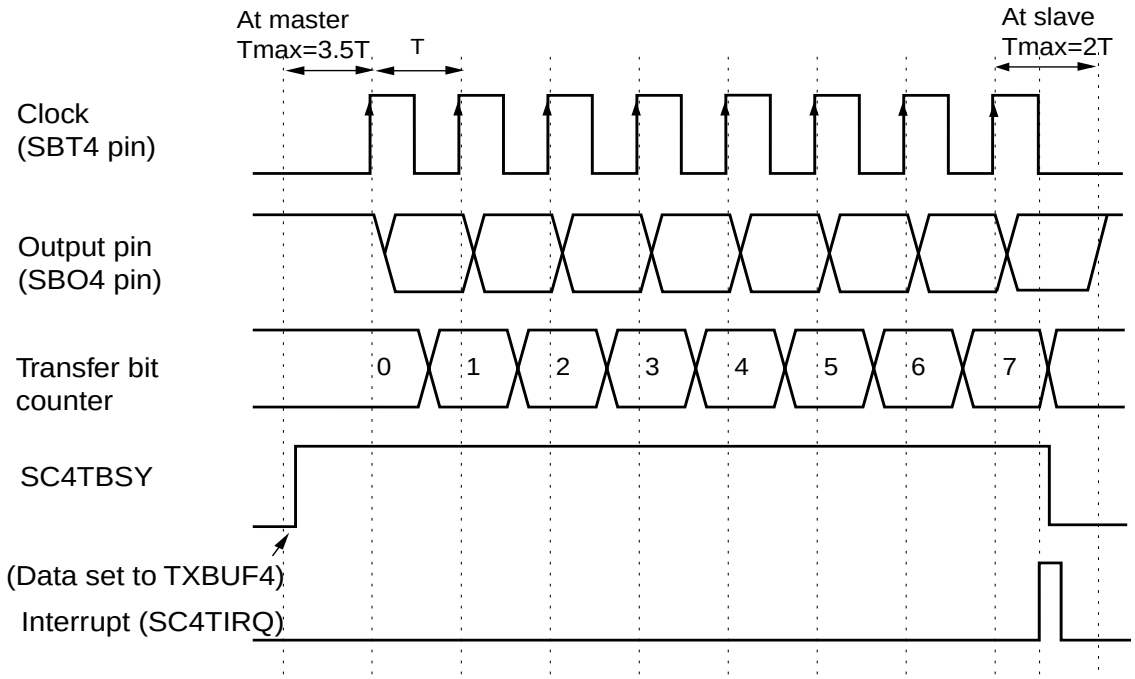


Figure:15.3.9 Transmission Timing (at rising edge, start condition is disabled)

■ Reception Timing

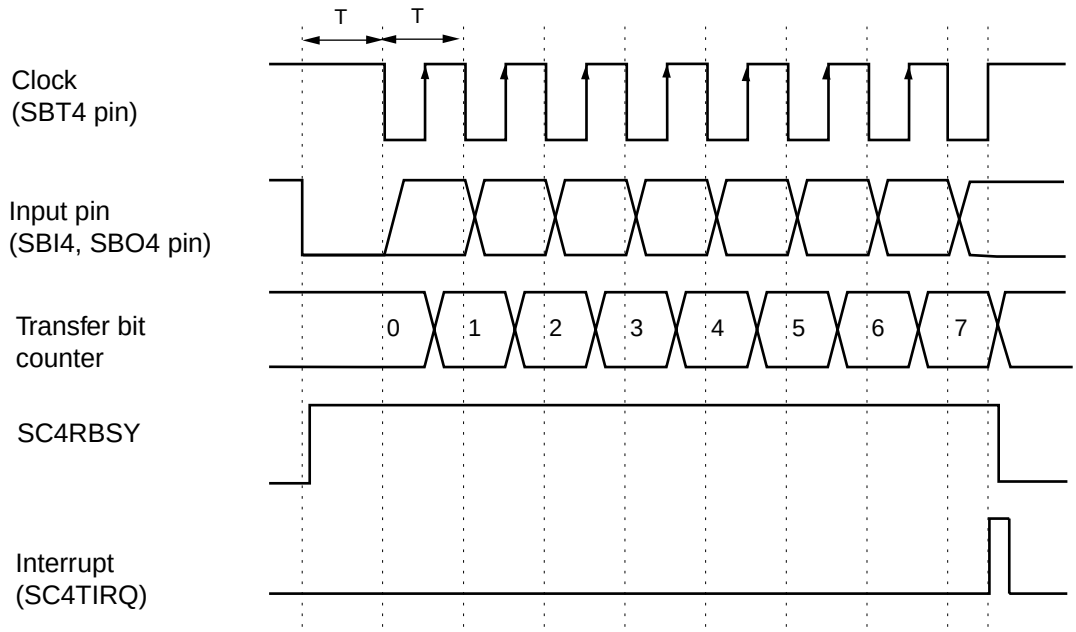


Figure:15.3.10 Reception Timing (at rising edge, start condition is enabled)

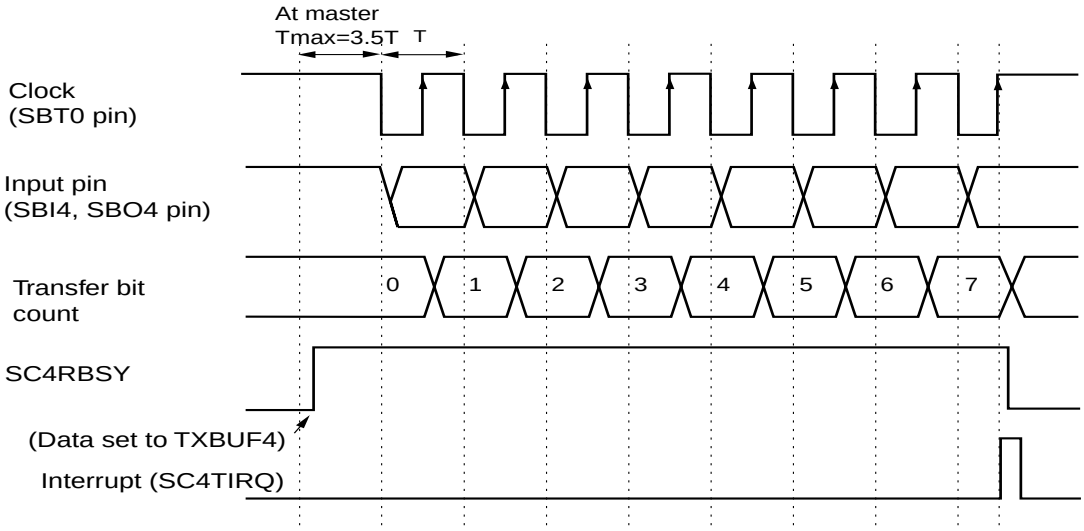


Figure:15.3.11 Reception Timing (at rising edge, start condition is disabled)

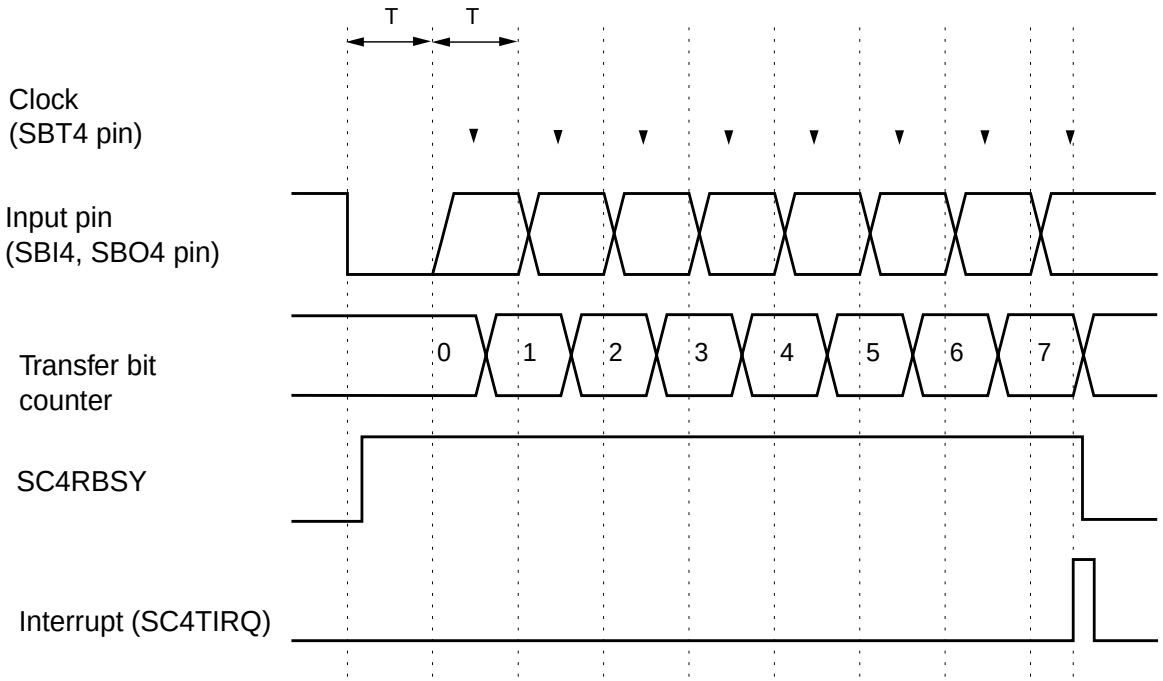


Figure:15.3.12 Reception Timing (at falling edge, start condition is enabled)

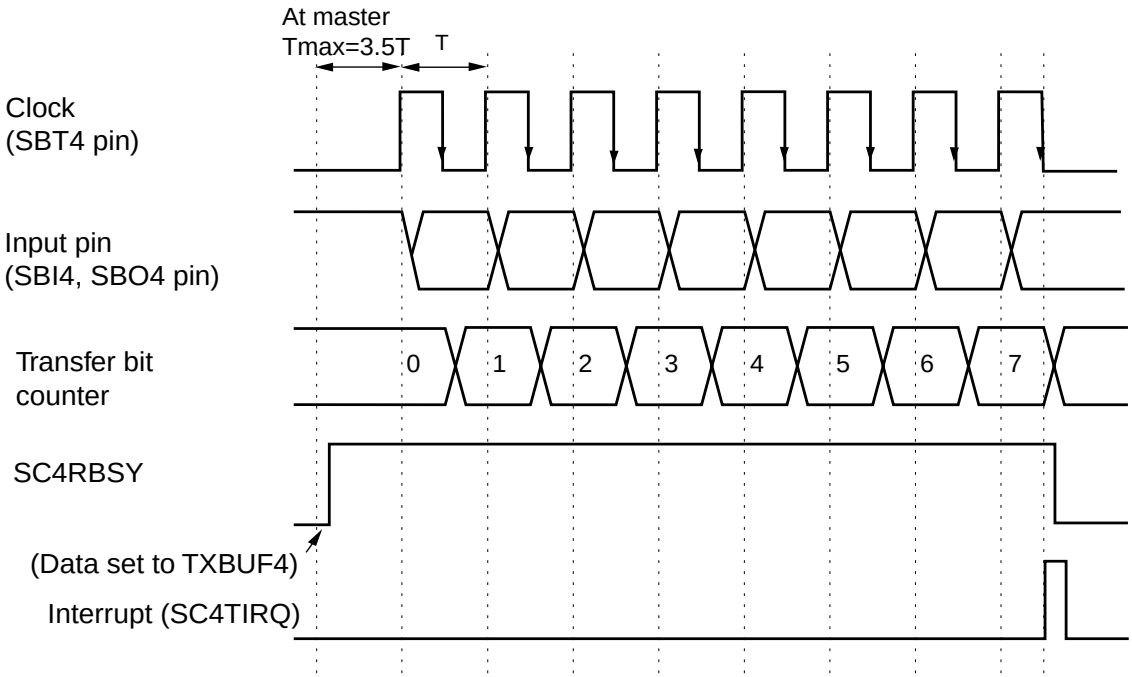


Figure:15.3.13 Reception Timing (at falling edge, start condition is disabled)

■ Transmission/ Reception Timing

When transmission and reception are operated at the same time, set the SC4CE1 flag of the SC4MD0 register to "0" or "1". Data is received at the opposite output edge of the transmission data, so that the input edge of the received data should be the opposite output edge of the transmission data from the other side.

Also, in the case transmission/ reception is done with the start condition, opposite of the communication should be done with the same condition to communicate properly.

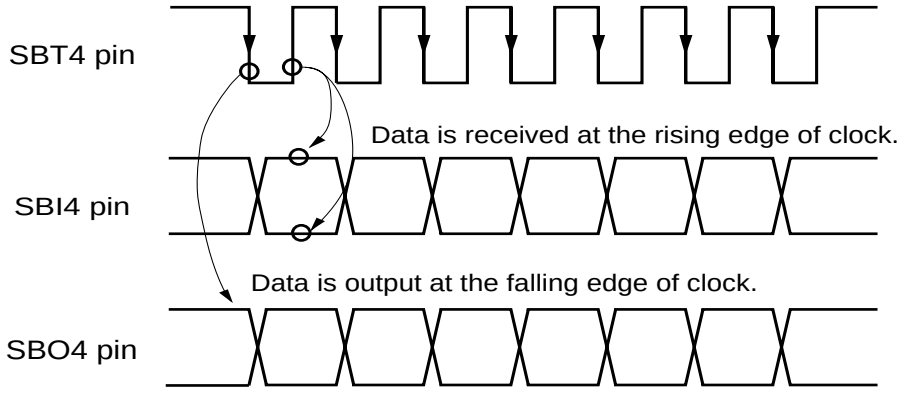


Figure:15.3.14 Transmission/ Reception Timing (Reception:at rising edge, Transmission:at falling edge)

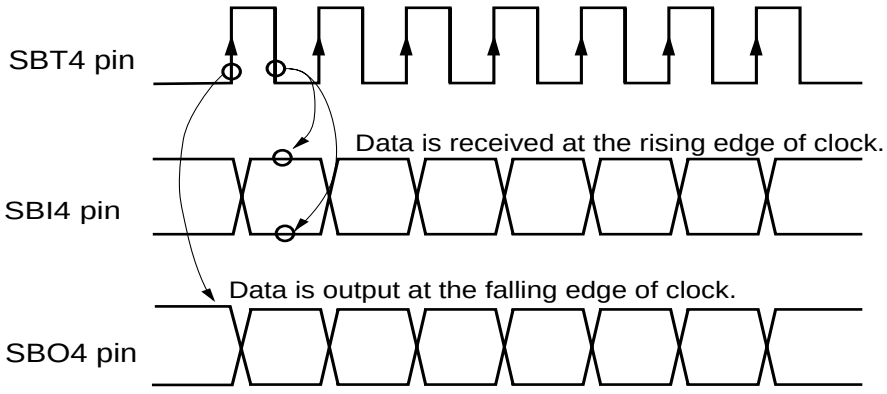


Figure:15.3.15 Transmission/ Reception Timing
(Reception:at falling edge, Transmission:at rising edge)

■ Communication Function at Standby Mode

This serial interface has the following way about the return from the standby mode.

This serial interface can do the slave reception at the standby mode. CPU operation status can be recovered from standby to normal by the communication complete interrupt SC4TIRQ that is generated after the slave reception.

(At the standby mode, if the transfer bit count data is received once that is set by the SC4LNG2 to 0 flag of the SC4MD0 register, the continuous reception is not available because the next data is not allowed.) The received data should be read out from the received data buffer RXBUF4 after recovering the normal mode.

In the reception at the standby mode, the communication with enabled start condition is not available. Disable the start condition. The dummy data should be set to the transmission data buffer TXBUF4 before the transition to the standby mode.

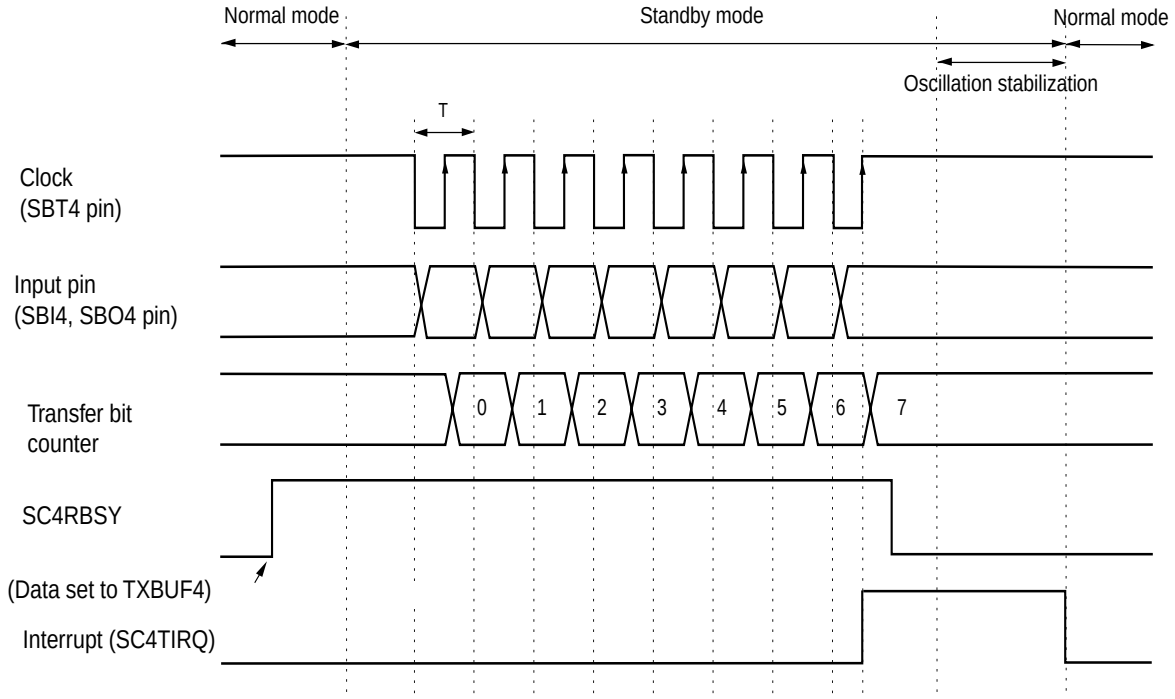


Figure:15.3.16 Reception Timing at Standby Mode (Reception:at rising edge, start condition is disabled)

■ Pins Setup (with 3 channels, at transmission)

Table:15.3.7 shows the setup for synchronous serial interface pin with 3 channels (SBO4 pin, SBI4 pin, SBT4 pin) at transmission.

Table:15.3.7 Setup for Synchronous Serial Interface Pin (with 3 channels, at transmission)

Setup item	Data output pin	Data input pin	Clock I/O pin	
	SBO4 pin	SBI4 pin	SBT4 pin	
			Clock master	Clock slave
			SC4MD1(SC4MST)	
Port pin	P40	P41	P42	
Serial data input selection	SBI4		-	
	SC4MD1(SC4IOM)			
Function	Serial data output	"1" input	Transfer clock input/ output	Transfer clock input/ output
	SC4MD1(SC4SBOS)	SC4MD1(SC4SBIS)	SC4MD1(SC4SBTS)	
Style	Push-pull/ Nch open-drain	-	Push-pull/ Nch open-drain	Push-pull/ Nch open-drain
	P4ODC(P4ODC0)		P4ODC(P4ODC2)	
I/O	Output mode	-	Output mode	Input mode
	P4DIR(P4DIR0)		P4DIR(P4DIR2)	
Pull-up setup	Added/ Not added	-	Added/ Not added	Added/ Not added
	P4PLU(P4PLU0)		P4PLU(P4PLU2)	

■ Pins Setup (with 3 channels, at reception)

Table:15.3.8 shows the setup for synchronous serial interface pin with 3 channels (SBO4 pin, SBI4 pin, SBT4 pin) at reception.

Table:15.3.8 Setup for Synchronous Serial Interface Pin (with 3 channels, at reception)

Setup item	Data output pin	Data input pin	Clock I/O pin	
	SBO4A pin	SBI4 pin	SBT4 pin	
			Clock master	Clock slave
			SC4MD1(SC4MST)	
Port pin	P40	P41	P42	
Serial data input selection	SBI4		-	
	SC4MD1(SC4IOM)			
Function	Port	Serial input	Transfer clock input/ output	Transfer clock input/ output
	P4DIR(P4DIR0)	SC4MD1(SC4SBIS)	SC4MD1(SC4SBTS)	
Style	-	-	Push-pull/ Nch open-drain	Push-pull/ Nch open-drain
			P4ODC(P4ODC2)	
I/O	-	Input mode	Output mode	Input mode
		P4DIR(P4DIR1)	P4DIR(P4DIR2)	
Pull-up setup	-	-	Added/ Not added	Added/ Not added
			P4PLU(P4PLU2)	

■ Pins Setup (with 3 channels, at transmission / reception)

Table:15.3.9 shows the setup for synchronous serial interface pin with 3 channels (SBO4 pin, SBI4 pin, SBT4 pin) at transmission / reception.

Table:15.3.9 Setup for Synchronous Serial Interface Pin (with 3 channels, at transmission / reception)

Setup item	Data output pin	Data input pin	Clock I/O pin	
	SBO4 pin	SBI4 pin	SBT4 pin	
			Clock master	Clock slave
			SC4MD1(SC4MST)	
Port pin	P40	P41	P42	
Serial data input selection	SBI4		-	
	SC4MD1(SC4IOM)			
Function	Serial data output	Serial input	Transfer clock input/ output	Transfer clock input/ output
	SC4MD1(SC4SBOS)	SC4MD1(SC4SBIS)	SC4MD1(SC4SBTS)	
Style	Push-pull/ Nch open-drain	-	Push-pull/ Nch open-drain	Push-pull/ Nch open-drain
	P4ODC(P4ODC0)		P4ODC(P4ODC2)	
I/O	Output mode	Input mode	Output mode	Input mode
	P4DIR(P4DIR0)	P4DIR(P4DIR1)	P4DIR(P4DIR2)	
Pull-up setup	Added/ Not added	-	Added/ Not added	Added/ Not added
	P4PLU(P4PLU0)		P4PLU(P4PLU2)	

■ Pins Setup (with 2 channels, at transmission)

Table:15.3.10 shows the setup for synchronous serial interface pin with 2 channels (SBO4 pin, SBT4 pin) at transmission. SBI4 pin can be used as a port.

Table:15.3.10 Setup for Synchronous Serial Interface Pin (with 2 channels, at transmission)

Setup item	Data output pin	Serial unused pin	Clock I/O pin	
	SBO4 pin	SBI4 pin	SBT4 pin	
			Clock master	Clock slave
			SC4MD1(SC4MST)	
Port pin	P40	P41	P42	
Serial data input selection	SBI4		-	
	SC4MD1(SC4IOM)			
Function	Serial data input	"1" input	Transfer clock input/ output	Transfer clock input/ output
	SC4MD1(SC4SBOS)	SC4MD1(SC4SBIS)	SC4MD1(SC4SBIS)	
Style	Push-pull/ Nch open-drain	-	Push-pull/ Nch open-drain	Push-pull/ Nch open-drain
	P4ODC(P4ODC0)		P4ODC(P4ODC2)	
I/O	Output mode	-	Output mode	Input mode
	P4DIR(P4DIR0)		P4DIR(P4DIR2)	
Pull-up setup	Added/ Not added	-	Added/ Not added	Added/ Not added
	P4PLU(P4PLU0)		P4PLU(P4PLU2)	

■ Pins Setup (with 2 channels, at reception)

Table:15.3.11 shows the setup for synchronous serial interface pin with 2 channels (SBO4 pin, SBT4 pin) at reception. SBI4 pin can be used as a port.

Table:15.3.11 Setup for Synchronous Serial Interface Pin (with 2 channels, at reception)

Setup item	Data output pin	Serial unused pin	Clock I/O pin	
	SBO4 pin	SBI4 pin	SBT4 pin	
			Clock master	Clock slave
			SC4MD1(SC4MST)	
Port pin	P40	P41	P42	
Serial data input selection	SBI4		-	
	SC4MD1(SC4IOM)			
Function	Port	Serial input	Transfer clock input/ output	Transfer clock input/ output
	SC4MD1(SC4SBOS)	SC4MD1(SC4SBIS)	SC4MD1(SC4SBIS)	
Style	-	-	Push-pull/ Nch open-drain	Push-pull/ Nch open-drain
			P4ODC(P4ODC2)	
I/O	Input mode	-	Output mode	Input mode
	P4DIR(P4DIR0)		P4DIR(P4DIR2)	
Pull-up setup	-	-	Added/ Not added	Added/ Not added
			P4PLU(P4PLU2)	

15.3.2 Setup Example

■ Transmission / Reception Setup Example

The setup example for clock synchronous serial communication with serial 4 is shown. Table:15.3.12 shows the conditions at transmission / reception.

Table:15.3.12 Setup Examples for Synchronous Serial Interface Transmission / Reception

Setup item	Set to
Serial data input pin	Independent (3 channels)
Transfer bit count	8 bit
Start condition	None
First transfer bit	MSB
Input edge	Falling edge
Output edge	Rising edge
Clock	Clock master
Clock source	fs/2
Clock source 1/8 dividing	Not divided by 8
SBT4/SBO4 pin style	Nch open-drain
SBT4 pin pull-up resistor	Added
SBO4 pin pull-up resistor	Added
serial 4 communication complete interrupt	Enable
SBO4 output after last data output	"1"(H) fix

An example setup procedure, with a description of each step is shown below.

Setup Procedure	Description
(1) Select the prescaler operation SC4MD3(0x03FAE) bp3 :SC4PSCE =1	(1) Set the SC4PSCE flag of the SC4MD3 register to "1" to select "prescaler operation".
(2) Select the clock source SC4MD3(0x03FAE) bp2-0 :SC4PSC2-0 =100	(2) Set the SC4PSC2 to 0 flag of the SC4MD3 register to "100" to select the fs/2 to clock source.
(3) SBO4A output control after the last data output SC4MD3(0x03FAE) bp7,6 :SC4FDC1-0 =00	(3) Set the SC4FDC1 to 0 flag of the SC4MD3 register to "00" to select "1" (High) fix of the SBO4 last data output.

Setup Procedure	Description
(4) Control of pin type. P4ODC (0x03F3C) bp2 :P4ODC2 =1 bp0 :P4ODC0 =1 P4PLU(0x03F44) b2 :P4PLU2 =1 bp0 :P4PLU0 =1	(4) Set the P4ODC2, P4ODC0 flags of the P4ODC register to "1, 1" to select open-drain for the SBO4/SBT4 pin type. Set the P4PLU2, P4PLU0 flags of the P4PLU register to "1, 1" to select enable pull-up resistor.
(5) Control the pin direction P4DIR(0x03F34) bp2 :P4DIR2 =1 bp1 :P4DIR1 =0 bp0 :P4DIR0 =1	(5) Set the P4DIR2, P4DIR0 flag of the Port 4 pin direction control register (P4DIR) to "1,1" and the P4DIR3 flag to "0" to set P42, P40 to the output mode, P41 to the input mode.
(6) Set the SC4MD0 register Select the transfer bit count SC4MD0(0x03FAB) bp2-0 :SC4LNG2-0 =111 Select the start condition SC4MD0(0x03FAB) bp3 :SC4STE =0 Select the first bit to be transferred SC4MD0(0x03FAB) bp4 :SC4DIR =0 Select the transfer edge SC4MD0(0x03FAB) bp7 :SC4CE1 =1	(6) Set the SC4LNG2 to 0 flag of the serial 4 mode register 0 (SC4MD0) to "111" to set the transfer bit count "8 bits". Set the SC4STE flag of the SC4MD0 register to "0" to disable the start condition. Set the SC4DIR flag of the SC4MD0 register to "0" to set MSB as a transfer first bit. Set the SC4CE1 flag of the SC4MD0 register to "1" to set the reception data input edge "falling" and the transmission data output edge "rising".
(7) Set the SC4MD1 register Select the communication style SC4MD1(0x03FAC) bp0 :SC4CMD =0 Select the transfer clock SC4MD1(0x03FAC) bp2 :SC4MST =1 bp3 :SC4CKM =0 Select the transfer clock SC4MD1(0x03FAC) bp4 :SC4SBOS =1 bp5 :SC4SBIS =1 bp6 :SC4SBTS =1 bp7 :SC4IOM =0	(7) Set the SC4CMD flag of the SC4MD1 register to "0" to select the synchronous serial. Set the SC4MST flag of the SC4MD1 register to "0" to select the clock master (internal clock). Set the SC4CKM flag to "0" to select "not divided by 8" for the clock source. Set the SC4SBOS, SC4SBIS, SC4SBTS flag of the SC4MD1 register to "1" to set the SBO4 pin to the serial data output, the SBI4 pin to the serial input, SBT4 pin to the transfer clock input/output. Set the SC4IOM flag "0" to set the serial data input from the SBI4 pin.
(8) Set the interrupt level SC4TICR(0x03FF9) bp7-6 :SC4LV1-0 =10	(8) Set the interrupt level by the SC4TLV1 to 0 flag of the serial 4 UART transmission interrupt control register (SC4TICR).
(9) Enable the interrupt SC4TICR(0x03FF9) bp1 :SC4TIE =1	(9) Set the SC4TIE flag of the SC4TICR register to "1" to enable the interrupt. If any interrupt request flag (SC4TIR of the SC4TICR register) is already set, clear SC4TIR before the interrupt is enabled.

Setup Procedure	Description
(10) Start the serial transmission Transmission data ý TXBUF4(0x03FB1) Received data ý input SBI4 pin	(10) Set the transmission data to the serial transmission data buffer TXBUF4. The transmission or reception is started by the internal clock generation. When the transmission finished, the serial 4 UART transmission interrupt SC4TIRQ is generated. [Chapter 3. 3-1-4 Setup]

Each procedure (1) to (3), (6), and (8) can be set at the same time.

When only reception with 3 channels is operated, set the SC4SBIS of the SC4MD1 register to "0" and set the serial input to "1" input. The SBI4 pin can be used as a general port. Also, when only transmission is operated, set the SC4SBOS of the SC4MD1 register to "0" to select a port.

When communicate with 2 channels, the SBO4 pin inputs / outputs serial data. The port direction control register P4DIR switches I/O. At reception, set SC4SBIS of the SC4MD1 register to "1", always, to select "serial input". The SBI4 pin can be used as a general port.

This serial interface contains a emergency reset function. If the communication should be stopped by force, set SC4SBOS and SC4SBIS of the SC4MD1 register to "0".

Each flag should be set as this setup procedure in order. Activation of communication should be operated after all control registers (refer to Table:15.2.1 except TXBUF4) are set.

Transfer rate of transfer clock set by the SC4MD3 register should be under 5.0 MHz.

■ Transmission / Reception Setup Example (Standby Mode Reception)

The setup example for clock synchronous serial communication with serial 4 is shown. Table:15.3.13 shows the condition at standby mode reception.

Table:15.3.13 Setup Examples for Synchronous Serial Interface Transmission / Reception (Standby Mode Reception)

Setup item	Set to
Serial data input pin	Select SBI4
Transfer bit count	8 bit
Start condition	None
First transfer bit	MSB
Input edge	Falling edge
Clock	Clock slave
Operation mode	Stop mode
Clock source	fs/2
Clock source 1/8 dividing	Not divided by 8
SBT4/SBO4 pin style	Push-pull
SBT4 pin pull-up resistor	Not added
SBO4 pin pull-up resistor	Not added
serial 4 communication complete interrupt	Enable

An example setup procedure, with a description of each step is shown below.

Setup Procedure	Description
(1) Select the prescaler operation SC4MD3(0x03FAE) bp3 :SC4PSCE =1	(1) Set the SC4PSCE flag of the SC4MD3 register to "1" to select "prescaler operation".
(2) Select the clock source SC4MD3(0x03FAE) bp2-0 :SC4PSC2-0 =100	(2) Set the SC4PSC2 to 0 flag of the SC4MD3 register to "100" to select fs/2 as the clock source.
(3) Control of pin type. P4ODC (0x03F3C) bp2 :P4ODC2 =0 bp1 :P4ODC1 =0 P4PLU(0x03F44) bp2 :P4PLU2 =0 bp1 :P4PLU1 =0	(3) Set the P4ODC2, P4ODC1 flags of the P4ODC register to "0,0" to select push-pull for the SBI4/SBT4 pin type. Set the P4PLU2, P4PLU1 flags of the P4PLU register to "0,0" to select disable pull-up resistor.

Setup Procedure	Description
(4) Control the pin direction P4DIR(0x03F34) bp2 :P4DIR2 =0 bp1 :P4DIR1 =0 bp0 :P4DIR0 =1	(4) Set the P4DIR2, P4DIR3 flag of the Port 4 pin direction control register (P4DIR) to "0,0" to set P42, P41 to the input mode.
(5) ÏSelect the transfer bit count SC4MD0(0x03FAB) bp2-0 :SC4LNG2-0 =111	(5) Set the SC4LNG2 to 0 flag of the serial 4 mode register (SC4MD0) to "111" to set the transfer bit count "8 bits".
(6) Select the start condition SC4MD0(0x03FAB) bp3 :SC4STE =0	(6) Set the SC4LNG2 to 0 flag of the serial 4 mode register (SC4MD0) to "111" to disable the start condition.
(7) Select the first bit to be transferred SC4MD0(0x03FAB) bp4 :SC4DIR =0	(7) Set the SC4DIR flag of the SC4MD0 register to "0" to set MSB as a transfer first bit.
(8) Select the transfer edge SC4MD0(0x03FAB) bp7 :SC4CE1 =1	(8) Set the SC4CE1 flag of the SC4MD0 register to "1" to set the reception data input edge "falling".
(9) Select the communication type SC4MD1(0x03FAC) bp0 :SC4CMD =0	(9) Set the SC4CMD flag of the SC4MD1 register to "0" to select the synchronous serial.
(10) Select the transfer clock SC4MD1(0x03FAC) bp2 :SC4MST =0 bp3 :SC4CKM =0	(10) Set the SC4MST flag of the SC4MD1 register to "0" to select the clock slave (external slave). Set the SC4CKM flag to "0" to select "not divided by 8" for the clock source.
(11) Control the pin function SC4MD1(0x03FAC) bp4 :SC4SBOS =0 bp5 :SC4SBIS =1 bp6 :SC4SBTS =1 bp7 :SC4IOM =0	(11) Set the SC4SBOS flag of the SC4MD1 register to "0", the SC4SBTS flag of the SC4SBIS register to "1" to set the SBI4 pin to the serial data input as the SBO4 pin general port, the SBT4 pin to the transfer clock input/ output. Set the SC4IOM flag "0" to set the serial data input from the SBI4 pin.
(12) Set the interrupt level SC4TICR(0x03FF9) bp7-6 :SC4LV1-0 =10	(12) Set the interrupt level by the SC4LV1 to 0 flag of the serial 4 UART transmission interrupt control register (SC4TICR). (Set level 2)
(13) Enable the interrupt SC4TICR(0x03FF9) bp1 :SC4TIE =1	(13) Set the SC4TIE flag of the SC4TICR register to "1" to enable the interrupt. If any interrupt request flag (SC4TIR of the SC4TICR register) is already set, clear SC4TIR before the interrupt is enabled. [Chapter 3. 3-1-4 Setup]
(14) Set the startup factor of the serial communication Dummy data ý TXBUF4(0x03FB1)	(14) Set the dummy data to the serial transmission data buffer TXBUF4.

Setup Procedure	Description
(15) Transfer to STOP mode CPUM(0x03F00) bp3:STOP =1	(15) Set the STOP flag of the CPUM register to "1" to transfer to the stop mode.
(16) Start the serial communication Transmission clock ý input SBT4 pin Received data ý input SBI4 pin	(16) Input the transfer clock to the SBT4 pin and transfer data to the SBI4 pin.
(17) Recover from the standby mode	(17) The serial 4 UART transmission interrupt SC4TIRQ is generated at the same time of the 8th bits data reception, then, CPU is recovered from the stop mode to the normal mode after the oscillation stabilization wait.

Note:Each procedure (1) to (2), (5) to (8), (9) to (11) can be set at the same time.

The slave reception at the standby mode should be used without the start condition to receive properly.

Each flag should be set as this setup procedure in order. Activation of communication should be operated after all control registers (refer to Table:15.2.1 except TXBUF4) are set.

15.3.3 UART Serial Interface

serial 4 can be used for full duplex UART communication. Table:15.3.14 shows UART serial interface functions.

Table:15.3.14 URAT Serial Interface Functions

Communication style	UART (full duplex)
Interrupt	SC4TIRQ (transmission), SC4RIRQ (reception)
Used pins	TXD4 (output / input) RXD4 (input)
Specification the first transfer bit	MSB / LSB
Selection of parity bit	O
Parity bit control	0 parity 1 parity odd parity even parity
Frame selection	7 bits + 1 STOP 7 bits + 2 STOP 8 bits + 1 STOP 8 bits + 2 STOP
Continuous operation	O
Maximum transfer rate	300 kbps (standard 300 bps to 38.4 kbps) (with baud rate timer)

■ Activation Factor for Communication

At transmission, if any data is set to the transmission data buffer TXBUF4, a start condition is generated to start transfer. At reception, if a start condition is received, communication is started. At reception, if the data length of "L" for start bit is longer than 0.5 bit, that can be regarded as a start condition.

■ Transmission

Data transfer is automatically started by setting data to the transmission data buffer TXBUF4. When the transmission is completed, the serial 4 transmission interrupt SC4TIRQ is generated.

■ Reception

Once a start condition is received, reception is started after the transfer bit counter that counts transfer bit is cleared. When the reception is completed, the serial 4 reception interrupt SC4RIRQ is generated.

■ Full duplex communication

On full duplex communication, the transmission and reception can be operated separately at the same time. The frame mode and parity bit of the used data on transmission / reception should have the same polarity.

■ Transfer Bit Count Setup

The transfer bit count is automatically set after the frame mode is specified by the SC4FM1 to 0 flag of the SC4MD2 register. If the SC4CMD flag of the SC4MD1 register is set to "1", and UART communication is selected, the setup by the synchronous serial transfer bit count selection flag SC4LNG2 to 0 is no more valid.

■ Data Input Pin Setup

The communication mode can be selected from with 2 channels (data output pin (TXD4 pin), data input pin (RXD4 pin)), or with 1 channel (data I/O pin TXD4 pin). The RXD4 pin can be used only for serial data input. The TXD4 pin can be used for serial data input or output. The SC4IOM flag of the SC4MD1 register can specify which pin, RXD4 or TXD4 inputs the serial data. If "data input from TXD4 pin" is selected to be with 1 line communication, transmission / reception is switched by controlling TXD4 pin's direction by the P4DIR0 flag of the P4DIR register. At the same time, the RXD4 pin can be used as a general port.

■ Reception Buffer Empty Flag

When SC4RIRQ is generated, data is stored to RXBUF4 from the internal shift register, automatically. If data is stored to RXBUF4 from the shift register, the reception buffer empty flag SC4REMP of the SC4STR register is set to "1". That indicates that the received data is going to be read out. SC4REMP is cleared to "0" by reading out the data of RXBUF4.

■ Reception BUSY Flag

When the start condition is regarded, the SC4RBSY flag of the SC4STR register is set to "1". That is cleared to "0" by the generation of the reception complete interrupt SC4TIRQ. If the SC4SBIS flag is set to "0" during reception, the SC4RBSY flag is reset to "0".

■ Transmission BUSY Flag

When any data is set to TXBUF4, the SC4TBSY flag of the SC4STR register is set to "1". That is cleared to "0" by the generation of the transmission complete interrupt SC4TIRQ. During continuous communication the SC4TBSY flag is always set. If the transmission buffer empty flag SC4TEMP is set to "0" as the transmission complete interrupt SC4TIRQ is generated, the SC4TBSY is cleared to "0". If the SC4SBOS flag is set to "0", the SC4TBSY flag is reset to "0".

■ Frame Mode and Parity Check Setup

Figure 11-3-17 shows the data format at UART communication.

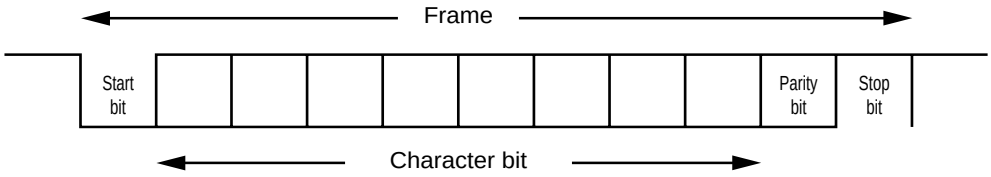


Figure:15.3.17 UART Serial Interface Transmission / Reception Data Format

The transmission / reception data consists of start bit, character bit, parity bit and stop bit. Table:15.3.15 shows its kinds to be set.

Table:15.3.15 UART Serial Interface Transmission / Reception Data

Start bit	1 bit
Character bit	7,8 bit
Parity bit	fixed to 0, fixed to 1, odd, even, none
Stop bit	1,2 bits

The SC4FM1 to 0 flag of the SC4MD2 register sets the frame mode. Table:15.3.16 shows the UART serial interface frame mode settings. If the SC4CMD flag of the SC4MD1 register is set to "1", and UART communication is selected, the transfer bit count on the SC4LNG2 to 0 flag of the SC4MD0 register is no more valid.

Table:15.3.16 UART Serial Interface Frame Mode

SC4MD2 register		Frame mode
SC4FM1	SC4FM0	
0	0	Character bit 7 bits + Stop bit 1 bit
0	1	Character bit 7 bits + Stop bit 2 bits
1	0	Character bit 8 bits + Stop bit 1 bit
1	1	Character bit 8 bits + Stop bit 2 bits

Parity bit is to detect wrong bits with transmission / reception data. Table:15.3.17 shows kinds of parity bit. The SC4NPE, SC4PM1 to 0 flag of the SC4MD2 register set parity bit.

Table:15.3.17 Parity Bit of UART Serial Interface

SC4MD2			Parity bit	Setup
SC4NPE	SC4PM1	SC4PM0		
0	0	0	Fixed to 0	Set parity bit to "0"
0	0	1	Fixed to 1	Set parity bit to "1"
0	1	0	Odd parity	Control that the total of "1" of parity bit and character bit should be odd
0	1	1	Even parity	Control that the total of "1" of parity bit and character bit should be even
1	-	-	None	Do not add parity bit

■ Break Status Transmission Control Setup

The SC4BRKE flag of the SC4MD2 register generates the brake status. If SC4BRKE is set to "1" to select the brake transmission, all bits from start bits to stop bits transfer "0".

■ Reception Error

At reception, there are 3 types of error; overrun error, parity error and framing error. Reception error can be determined by the SC4ORE, SC4PEK, SC4FEF flag of the SC4STR register. Even one of those errors is detected, the SC4ERE flag of the SC4STR register is set to "1". SC4PEK, the SC4FEF flags in reception error flag are renewed at generation of the reception complete interrupt SC4RIRQ. The SC4ORE flag is cleared at the same time of next communication complete interrupt SC4RIRQ generation after the data of the RXBUF4 is read out. The decision of the received error flag should be operated until the next communication is finished. Those error flag has no effect on communication operation. Table:15.3.18 shows the list of reception error source.

Table:15.3.18 Reception Error Source of UART Serial Interface

Flag	Error		
SC4ORE	Overrun error	Next data is received before reading the receive buffer	
SC4PEK	Parity error	at fixed to 0	when parity bit is "1"
		at fixed to 1	When parity bit is "0"
		Odd parity	The total of "1" of parity bit and character bit is even
		Even parity	The total of "1" of parity bit and character bit is odd
SC4FEF	Framing error	Stop bit is not detected	

■ Judgement of Break Status Reception

Reception at break status can be judge. If all received data from start bit and stop bit is "0", the SC4BRKF flag of the SC4MD2 register is set and regards the break status. The SC4BRKF flag is set at generation of the reception complete interrupt SC4RIRQ.

■ Continuous Communication

This serial interface has continuous communication function. If data is set to the transmission data buffer TXBUF4 during communication, the transmission buffer empty flag SC4TEMP is set to continue automatic communication. This does not generate any blank in communication. Set data to TXBUF between previous data setup and generation of the communication complete interrupt SC4TIRQ.

■ Clock Setup

Transfer clock is not necessary for UART communication itself, but necessary for setup of data transmission / reception timing in the serial interface.

Select the timer to be used as a baud rate timer by the SC4MD3 register.

■ Receive Bit Count and First Transfer Bit

In the case of reception, when the transfer bit count is 7 bits, the data storing method to the received data buffer RXBUF4 is different depending on the first transfer bit selection. At MSB first, data are stored to the upper bits of RXBUF4. When there are 7 bits to be transferred, as shown on Table:15.3.18, if data "G" to "A" are stored to bp7 to bp1 of RXBUF4. At LSB first, data are stored to the lower bits of RXBUF4. When there are 7 bits to be transferred, as shown on Table:15.3.19, if data "A" to "G" are stored to bp0 to bp6 of RXBUF4.

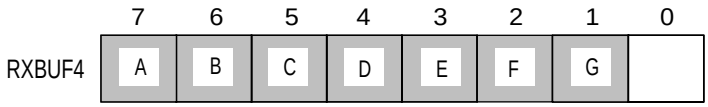


Figure:15.3.18 Transfer Bit Count and First Transfer Bit (starting with MSB)

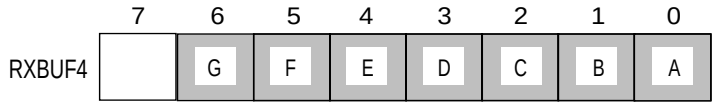


Figure:15.3.19 Transfer Bit Count and First Transfer Bit (starting with LSB)

The following items are the same as clock synchronous serial.

■ First Transfer Bit Setup

Refer to:XV-13

■ Transmission Data Buffer

Refer to:XV-13

■ Received Data Buffer

Refer to:XV13

■ Transfer Bit Count and First Transfer Bit

Refer to:XV-14

■ Transmission Buffer Empty Flag

Refer to:XV-18

■ Emergency Reset

Refer to:XV-19

■ Transmission Timing

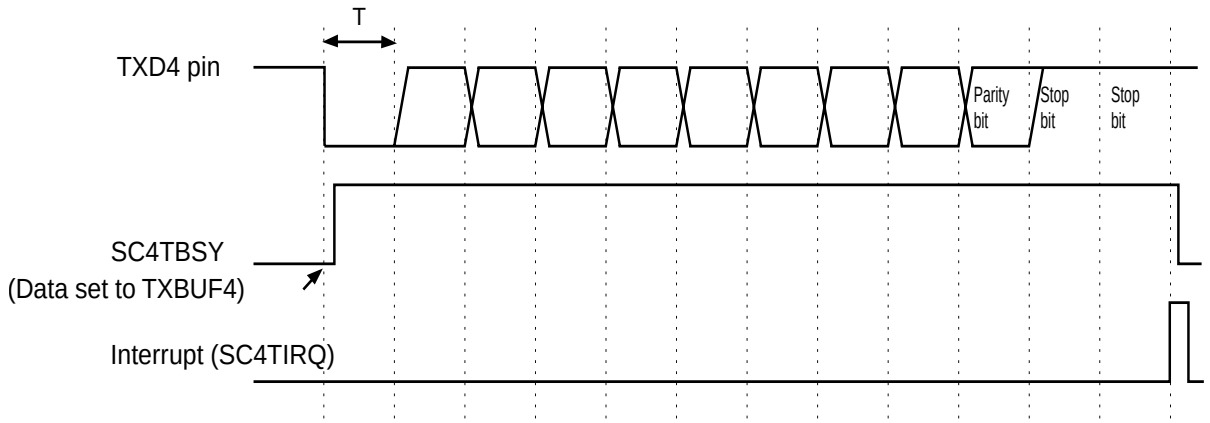


Figure:15.3.20 Transmission Timing (parity bit is enabled)

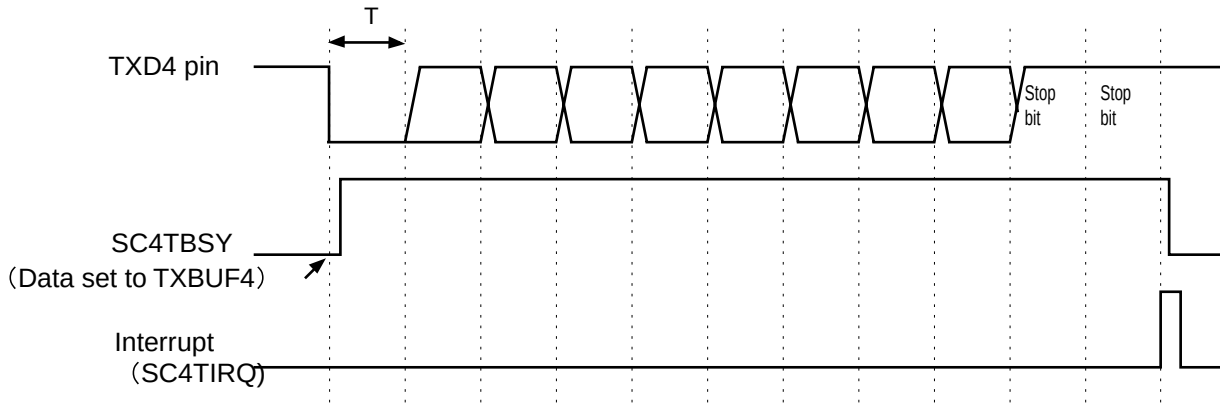


Figure:15.3.21 Transmission Timing (parity bit is disabled)

■ Reception Timing

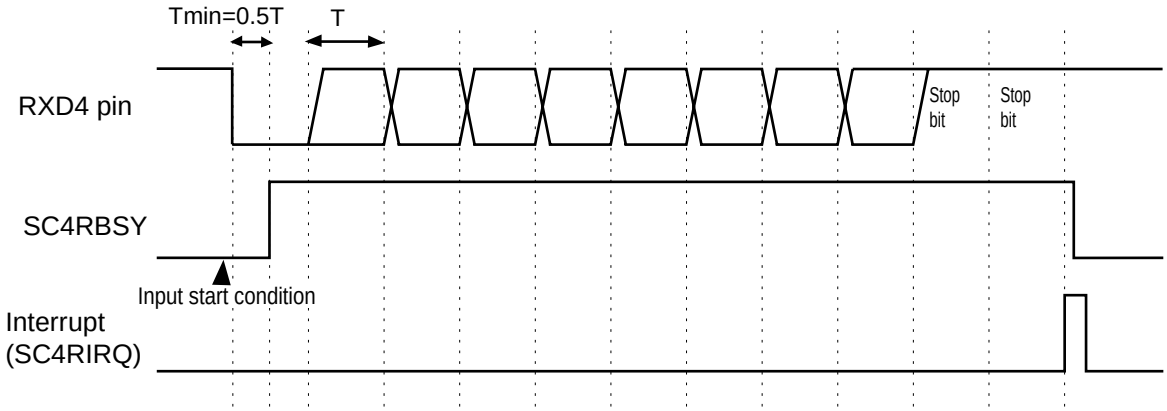


Figure:15.3.22 Reception Timing (parity bit is enabled)

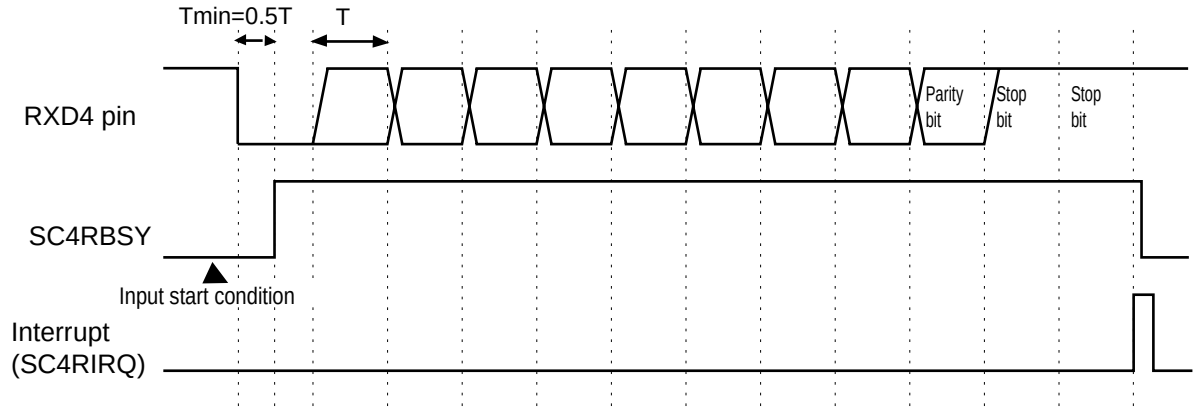


Figure:15.3.23 Reception Timing (parity bit is disabled)

■ Transfer Speed Setup

Baud rate timer (timer 1, timer 2) can set any transfer rate. Table:15.3.19 shows the setup example of the transfer speed.

Table:15.3.19 UART Serial Interface Transfer Speed

Setup	Register	Page
Serial 4 clock source (timer 2 , timer 5)	SC4MD3	XV-10
Timer 2 clock source	TM2MD	V-19
Timer 2 compare register	TM2OC	V-14
Timer 5 clock source	TM5MD	V-22
Timer 5 compare register	TM5OC	V-15

Timer compare register is set as follows;

baud rate = 1 / (overflow cycle $\times$ 2 $\times$ 8) ("8" means that clock source is divided by 8)

overflow cycle = (set value of compare register + 1)$\times$ timer clock cycle

therefore,

set value of compare register = timer clock frequency / (baud rate $\times$ 2 $\times$ 8) - 1

For example, if baud rate should be 300 bps at timer clock source fs/4 (fosc = 8 MHz, fs = fosc/2), set value should be as follows;

Set value of compare register = $(8 \times 10^6 / 2 / 4) / (300 \times 2 \times 8) - 1$

= 207

= 0xCF

Timer clock source and the set value of timer compare register at the standard rate are shown in the following page.

Transfer rate should be selected under 300 kbps.

fosc (MHz)	Clock source (Timer)	Transfer Speed (bit/s)									
		300		960		1200		2400		4800	
		Set Value	caluculated value	Set Value	caluculated value	Set Value	caluculated value	Set Value	caluculated value	Set Value	caluculated value
4.00	fosc	-	-	-	-	207	1202	103	2404	51	4808
	fosc/4	207	300	64	962	51	1202	25	2404	12	4808
	fosc/16	51	300	-	-	12	1202	-	-	-	-
	fosc/32	25	300	-	-	-	-	-	-	-	-
	fosc/64	12	300	-	-	-	-	-	-	-	-
	fs/2	207	300	64	962	51	1202	25	2404	12	4808
	fs/4	104	297	-	-	25	1202	12	2404	-	-
4.19	fosc	-	-	-	-	217	1201	108	2403	54	4761
	fosc/4	217	300	67	963	-	-	-	-	-	-
	fosc/16	-	-	16	963	-	-	6	2338	-	-
	fosc/32	-	-	-	-	-	-	-	-	-	-
	fosc/64	-	-	-	-	-	-	-	-	-	-
	fs/2	217	300	67	963	-	-	-	-	-	-
	fs/4	108	300	33	963	-	-	13	2338	-	-
8.00	fosc	-	-	-	-	-	-	207	2404	103	4808
	fosc/4	-	-	129	962	103	1202	51	2404	25	4808
	fosc/16	103	300	-	-	25	1202	12	2404	-	-
	fosc/32	51	300	-	-	12	1202	-	-	-	-
	fosc/64	25	300	-	-	-	-	-	-	-	-
	fs/2	-	-	129	962	103	1202	51	2404	25	4808
	fs/4	207	300	64	962	51	1202	25	2404	12	4808
8.38	fosc	-	-	-	-	-	-	217	2403	108	4805
	fosc/4	-	-	135	963	108	1201	-	-	-	-
	fosc/16	108	300	33	963	-	-	13	2338	-	-
	fosc/32	-	-	16	963	-	-	6	2338	-	-
	fosc/64	-	-	-	-	-	-	-	-	-	-
	fs/2	-	-	135	963	108	1201	-	-	-	-
	fs/4	217	300	67	963	-	-	-	-	-	-
12.00	fosc	-	-	-	-	-	-	-	-	155	4808
	fosc/4	-	-	194	962	155	1202	77	2404	38	4808
	fosc/16	155	300	-	-	38	1202	-	-	-	-
	fosc/32	77	300	-	-	-	-	-	-	-	-
	fosc/64	38	300	-	-	-	-	-	-	-	-
	fs/2	-	-	194	962	155	1202	77	2404	38	4808
	fs/4	-	-	-	-	77	1202	38	2404	-	-
16.00	fosc	-	-	-	-	-	-	-	-	207	4808
	fosc/4	-	-	-	-	207	1202	103	2404	51	4808
	fosc/16	207	300	64	962	51	1202	25	2404	12	4808
	fosc/32	103	300	-	-	25	1202	12	2404	-	-
	fosc/64	51	300	-	-	12	1202	-	-	-	-
	fs/2	-	-	-	-	207	1202	103	2404	51	4808
	fs/4	-	-	129	962	103	1202	51	2404	25	4808

Figure:15.3.24 Setup Value of UART Serial Interface Transfer Speed

		Transfer Speed (bit/s)									
fosc (MHz)	Clock source (Timer)	9600		19200		28800		31250		38400	
		Set Value	caluculated value	Set Value	caluculated value	Set Value	caluculated value	Set Value	caluculated value	Set Value	caluculated value
4.00	fosc	25	9615	12	19231	-	-	7	31250	-	-
	fosc/4	-	-	-	-	-	-	1	31250	-	-
	fosc/16	-	-	-	-	-	-	-	-	-	-
	fosc/32	-	-	-	-	-	-	-	-	-	-
	fosc/64	-	-	-	-	-	-	-	-	-	-
	fs/2	-	-	-	-	-	-	1	31250	-	-
	fs/4	-	-	-	-	-	-	-	-	-	-
4.19	fosc	26	9699	-	-	-	-	-	-	-	-
	fosc/4	-	-	-	-	-	-	-	-	-	-
	fosc/16	-	-	-	-	-	-	-	-	-	-
	fosc/32	-	-	-	-	-	-	-	-	-	-
	fosc/64	-	-	-	-	-	-	-	-	-	-
	fs/2	-	-	-	-	-	-	-	-	-	-
	fs/4	-	-	-	-	-	-	-	-	-	-
8.00	fosc	51	9615	25	19231	-	-	15	31250	12	38462
	fosc/4	12	9615	-	-	-	-	3	31250	-	-
	fosc/16	-	-	-	-	-	-	-	-	-	-
	fosc/32	-	-	-	-	-	-	-	-	-	-
	fosc/64	-	-	-	-	-	-	-	-	-	-
	fs/2	12	9615	-	-	-	-	3	31250	-	-
	fs/4	-	-	-	-	-	-	1	31250	-	-
8.38	fosc	54	9523	26	19398	-	-	-	-	-	-
	fosc/4	-	-	-	-	-	-	-	-	-	-
	fosc/16	-	-	-	-	-	-	-	-	-	-
	fosc/32	-	-	-	-	-	-	-	-	-	-
	fosc/64	-	-	-	-	-	-	-	-	-	-
	fs/2	-	-	-	-	-	-	-	-	-	-
	fs/4	-	-	-	-	-	-	-	-	-	-
12.00	fosc	77	9615	38	19231	25	28846	23	31250	-	-
	fosc/4	-	-	-	-	-	-	5	31250	-	-
	fosc/16	-	-	-	-	-	-	-	-	-	-
	fosc/32	-	-	-	-	-	-	-	-	-	-
	fosc/64	-	-	-	-	-	-	-	-	-	-
	fs/2	-	-	-	-	-	-	5	31250	-	-
	fs/4	-	-	-	-	-	-	2	31250	-	-
16.00	fosc	103	9615	51	19231	-	-	31	31250	25	38462
	fosc/4	25	9615	12	19231	-	-	7	31250	-	-
	fosc/16	-	-	-	-	-	-	-	-	-	-
	fosc/32	-	-	-	-	-	-	-	-	-	-
	fosc/64	-	-	-	-	-	-	-	-	-	-
	fs/2	25	9615	-	-	-	-	7	31250	-	-
	fs/4	12	9615	-	-	-	-	3	31250	-	-

Figure:15.3.25 Setup Value of UART Serial Interface Transfer Speed

■ Pin Setup (with 1,2 channels, at transmission)

Table:15.3.20 shows the pins setup at UART serial interface transmission. The pins setup is common to the TXD4 pin, RXD4 pin, regardless of those pins are independent / connected.

Table:15.3.20 UART Serial Interface Pin Setup (with 1,2 channels, at transmission)

Setup item	Data output pin	Data input pin
	TXD4 pin	RXD4 pin
Port pin	P40	P41
Serial data input selection	RXD4	
	SC4MD1(SC4IOM)	
Function	Serial data output	"1" output
	SC4MD1(SC4SBOS)	SC4MD1(SC4SBIS)
Style	Push-pull/ Nch open-drain	-
	P4ODC(P4ODC0)	
I/O	Output mode	-
	P4DIR(P4DIR0)	
Pull-up setup	Added / not added	-
	P4PLU(P4PLU0)	

■ Pin Setup (with 2 channels, at reception)

Table:15.3.21 shows the pins setup at UART serial interface reception with 2 channels (TXD4 pin, RXD4pin).

Table:15.3.21 UART Serial Interface Pin Setup (with 2 channels, at reception)

Setup item	Data output pin	Data input pin
	TXD4 pin	RXD4 pin
Port pin	P40	P41
Serial data input selection	RXD4	
	SC4MD1(SC4IOM)	
Function	Port	Serial data input
	SC4MD1(SC4SBOS)	SC4MD1(SC4SBIS)
Style	-	-
I/O	-	Input mode
	-	P4DIR(P4DIR1)
Pull-up setup	-	-

■ Pin Setup (with 1 channel, at reception)

Table:15.3.22 shows the pin setup at UART serial interface reception with 1 channel (TXD4 pin). The RXD4 pin in not used, so can be used as a port.

Table:15.3.22 UART Serial Interface Pin Setup (with 1 channel, at reception)

Setup item	Data output pin	Data input pin
	TXD4 pin	RXD4 pin
Port pin	P40	P41
Serial data input selection	TXD4	
	SC4MD1(SC4IOM)	
Function	Port	Serial data input
	SC4MD1(SC4SBOS)	SC4MD1(SC4SBIS)
Style	-	-
I/O	-	Input mode
	-	P4DIR(P4DIR1)
Pull-up setup	-	-

■ Pin Setup (with 2 channels, at transmission / reception)

Table:15.3.23 shows the pin setup at UART serial interface transmission / reception with 2 channels (TXD4 pin, RXD4 pin).

Table:15.3.23 UART Serial Interface Pin Setup (with 2 channels, at transmission / reception)

Setup item	Data output pin	Data input pin
	TXD4 pin	RXD4 pin
Port pin	P40	P41
Serial data input selection	RXD4	
	SC4MD1(SC4IOM)	
Function	Serial data output	Serial data input
	SC4MD1(SC4SBOS)	SC4MD1(SC4SBIS)
Style	Push-pull/ Nch open-drain	-
	P4ODC(P4ODC0)	
I/O	Output mode	Input mode
	P4DIR(P4DIR0)	P4DIR(P4DIR1)
Pull-up setup	Added / not added	-
	P4PLU(P4PLU0)	

15.3.4 Setup Example

■ Transmission / Reception Setup

The setup example at UART transmission / reception with serial 4 is shown. Table:15.3.24 shows the condition at transmission / reception.

Table:15.3.24 UART Interface Transmission Reception Setup

Setup item	SEt to
TXD4/RXD4 pin	Independent (with 2 channels)
Frame mode specification	8 bits + 2 stop bits
First transfer bit	MSB
Clock source	Timer 2
TXD4/RXD4 pin type	Nch open-drain
Pull-up resistor of TXD4 pin	Added
Parity bit add/check	"0" added/check
Serial 4 transmission complete interrupt	Enable
Serial 4 reception complete interrupt	Enable

An example setup procedure, with a description of each step is shown below.

Setup Procedure	Description
(1) Set the baud rate timer	(1) Set the baud rate timer by the TM2MD register, the TM2OC register. Set the TM2EN flag to "1" to start timer 2. [Chapter 5. 5.9 Serial Transfer Clock Output Operation]
(2) Select the clock source SC4MD3(0x03FAE) bp2-0 :SC4PSC2-0 =110	(2) Set the bp2 to 0 flag of the SC4MD3 register to "110" to select Timer 2 output as a clock source.
(3) Control the pin type P4ODC(0x03F3C) bp0 :P4ODC0 =1 P4PLU(0x03F44) bp0 :P4PLU0 =1	(3) Set the P4ODC0 flag of the P4ODC register to "1" to select Nch open-drain for the TXD4 pin. P4PLU0 flag of the P4PLU register to "1" to add pull-up register.
(4) Control the pin direction P4DIR(0x03F34) bp1,0 :P4DIR1,0 =0,1	(4) Set the P4DIR0 flag of the Port 4 pin direction control register (P4DIR) to "1" and the P4DIR3 flag to "0" to set P40 to the output mode, P41 to the input mode.

Setup Procedure	Description
(5) Set the SC4MD0 register Select the start condition SC4MD0(0x03FAB) bp3 :SC4STE =1	(5) Set the SC4STE flag of the SC4MD0 register to "1" to enable start condition.
Select the first bit to be transferred SC4MD0(0x03FAB) bp4 :SC4DIR =0	Set the SC4DIR flag of the SC4MD0 register to "0" to select MSB as first transfer bit.
(6) Set the SC4MD2 register Control the output data SC4MD2(0x03FAD) bp0 :SC4BRKE =0	(6) Set the SC4BRKE flag of the SC4MD2 register to "0" to select the serial data transmission.
Select the added parity bit SC4MD2(0x03FAD) bp3 :SC4NPE =0 bp5-4 :SC4PM1-0 =00	Set the SC4PM1 to 0 flag of the SC4MD2 register to "00" to select 0 parity, and set the SC4NPE flag to "0" to enable add parity bit.
Specify the flame mode SC4MD2(0x03FAD) bp7-6 :SC4FM1-0 =11	Set the SC4FM1 to 0 flag of the SC4MD2 register to "11" to select 8 bits + 2 stop bits at the flame mode.
(7) Set the SC4MD1 register Select the communication type SC4MD1(0x03FAC) bp0 :SC4CMD =1	(7) Set the SC4CMD flag of the SC4MD1 register to "1" to select full duplex UART.
Select the clock frequency SC4MD1(0x03FAC) bp3 :SC4CKM =1 bp2 :SC4MST =1	Set the SC4CKM flag of the SC4MD1 register to "1" to select "divided by 8" at source clock. And, the SC4MST flag should be always set to "1" to select clock master.
Control the pin function SC4MD1(0x03FAC) bp4 :SC4SBOS =1 bp5 :SC4SBIS =1 bp7 :SC4IOM =0	Set the SC4SBOS, SC4SBIS, SC4IOM flag of the SC4MD1 register to "1" to set the TXD4 pin to serial data output and the RXD4 pin to serial data input.
(8) Enable the interrupt SC4RICR(0x03FF8) bp1 :SC4RIE =1 SC4TICR(0x03FF9) bp1 :SC4TIE =1	(8) Set the SC4RIE flag of the SC4RICR register to "1", and SC4TIE flag of the SC4TICR register to "1" to enable the interrupt request. If any the interrupt request already set, clear them.
(9) Start the serial transmission The transmission ý TXBUF4(0x03FB1) The reception data ý input to RXD4	(9) The transmission is started by setting the transmission data to the serial transmission data buffer (TXBUF4). When the transmission is finished, the serial 4 transmission interrupt (SC4TIRQ) is generated. Also, after the received data is stored to the RXBUF4, the serial 4 reception interrupt (SC4RIRQ) is generated.

Note:(5), (6), (7) can be set at the same time.

When the TXD4 / RXD4 pin are connected for communication with 1 channel, the TXD4 pin inputs / outputs serial data. The port direction control register P4DIR switches I/O. At reception, set SC4SBIOS of the SC4MD1 register to "1" to select serial data input. The RXD4 pin can be used as a general port.

This serial interface contains emergency reset function. If communication need to be stopped by force, set SC4SBOS and SC4SBIS of the SC4MD1 register to "0".

Each flag should be set as the setup procedure in order. Activation of communication should be operated after all control registers (refer to Table:15.2.1 TXBUF4, RXBUF4) are set.

Timer 2 and timer 5 can be used as a baud rate timer. Refer to Chapter 5. 5.9 Serial Transfer Clock Output Operation.

Chapter 16 A/D Converter

16

16.1 Overview

This LSI has an A/D converter with 10 bits resolutions. It contains a built-in sample hold circuit. The channels 0 to 7 (AN0 to AN7) of analog input can be switched by software. When A/D converter is stopped, the power consumption can be reduced by turning the built-in ladder resistance OFF. A/D conversion is activated by a register setup and an external interrupt.

16.1.1 Functions

Table:16.1.1 shows the A/D converter functions.

Table:16.1.1 A/D Converter Functions

A/D Input Pins	8 pins
Pins	AN7 to AN0
Interrupt	ADIRQ
Resolution	10 bits
Conversion Time (Min.)	8.10 µs(T_{AD}= as 500 ns)
Input range	V_{SS} to V_{REF+}
Power Consumption	Built-in Ladder Resistance (ON/OFF)

Sampling time of analog signal after enabled A/D conversion start flag is not mentioned in conversion time above. Actual conversion time is value that is added 1 T_{AD} to conversion time.

16.1.2 Block Diagram

■ A/D Converter Block Diagram

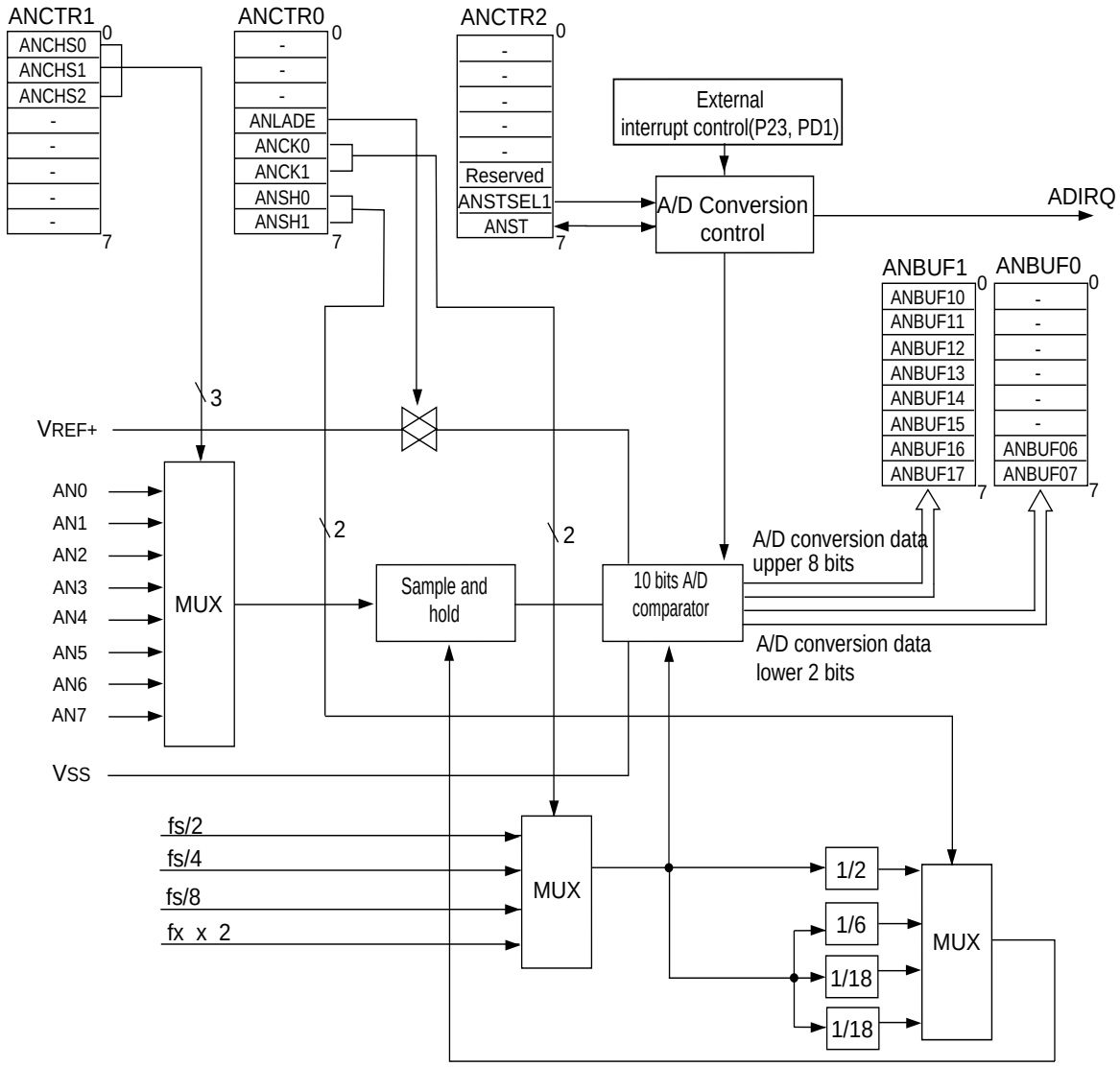


Figure:16.1.1 A/D Converter Block Diagram

16.2 Control Registers

A/D converter consists of the register (ANCTRn) and the data storage buffer (ANBUFn).

16.2.1 Registers

Table:16.2.1 shows the registers used to control A/D converter.

Table:16.2.1 A/D Converter Control Registers

Register	Address	R/W	Function	Page
ANCTR0	0x03FB2	R/W	A/D converter control register 0	XVI-5
ANCTR1	0x03FB3	R/W	A/D converter control register 1	XVI-6
ANCTR2	0x03FB4	R/W	A/D converter control register 2	XVI-6
ANBUF0	0x03FB5	R	A/D converter data storage buffer 0	XVI-7
ANBUF1	0x03FB6	R	A/D converter data storage buffer 1	XVI-7
ADICR	0x03FFA	R/W	A/D converter interrupt control register	III-44
PAIMD	0x03F3B	R/W	Port A input mode register	IV-99
PAPLU	0x03F4A	R/W	Port A Pull-up resistance control register	IV-99

R/W : Readable/Writable

R : Readable only

16.2.2 Control Registers

■ A/D Converter Control Register0 (ANCTR0:0x03FB2)

bp	7	6	5	4	3	2	1	0
Flag	ANSH1	ANSH0	ANCK1	ANCK0	ANLADE	-	-	-
Reset	0	0	0	0	0	-	-	-
Access	R/W	R/W	R/W	R/W	R/W	-	-	-

bp	Flag	Description
7-6	ANSH1 ANSH0	Sample and hold time 00:T_{AD} x 2 01:T_{AD} x 6 10:T_{AD} x 18 11:T_{AD} x 18
5-4	ANCK1 ANCK0	A/D conversion clock (ftad=1/T_{AD}) 00:fs/2 01:fs/4 10:fs/8 11:fx x 2 * as T_{AD}>500 ns
3	ANLADE	A/D ladder resistance control 0:A/D ladder resistance OFF 1:A/D ladder resistance ON
2-0	-	-

■ A/D Converter Control Register1 (ANCTR1:0x03FB3)

bp	7	6	5	4	3	2	1	0
Flag	-	-	-	-	-	ANSHS2	ANSHS1	ANSHS0
Reset	-	-	-	-	-	0	0	0
Access	-	-	-	-	-	R/W	R/W	R/W

bp	Flag	Description
7-3	-	-
2-0	ANSHS2 ANSHS1 ANSHS0	Analog input channel 000:AN0 (PA0) 001:AN1 (PA1) 010:AN2 (PA2) 011:AN3 (PA3) 100:AN4 (PA4) 101:AN5 (PA5) 110:AN6 (PA6) 111:AN7 (PA7)

■ A/D Converter Control Register2 (ANCTR2:0x03FB4)

bp	7	6	5	4	3	2	1	0
Flag	ANST	ANSTSEL1	Reserved	-	-	-	-	-
Reset	0	0	0	-	-	-	-	-
Access	R/W	R/W	R/W	-	-	-	-	-

bp	Flag	Description
7	ANST	A/D conversion status 0:Finish, Hold 1:Start, Converting
6	ANSTSEL1	A/D conversion starting factor select 0:Set ANST flag to "1" 1:Set external factor (P23, PD1 falling edge), ANST flag to "1"
5	Reserved	Set always to "0"
4-0	-	-

16.2.3 Data Buffers

■ A/D Conversion Data Storage Buffer0 (ANBUF0:0x03FB5)

The lower 2 bits results from A/D conversion are stored to this register.

bp	7	6	5	4	3	2	1	0
Flag	ANBUF07	ANBUF06	-	-	-	-	-	-
Reset	X	X	-	-	-	-	-	-
Access	R	R	-	-	-	-	-	-

■ A/D Conversion Data Storage Buffer1 (ANBUF1:0x03FB6)

The upper 8 bits results from A/D conversion are stored to this register.

bp	7	6	5	4	3	2	1	0
Flag	ANBUF17	ANBUF16	ANBUF15	ANBUF14	ANBUF13	ANBUF12	ANBUF11	ANBUF10
Reset	X	X	X	X	X	X	X	X
Access	R	R	R	R	R	R	R	R

16.3 Operation

Here is a description of A/D converter circuit setup procedure.

1. Set the analog pins.

   Set the analog input pin, set in (2), to "special function pin" by the port A input mode register (PAIMD).

   * Setup of the port A input mode register should be done before analog voltage is put to pins.

2. Select the analog input pin.

   Select the analog input pin from AN7 to AN0 by the ANCHS2-0 flag of the A/D converter control register1 (ANCTR1).

3. Select the A/D converter clock.

   Select the A/D converter clock by the ANCK1, ANCK0 flag of the A/D converter control register 0 (ANCTR0). Setup should be such a way that converter clock (T_{AD}) does not drop less than 500 ns with any resonator.

4. Set the sample hold time.

   Set the sample hold time by the ANSH1, ANSH0 flag of the A/D converter control register 0 (ANCTR0). The sample hold time should be based on analog input impedance.

   * (2) to (4) are not in order. (3) and (4) can be operated simultaneously.

5. Set the A/D ladder resistance.

   Set the ANLADE flag of the A/D converter control register 0 (ANCTR0) to "1", and a current flow through the ladder resistance and A/D converter goes into the waiting.

6. Select the A/D converter activation factor, then start A/D conversion.

   Set the ANST flag of the A/D converter control register 2 (ANCTR2) to "1" to start A/D converter or set ANSTSEL1 flag of A/D converter control register 2 (ANCTR2) to "1" to start A/D converter by the external trigger factor.

   * Specify the valid edge by the EDGSEL0 flag of the both edges interrupt control register (EDGDT) and the REDG0 flag of the external factor (P23, PD1 "L level") control register (0).

7. A/D conversion

   After sampling with the sample and hold time, set in (4), A/D conversion is decided in comparison with MBS, in order.

8. Complete the A/D conversion.

   When A/D conversion is finished, the ANST flag is cleared to "0", and the result of the conversion is stored to the A/D buffer (ANBUF0,1). Then, the A/D complete interrupt request (ADIRQ) is generated.

2 conversion clocks are needed to start A/D conversion after you set ANLADE flag to "1".

In the middle of A/D conversion, when you restart after crushing A/D conversion by setting ANST flag to "0", more than (2 system clock) + (2 converter clock) time is needed to start A/D conversion.

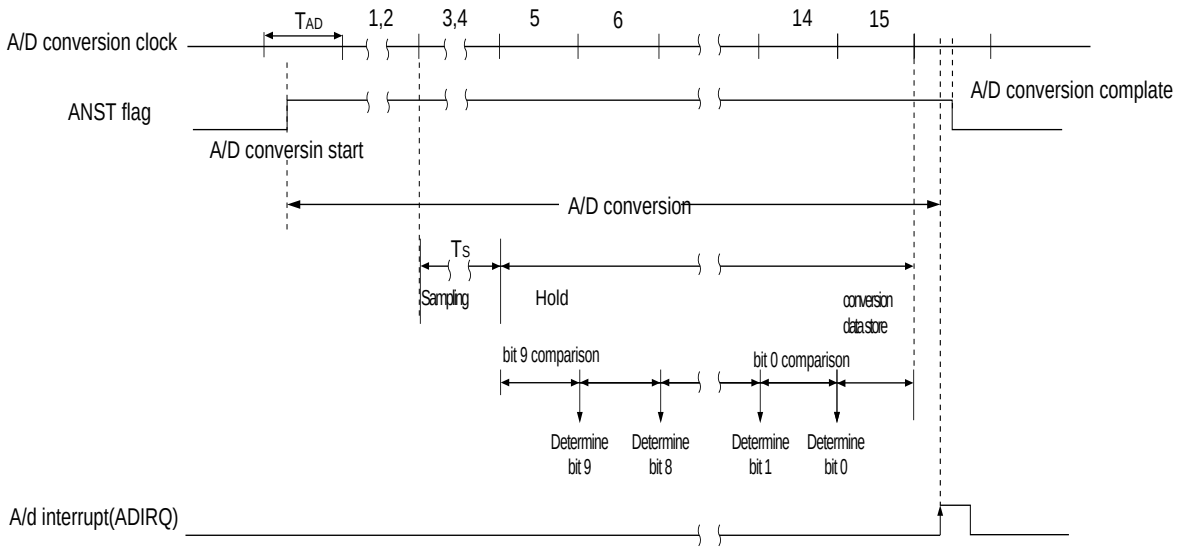


Figure:16.3.1 Operation of A/D Conversion

To read out the value of the A/D conversion, A/D conversion should be done several times to prevent noise error by confirming the match of level by program, or by using the average value.

16.3.1 Setup

■ Input Pins of A/D Converter Setup

Input pins for A/D converter is selected by the ANCH2-0 flag of the ANCTR1 register.

Table:16.3.1 A/D Conversion Input Pins Setup

ANCHS2	ANCHS1	ANCHS0	A/D pins
0	0	0	AN pins0
		1	AN pins1
	1	0	AN pins2
		1	AN pins3
1	0	0	AN pins4
		1	AN pins5
	1	0	AN pins6
		1	AN pins7

■ A/D Converter Clock Setup

The A/D converter clock is set with the ANCK1 to ANCK0 flag of the ANCTR0 register. Set the A/D converter clock (T_{AD}) more than 500 ns and less than 15.26 ms. Table:16.3.2 shows the machine clock (fosc, fx, fs) and the A/D converter clock (T_{AD}). (calculated as fs = fosc/2, fx/4)

Table:16.3.2 A/D Conversion Clock and A/D Conversion Cycle

ANCK1	ANCK0	A/D conversion clock	A/D conversion cycle (T_{AD})		
			at high speed oscillation		at low speed oscillation
			fosc=32 MHz	fosc=8.38 MHz	fosc=32.768 kHz
0	0	fs/2	125.00 ns(unusable)	477.33 ns(unusable)	244.14 µs
	1	fs/4	250.00 ns(unusable)	954.65 ns	488.28 µs
1	0	fs/8	500.00 ns	1.91 µs	976.56 µs
	1	fx x 2	15.26 µs	15.26 µs	15.26 µs

For the system clock (fs), refer to Chapter 2 2.6 Clock Switching.

■ A/D Converter Sampling Time (Ts) Setup

The sampling time of A/D converter is set with the ANSH1 to 0 flag of the ANCTR0 register. The sampling time of A/D converter depends on external circuit, so set the right value by analog input impedance.

Table:16.3.3 Sampling Time of A/D Conversion and A/D Conversion Time

ANSH1	ANSH0	Sampling time (Ts)	A/D conversion time[µs]				
			at high speed (fs=10 MHz)				at low speed (fx =8.19 kHz)
			at T_{AD} =800 ns	at T_{AD} =954.65 ns	at T_{AD} =1.91 µs	at T_{AD} =15.26 µs	at T_{AD} =15.26 µs
0	0	T_{AD} x 2	12.95	15.42	30.71	244.31	427.31
	1	T_{AD} x 6	16.15	19.24	38.35	305.35	488.35
1	0	T_{AD} x 18	25.75	30.70	61.27	488.47	671.47
	1	T_{AD} x 18	25.75	30.70	61.27	488.47	671.47

* Calculated as fosc=20 MHz, fx=32.768 kHz, fs=fosc/2, fx/4.

Sampling time of analog signal after enabled A/D conversion start flag is not mentioned in conversion time above. Actual conversion time is value that is added 1 T_{AD} to conversion time.
[Calculus]
Conversion Time = T_S + 14T_{AD} + 1.5/fs

■ Built-in Ladder Resistance Control

The ANLADE flag to the ANCTR0 register is set to "1" to send a current to the ladder resistance for A/D conversion. When A/D converter is stopped, the ANLADE flag of the ANCTR0 register is set to "0" to save the power consumption.

Table:16.3.4 A/D Ladder Resistance Control

ANLADE	A/D ladder resistance control
0	A/D ladder resistance control disabled (A/D conversion stop)
1	A/D ladder resistance control enabled (A/D conversion halt)

■ A/D Conversion Starting Factor Setup

A/D conversion starting factor is set with the ANSTSEL1 flag of the ANCTR2 register. The ANSTSEL1 flag of the ANCTR2 register is set to start A/D conversion by the external (P23, PD1, PD1 falling edge) factor. Also, the ANST flag of the ANCTR2 register is set to "1" is possible.

Table:16.3.5 A/D Conversion Starting Factor Setup

ANSTSEL	A/D Conversion Starting Factor
0	Set ANST flag to “1“
1	Set ANST flag and external factor (P23 falling edge) to “1“

■ A/D Conversion Starting Setup

A/D conversion starting is set with the ANST flag of the ANCTR2 register. The ANST flag of the ANCTR2 register is set to "1" to start A/D conversion. ANST flag of the ANCTR2 register is set to "1" after the external factor (P23 falling edge) to start A/D conversion by the external (P23, PD1 falling edge) factor. Also, the ANST flag of ANCTR2 register is set to "1" during A/D conversion, then cleared to "0".

Table:16.3.6 A/D Conversion Starting Setup

ANST	A/D Conversion Starting Factor
0	A/D conversion start and A/D conversion is during conversion
1	After the conversion ends, A/D conversion stop

16.3.2 Setup Example

■ Example of A/D Converter Setup by Registers

A/D conversion is started by setting registers. The analog input pins are set to AN0, the converter clock is set to fs/4, and the sampling hold time is set to T_{AD} x 6. Then, A/D conversion complete interrupt is generated. An example setup procedure, with a description of each step is shown below.

Setup Procedure	Description
(1) Set the analog input pin. PAIMD(0x03F3B) p0 :PAIMD0 =1 PAPLU(0x03F4A) bp0 :PAPLU0 =0	(1) Set the analog input pin, set in a(2), as the special function pin with the port A input mode register (PAIMD). Also, set no pull-up/pull-down resistance with the port A pull-up/pull-down resistance control register (PAPLUD).
(2) Select the analog input pin. ANCTR1(0x03FB3) bp2-0 :ANCHS2-0 =000	(2) Select the analog input pin from AN7 to AN0 by the ANCH2-0 flag of the A/D converter control register1 (ANCTR1).
(3) Select the A/D converter clock. ANCTR0(0x03FB2) bp5-4 :ANCK1-0 =01	(3) Select the A/D converter clock by the ANCK1, ANCK0 flag of the A/D converter control register0 (ANCTR0).
(4) Set the sample and hold time. ANCTR0(0x03FB2) bp7-6 :ANSH1-0 =01	(4) Set the sample and hold time by the ANSH1, ANSH0 flag of the A/D converter control register0 (ANCTR0).
(5) Set the interrupt level. ADICR(0x03FFA) bp7-6 :ADLV1-0 =00	(5) Set the interrupt level by the ADLV1-0 flag of the A/D conversion complete interrupt control register (ADICR). If any interrupt request flag is already set, clear it.
(6) Enable the interrupt. ADICR(0x03FFA) bp1 :ADIE =1	(6) Enable the interrupt by setting the ADIE flag the ADICR register to "1". [Chapter 3 3.1.4 Interrupt Flag Setup]
(7) Set the A/D ladder resistance. ANCTR0(0x03FB2) bp3 :ANLADE =1	(7) Set the ANLADE flag of the A/D converter control register0 (ANCTR0) to "1" to send a current to the ladder resistance for the A/D conversion.
(8) Start A/D conversion. ANCTR2(0x03FB4) bp6 :ANSTSEL1 =0	(8) Clear the ANSTSEL1 flag of the A/D converter control register2 (ANCTR2) to "0" to set A/D conversion starting factor to ANST flag of the A/D converter control register2 (ANCTR2).
(9) Start A/D conversion operation. ANCTR2(0x03FB4) bp7 :ANST =1	(9) Set the ANST flag of the A/D converter control register2 (ANCTR2) to "1" to start the A/D conversion.

Setup Procedure	Description
(10) Complete A/D conversion operation. ANBUF0(0x03FB5) ANBUF1(0x03FB6)	(10) After A/D conversion operation,the result of conversion is stored at A/D buffer (ANBUF 0,1), the ANST flag of A/D control register 2 (ANCTR2) is reset, and then A/D conversion complete interrupt is generated.

* The above (3) to (4) can be set at the same time.

After the A/D conversion, when you restart, set the ANLADE of the A/D converter control register0 (ANCTR0) to "0" and confirm the analog stop before changing the setup. Operations of other than this order are not guaranteed.

■ Example of A/D Converter Setup by the external factor (P23 falling edge)

A/D conversion is started by the external factor (P23 falling edge). The analog input pins are set to AN0, the converter clock is set to fs/4, and the sampling hold time is set to T_{AD} x 6. Then, A/D conversion complete interrupt is generated.

An example setup procedure, with a description of each step is shown below.

Setup Procedure	Description
(1) Set the analog input pin. PAIMD(0x03F3B) p0 :PAIMD0 =1 PAPLU(0x03F4A) bp0 :PAPLU0 =0	(1) Set the analog input pin, set in a(2), as the special function pin with the port A input mode register (PAIMD). Also, set no pull-up resistance with the port A pull-up resistance control register (PAPLUD).
(2) Select the analog input pin. ANCTR1(0x03FB3) bp2-0 :ANCHS2-0 =000	(2) Select the analog input pin from AN7 to AN0 by the ANCH2-0 flag of the A/D converter control register1 (ANCTR1).
(3) Select the A/D converter clock. ANCTR0(0x03FB2) bp5-4 :ANCK1-0 =01	(3) Select the A/D converter clock by the ANCK1, ANCK0 flag of the A/D converter control register0 (ANCTR0).
(4) Set the sample and hold time. ANCTR0(0x03FB2) bp7-6 :ANSH1-0 =01	(4) Set the sample and hold time by the ANSH1, ANSH0 flag of the A/D converter control register0 (ANCTR0).
(5) Set the interrupt level. ADICR(0x03FFA) bp7-6 :ADLV1-0 =10	(5) Set the interrupt level by the ADLV1-0 flag of the A/D conversion complete interrupt control register (ADICR). If any interrupt request flag is already set, clear it. [Chapter 3 3.1.4 Interrupt Flag Setup]
(6) Enable the interrupt. ADICR(0x3FFA) bp1 :ADIE =1	(6) Enable the interrupt by setting the ADIE flag the ADICR register to "1".
(7) Set the A/D ladder resistance. ANCTR0(0x03FB2) bp3 :ANLADE =1	(7) Set the ANLADE flag of the A/D converter control register0 (ANCTR0) to "1" to send a current to the ladder resistance for the A/D conversion.
(8) Select the A/D Conversion Starting factor. ANCTR2(0x03FB4) bp7 :ANSTSEL1 =1	(8) Set the ANSTSEL flag of the A/D converter control register2 (ANCTR2) to "1" , then setup the A/D conversion starting factor to the external factor (P23) and the ANST flag of the A/D converter control register2 (ANCTR2).
(9) Start the A/D conversion Operation. ANCTR2(0x03FB4) bp7 :ANST =1	(9) When the external factor (P23 falling edge) is generated, the ANST flag of the A/D converter control register2 (ANCTR2) is set to "1", then the A/D conversion is started. Also, even if the external factor (P23) is not generated, the A/D conversion can be started by setting the ANST flag of the A/D converter control register2 (ANCTR2)

Setup Procedure	Description
(10) Complete A/D conversion ANBUF0(0x03FB5) ANBUF1(0x03FB6)	(10) After A/D conversion operation,the result of conversion is stored at A/D buffer (ANBUF 0,1), the ANST flag of A/D control register 2 (ANCTR2) is reset, and then A/D conversion complete interrupt is generated.

* The above (3) to (4) can be set at the same time.

Even if the external interrupt is generated in the middle of the A/D conversion, operation is done as usual. Also, after finished, the A/D conversion is never be started again.

After the A/D conversion, when you restart, set the ANLADE of the A/D converter control register0 (ANCTR0) to "0" and confirm the analog stop before changing the setup. Operations of other than this order are not guaranteed.

16.3.3 Cautions

A/D conversion can be damaged by noise easily, therefore, anti-noise measures should be taken adequately.

■ Anti-noise measures

To A/D input (analog input pin), add condenser near the Vss pins of micro controller.

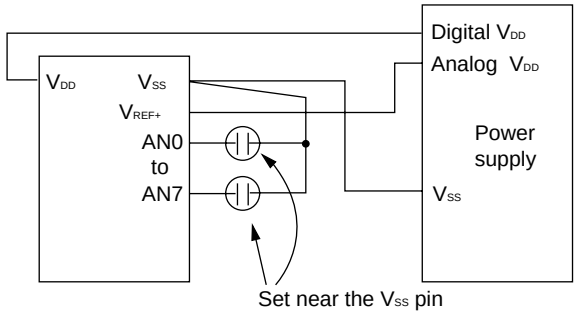


Figure:16.3.2 A/D Converter Recommended Example 1

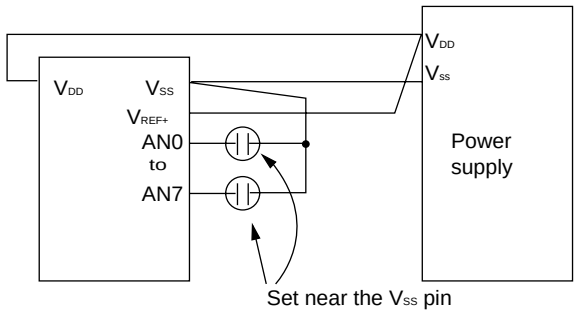


Figure:16.3.3 A/D Converter Recommended Example 2

For high precision of A/D conversion, the following cautions on A/D converter should be kept.
1.The input impedance R of A/D input pin should be under 500 kΩ, and the external capacitor C (more than 1000 pF, under 1 μF) should be connected to it.
2.The A/D conversion frequency should be set in regard to R, C.
3.At the A/D conversion, if the input level of microcontroller is changed, or the peripheral added circuit is switched to ON/OFF, the A/D conversion could work wrongly, as the analog input pins and power pins cannot be fixed. At the setup checking, confirm the wave form of analog input pins.

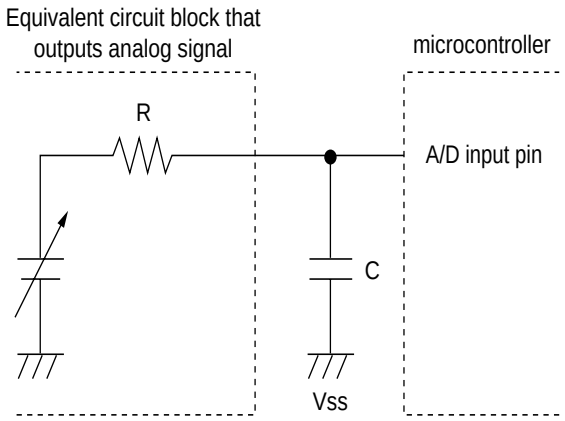


Figure:16.3.4 Recommended Circuit

Chapter 17 D/A Converter

17

17.1 Overview

This LSI has a built-in D/A converter with 8 bits solution. There is 1 output channel and 8-bit data registers for the channel. This LSI supports D/A conversion mode. When the D/A converter is not used, the built-in ladder resistance can be set to OFF to save the power consumption.

17.1.1 Functions

Here is the list of D/A converter functions.

Table:17.1.1 D/A converter functions

Resolution	8-bit
Pin	DA0 pin
Power consumption saving	Built-in ladder resistance ON/OFF

17.1.2 D/A Converter Block Diagram

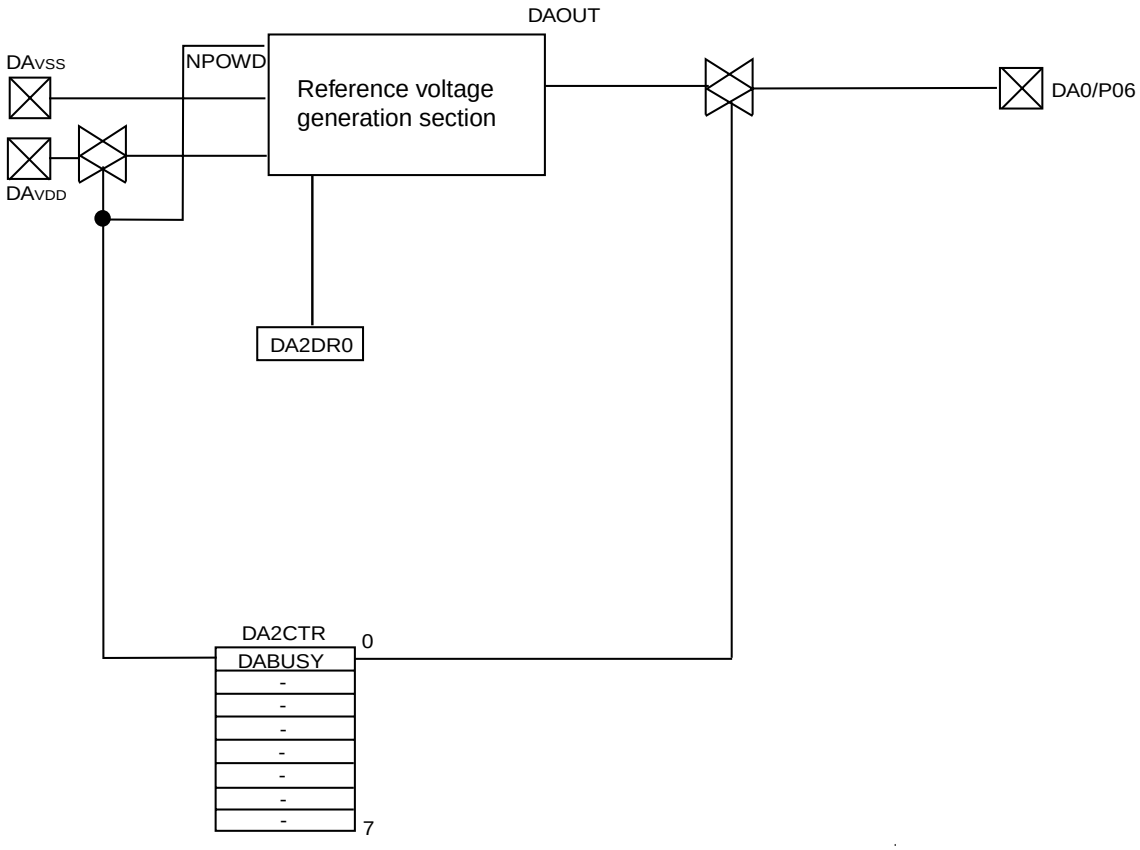


Figure:17.1.1 D/A Converter Block Diagram

17.2 D/A Converter Control Registers

17.2.1 D/A Converter Control Registers

Following table shows the registers to control the D/A converter of this LSI.

Table:17.2.1 D/A Converter Control Registers

Register	Address	R/W	Function	Page
DA2CTR	0x03FBE	R/W	D/A converter control register	XVII-5
DA2DR0	0x03FBF	R/W	D/A converter input data register 0	XVII-6
P0DIR	0x03F30	R/W	Port 0 direction control register	IV-8
P0PLU	0x03F40	R/W	Port 0 pull-up resistor control register	IV-9

R/W : Readable/Writable

17.2.2 D/A Converter Control Register (DA2CTR)

This is the 8-bit readable/writable register that controls the D/A conversion.

■ D/A Converter Control Register (DA2CTR)

bp	7	6	5	4	3	2	1	0
Flag	-	-	-	-	-	-	-	DABUSY
At reset	-	-	-	-	-	-	-	0
Access	-							R/W

bp	Flag	Description
7-1	-	-
0	DABUSY	D/A conversion enable flag 0: Stop D/A converter operation (ladder resistance OFF) 1: Enable D/A converter operation

17.2.3 D/A Converter Input Data Register

This readable/writable register stores the D/A converter data.

■ D/A Converter Input Data Register 01 (DA2DR0:0x03FBF)

This register stores the D/A converter data (for DA0 channel).

bp	7	6	5	4	3	2	1	0
Flag	DA20BUF7	DA20BUF6	DA20BUF5	DA20BUF4	DA20BUF3	DA20BUF2	DA20BUF1	DA20BUF0
At reset	X	X	X	X	X	X	X	X
Access	R/W							

17.3 Operation

Procedures of D/A converter operation is as follows;

1. Set the DABUSY flag of the D/A converter control register (DA2CTR) to “1” to send a ladder resistor current to start D/A conversion.
2. D/A conversion is executed to the data set to the DA2DR0 register and the result obtained from the conversion is output to the DA0 pin.

17.3.1 Fixed Channel D/A Converter Setup Example·

■ Fixed Channel D/A Converter Setup Example

Set the converter channel to DA0.

An example setup procedure, with a description of each step is shown below.

Setup Procedure	Description
(1) Set the port 0 pin. P0DIR(0x03F30) bp6 :P0DIR6 =0 P0PLU(0x03F40) bp6 :P0PLU6 =0	(1) Set the analog output pin to "input mode" by the port 0 output direction control register (P0DIR), and to "no pull-up resistor" with the port 0 pull-up resistor control register.
(2) Set the D/A conversion mode. DA2DR0(0x03FBF)	(2) Set the D/A converter data by the D/A converter input register 0 (DA2DR0).
(3) Start the D/A conversion. DA2CTR(0x03FBE) bp0 : DABUSY =1	(3) Set the DABUSY flag of the D/A converter control register (DA2CTR) to "1" to start the D/A conversion. the result obtained from the conversion is output to the DA0 pin.

Chapter 18 Automatic Transfer Controller

18

18.1 Automatic Transfer Controller

18.1.1 Overview

This LSI contains an automatic transfer controller (ATC) that uses direct memory access (DMA) to transfer the contents of the whole memory space (1 MB) using the hardware. This ATC block is called ATC1.

ATC1 is activated by an interrupt or a flag set by the software. Once this occurs, even if it is in the middle of executing an instruction, the microcontroller waits for a time when it can release the bus, stops normal operation, and transfers bus control to ATC1. ATC1 then uses the released bus for the hardware data transfer.

The software sets the activation factor in ATC1 control register 1 (AT1CNT1), then data transfer begins when the AT1ACT flag in ATC1 control register 0 (AT1CNT0) is set to "1". AT1ACT flag is automatically cleared to "0" when ATC1 is activated.

The transfer data counter (AT1TRC) determines the number of transfers that ATC1 makes, up to a maximum of 255 times. There are also 16 transfer modes, set in ATC1 control register 0 (AT1CNT0).

The interrupt enable flag (xxxIE) for interrupt as a trigger factor needs not to be set. This is because the automatic data transfer occurs in the hardware without going through an interrupt service routine. If the interrupt enable flag (xxxIE) is set for the type of interrupt ATC1, a regular interrupt is generated after the automatic transfer ends.

In processor mode and memory expansion mode, the automatic data transfer control function (ATC1) cannnot be used for access to external memory.

To use the automatic data transfer control function (ATC1) for access to internal memory in memory expansion mode and processor mode, set the NCS(P74), NRE(P75), NWE(P76) pins to 1 and pull-up.

18.1.2 Functions

Table:18.1.1 provides a list of the ATC1 trigger factors and transfer modes.

■ ATC1 Trigger Factors

Table:18.1.1 ATC1 Trigger Factors

Trigger Factors	External interrupt 0
	External interrupt 1
	External interrupt 2
	External interrupt 3
	Timer 0 interrupt
	Timer 1 interrupt
	Timer 7 interrupt
	Timer 7 capture trigger
	Serial interface 0 UART transmission interrupt
	Serial interface 0 UART reception interrupt
	Serial interface 1 UART transmission interrupt
	Serial interface 2 interrupt
	Serial interface 3 interrupt
	Serial interface 4 UART transmission interrupt
	A/D converter interrupt
	Software activation

■ Transfer Modes

Table:18.1.2 Transfer Modes

Transfer Mode	Transfer Direction (*)				Pointer Increment Control		Transfer Operation
	cycle	Source Address	→	Destination Address	AT1MAP0	AT1MAP1	
Transfer mode 0		AT1MAP0	→	AT1MAP1 (I/O area)	-	-	1-byte data transfer
Transfer mode 1		AT1MAP1 (I/O area)	→	AT1MAP0	-	-	1-byte data transfer
Transfer mode 2		AT1MAP0	→	AT1MAP1 (I/O area)	AT1MAP0+1	-	1-byte data transfer
Transfer mode 3		AT1MAP1 (I/O area)	→	AT1MAP0	AT1MAP0+1	-	1-byte data transfer
Transfer mode 4	1st 2nd	AT1MAP0 AT1MAP0 [=AT1MAP0+1]	→ →	AT1MAP1 ((I/O area : even ADR) AT1MAP1 (I/O area : odd ADR)	AT1MAP0+1 AT1MAP0+1	- -	1-word data transfer (An even address must be set in AT1MAP1)
Transfer mode 5	1st 2nd	AT1MAP1 (I/O area : even ADR) AT1MAP1 (I/O area : odd ADR)	→ →	AT1MAP0 AT1MAP0 [=AT1MAP0+1]	AT1MAP0+1 AT1MAP0+1	- -	1-word data transfer (An even address must be set in AT1MAP1)
Transfer mode 6	1st 2nd	AT1MAP1 (I/O area) AT1MAP0 [=AT1MAP0+1]	→ →	AT1MAP0 AT1MAP1 (I/O area)	AT1MAP0+1 AT1MAP0+1	- -	Two 1-byte data tranfers
Transfer mode 7	1st 2nd	AT1MAP1 (I/O area) AT1MAP0 [=AT1MAP0+1]	→ →	AT1MAP0 AT1MAP1 (I/O area)	AT1MAP0+1 -	- -	Two 1-byte data tranfers
Transfer mode 8	1st 2nd	AT1MAP1 (I/O area : even ADR) AT1MAP0 [=AT1MAP0+1]	→ →	AT1MAP0 AT1MAP1 (I/O area : odd ADR)	AT1MAP0+1 AT1MAP0+1	- -	Two 1-byte data tranfers (An even address must be set in AT1MAP1)
Transfer mode 9	1st 2nd	AT1MAP1 (I/O area : even ADR) AT1MAP0 [=AT1MAP0+1]	→ →	AT1MAP0 AT1MAP1 (I/O area : odd ADR)	AT1MAP0+1 -	- -	Two 1-byte data tranfers (An even address must be set in AT1MAP1)
Transfer mode A		AT1MAP0	→	AT1MAP1	-	-	1-byte data transfer (whole memory area)
Transfer mode B		AT1MAP1	→	AT1MAP0	-	-	1-byte data transfer (whole memory area)
Transfer mode C		AT1MAP0	→	AT1MAP1	AT1MAP0+1	AT1MAP1+1	1-byte data transfer (whole memory area)
Transfer mode D		AT1MAP1	→	AT1MAP0	AT1MAP0+1	AT1MAP1+1	1-byte data transfer (whole memory area)
Transfer mode E		AT1MAP0	→	AT1MAP1	AT1MAP0+1	AT1MAP1+1	Burst transfer (continues until AT1TCR=0)
Transfer mode F		AT1MAP1	→	AT1MAP0	AT1MAP0+1	AT1MAP1+1	Burst transfer (continues until AT1TCR=0)

(*) When a memory pointer points to the I/O space, only the lower 8 bits of the pointer are valid.

18.1.3 Block Diagram

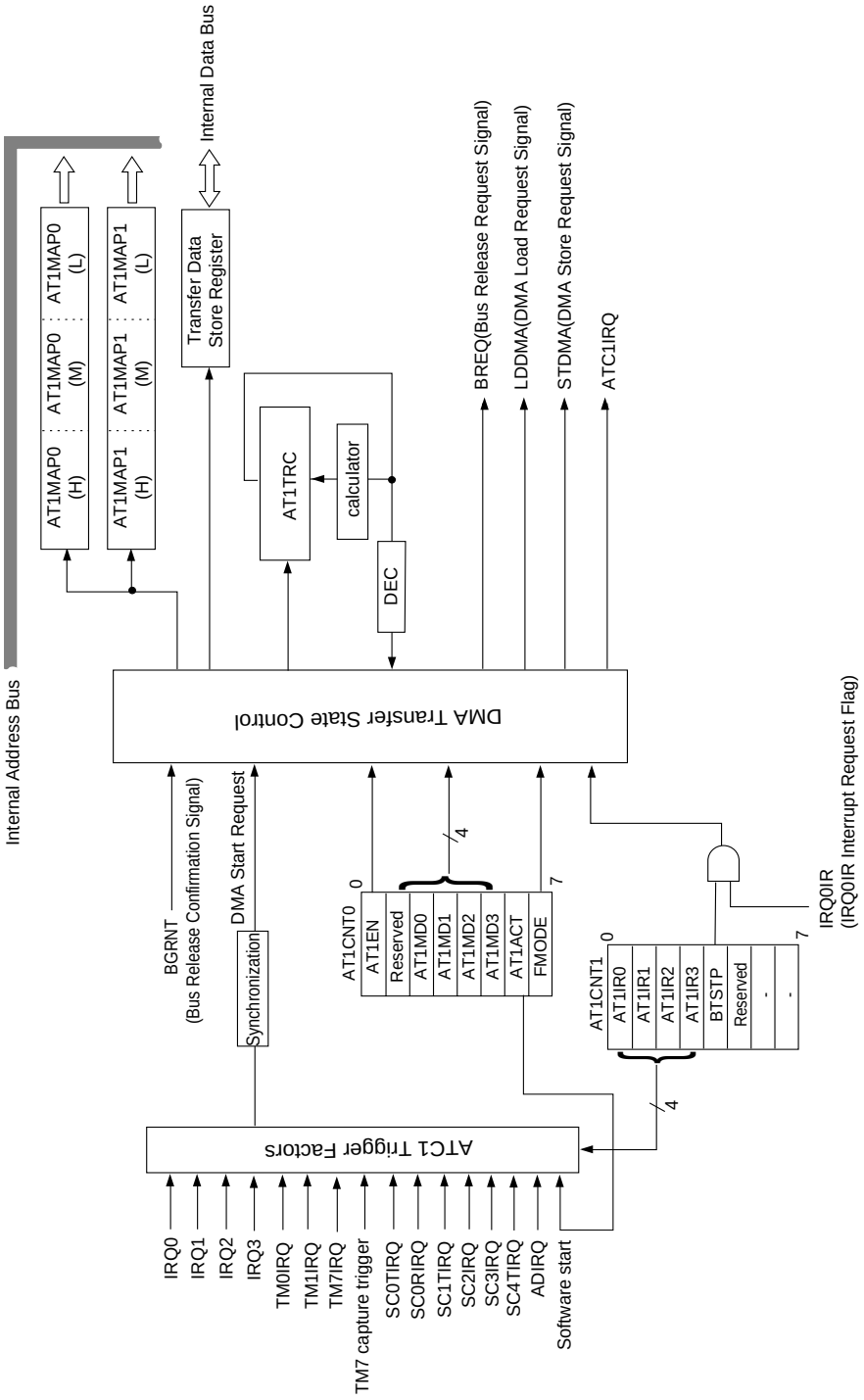


Figure:18.1.1 ATC1 Block Diagram

18.2 Control Registers

18.2.1 Registers

Table:18.2.1 shows the registers used to control ATC1.

Table:18.2.1 ATC1 Control Registers

	Register	Address	R/W	Function	Page
ATC1	AT1CNT0	0X03FD0	R/W	ATC1 control register 0	XVIII-7
	AT1CNT1	0X03FD1	R/W	ATC1 control register 1	XVIII-8
	AT1TRC	0X03FD2	R/W	ATC1 transfer data counter	XVIII-9
	AT1MAPOL	0X03FD3	R/W	ATC1 memory pointer 0 (lower 8 bits)	XVIII-10
	AT1MAPOM	0X03FD4	R/W	ATC1 memory pointer 0 (middle 8 bits)	XVIII-10
	AT1MAPOH	0X03FD5	R/W	ATC1 memory pointer 0 (upper 4 bits)	XVIII-10
	AT1MAP1L	0X03FD6	R/W	ATC1 memory pointer 1 (lower 8 bits)	XVIII-11
	AT1MAP1M	0X03FD7	R/W	ATC1 memory pointer 1 (middle 8 bits)	XVIII-11
	AT1MAP1H	0X03FD8	R/W	ATC1 memory pointer 1 (upper 4 bits)	XVIII-11

R/W : Readable / Writable

■ ATC1 Control Register 0 (AT1CNT0:0x03FD0)

bp	7	6	5	4	3	2	1	0
Flag	FMODE	AT1ACT	AT1MD3	AT1MD2	AT1MD1	AT1MD0	Reserved	AT1EN
At reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bp	Flag	Description
7	FM0DE	Increment control flag for memory pointer 0 0: Increment depending on transfer mode 1: Disable incrementing of memory pointer 0
6	AT1ACT	ATC1 software activation flag 0: Do not activate ATC1 1: Activate ATC1
5-2	AT1MD3 AT1MD2 AT1MD1 AT1MD0	ATC1 data transfer mode 0000 : Transfer mode 0 0001 : Transfer mode 1 0010 : Transfer mode 2 0011 : Transfer mode 3 0100 : Transfer mode 4 0101 : Transfer mode 5 0110 : Transfer mode 6 0111 : Transfer mode 7 1000 : Transfer mode 8 1001 : Transfer mode 9 1010 : Transfer mode A 1011 : Transfer mode B 1100 : Transfer mode C 1101 : Transfer mode D 1110 : Transfer mode E 1111 : Transfer mode F
1	Reserved	Set always to "0".
0	AT1EN	ATC1 transfer enable flag 0: ATC1 transfer disable 1: ATC1 transfer enable

■ ATC1 Control Register 1(AT1CNT1:0x03FD1)

bp	7	6	5	4	3	2	1	0
Flag	-	-	Reserved	BTSTP	AT1IR3	AT1IR2	AT1IR1	AT1IR0
At reset	-	-	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bp	Flag	Description
7-6	-	-
5	Reserved	Set always to "0".
4	BTSTP	Burst transfer stop enable 0: Burst transfer stop disable 1: Burst transfer stop enable (Transfer stops when external interrupt 0 occurs.)
3-0	AT1IR3 AT1IR2 AT1IR1 AT1IR0	ATC1 trigger factor settings 0000:External interrupt 0 0001:External interrupt 1 0010:Serial interface 0 UART transmission interrupt 0011:Serial interface 1 UART transmission interrupt 0100:Timer 7 interrupt 0101:Timer 7 capture trigger 0110:A/D converter interrupt 0111:Software activation 1000:External interrupt 2 1001:External interrupt 3 1010:Serial interface 2 interrupt 1011:Serial interface 3 interrupt 1100:Serial interface 4 UART transmission interrupt 1101:Serial interface 0 UART reception interrupt 1110:Timer 0 interrupt 1111:Timer 1 interrupt

When burst transfer stop is enabled, do not select external interrupt 0 for ATC1trigger factor.

■ ATC1 Transfer Counter (AT1TRC1:0x03FD2)

bp	7	6	5	4	3	2	1	0
Flag	AT1TRC7	AT1TRC6	AT1TRC5	AT1TRC4	AT1TRC3	AT1TRC2	AT1TRC1	AT1TRC0
At reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bp	Flag	Description
7-0	AT1TRC7-0	ATC1 Transfer Data Count Setting · For transfer modes 0 to D, set this register to the number of ATC activations. · For transfer modes E and F, set this register to number of burst transfers.

■ ATC1 Memory Pointer 0 : Lower 8 bits (AT1MAP0L:0x03FD3)

bp	7	6	5	4	3	2	1	0
Flag	bp7	bp6	bp5	bp4	bp3	bp2	bp1	bp0
At reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

■ ATC1 Memory Pointer 0 : Middle 8 bits (AT1MAP0M:0x03FD4)

bp	7	6	5	4	3	2	1	0
Flag	bp15	bp14	bp13	bp12	bp11	bp10	bp9	bp8
At reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

■ ATC1 Memory Pointer 0 : Upper 4 bits (AT1MAP0H:0x03FD5)

bp	7	6	5	4	3	2	1	0
Flag	-	-		-	bp19	bp18	bp17	bp16
At reset	-	-	-	-	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

■ ATC1 Memory Pointer 1 : Lower 8 bits (AT1MAP1L:0x03FD6)

bp	7	6	5	4	3	2	1	0
Flag	bp7	bp6	bp5	bp4	bp3	bp2	bp1	bp0
At reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

■ ATC1 Memory Pointer 1 : Middle 8 bits (AT1MAP1M:0x03FD7)

bp	7	6	5	4	3	2	1	0
Flag	bp15	bp14	bp13	bp12	bp11	bp10	bp9	bp8
At reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

■ ATC1 Memory Pointer 1 : Upper 4 bits (AT1MAP1H:0x03FD8)

bp	7	6	5	4	3	2	1	0
Flag	-	-		-	bp19	bp18	bp17	bp16
At reset	-	-	-	-	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

18.3 Operation

18.3.1 Basic Operations and Timing

ATC1 is a DMA block that enables the hardware to transfer the whole memory space (1 MB). This section provides a description of and timing for the basic ATC1 operations.

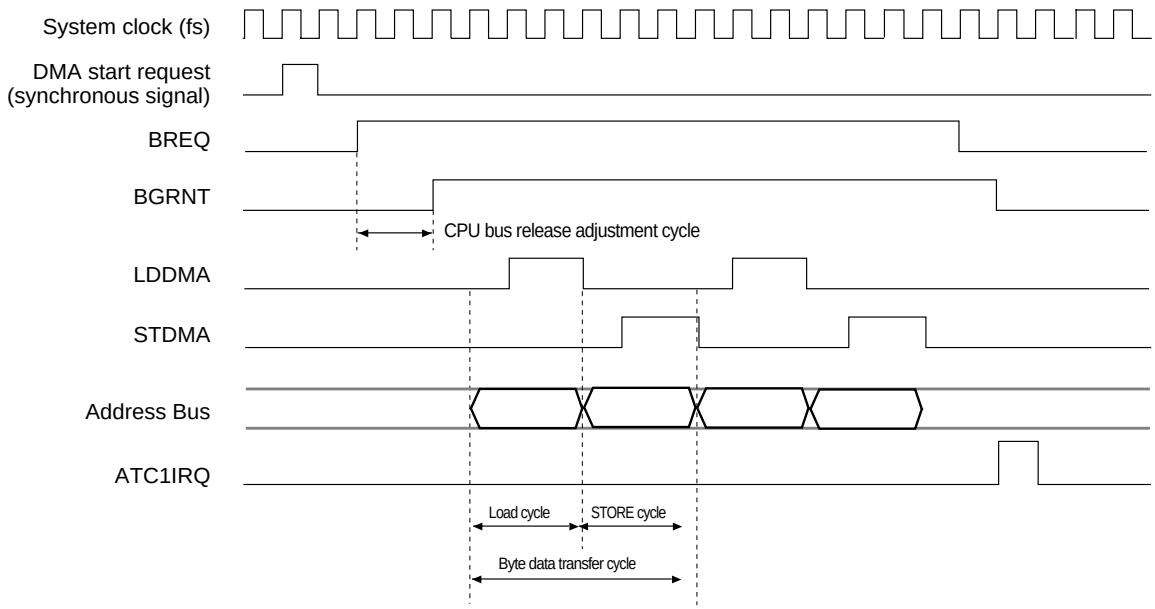


Figure:18.3.1 ATC1 Timing Chart

■ ATC1 activation and internal bus acquisition

ATC1 activates either when the selected interrupt factor occurs or when the software sets the activation flag. Set the ATC1 trigger factor in ATC1 control register 1 (AT1CNT1). When ATC1 starts, the ATC1 controller asserts the BREQ signal, which requests the MCU core to release the bus. When the core receives the BREQ signal, it stops all normal executions, even if it is in the middle of executing an instruction, and releases the bus at the next available timing. The core takes a maximum of five cycles from the time it receives the BREQ signal until it actually releases the bus. After it releases the internal bus, the core returns the bus granted signal, BGRNT, to ATC1. ATC1 can then begin using the bus to transfer data.

When an external interrupt is selected as an ATC1 trigger factor, specify the activation valid edge by the REDGn flag of the external interrupt control register and the EDGSELn flag of the both edges interrupt control register (EDGDT). [Chapter 3 3.3.1. External interrupts]

Set the valid edge for external interrupts before ATC1 activates.

■ Data transfer

The basic ATC1 operation cycle is the "byte-data transfer cycle", in which ATC1 transfers a single byte of data. This operation consists of two instruction cycles, a load and a store cycle. In the load cycle, ATC1 reads the data from the source address of the source memory, and in the store cycle, ATC1 stores the read data to the destination address of the destination memory. ATC1 transfers word-length data or a multi-byte stream of data by repeating the byte-data transfer cycle as many times as necessary.

■ Transfer end

Once it has transferred all the data, ATC1 generates an interrupt (ATC1IRQ) and stop the automatic transfer. In this way, the ATC1 block bypasses the software and automatically transfers data in a continuous DMA operation.

In both the load and store cycles, the read and write access occurs to the memory exactly as it does in a normal instruction execution. This means that the access timing is different depending on the memory space. Also, the wait settings for I/O and external memory spaces apply. The following is the access timing for each memory space, assuming no-wait situation.

- Internal ROM/RAM space 2 cycles
- I/O space (special registers) 3 cycles

In Figure:18.3.1 ATC1 Timing Chart, the time, from the rising of DMA activation request signal to the starting of LOAD cycle depends on the state of CPU, but it takes max. 9 cycles.

18.3.2 Memory Address Setting

■ Setting of transfer addresses to the memory pointers

The address of the memory space for an automatic data transfer (ATC1) should be set in the both of memory pointer 0 (AT1MAP0) and memory pointer 1 (AT1MAP1). In each transfer mode, one of those pointer is the source address, and another is the destination address.

■ Memory pointer 0 functions

Memory pointer 0 is consists of three 8-bit registers, AT1MAP0H, AT1MAP0M, and AT1MAP0L. AT1MAP0H holds upper 4bits of the 20-bit address, AT1MAP0M contains the middle 8 bits, and AT1MAP0L contains lower 8 bits. The 20-bit address set in memory pointer 0 points to a specific address in the total memory space of 1 MB. Memory pointer 0 also contains a computational function that enables it to increment the address based on the transfer state. You can disable this function for all transfer modes by setting the FMODE bit of ATC1 control register 0 to "1".

■ Memory pointer 1 functions

Memory pointer 1 is consists of three 8-bit registers, AT1MAP1H, AT1MAP1M, and AT1MAP1L. AT1MAP1H holds upper 4 bits of the 20-bit address, AT1MAP1M contains the middle 8 bits, and AT1MAP1L contains lower 8 bits. Depending on the transfer mode, either all 20 bits are valid, or only the least significant 8 bits (in AT1MAP1L) are valid. When only the 8 bits in AT1MAP1L are valid, the value 0x03F is assigned to the 12 bits in AT1MAP1H and AT1MAP1M, and the pointer points to the I/O space (special registers). Memory pointer 1 also contains a computational function that enables it to increment the address based on the transfer state.

18.3.3 Data Transfer Count Setting

■ Transfer data counter (AT1TRC) function

You can preset the data transfer count by ATC1. Set the value in the ATC1 transfer counter (AT1TRC). The counter decrements everytime when ATC1 transfers one byte of data.

The value in the transfer data counter is 0x00 at reset. Set the data transfer counts before activating ATC1. Note that ATC1 cannot be activated if the transfer data counter is set to 0x00.

■ Data transfer operations using the transfer data counter (AT1TRC)

There are two main types of ATC1 data transfers, standard and burst transfers. (See section 15.3.4 "Data Transfer Modes Setting"). The transfer counter operates differently depending on the transfer type.

1. Standard transfers [transfer modes 0 to D]

In standard transfers, the transfer counter decrements everytime when ATC1 is activated. When the counter reaches 0x00 after a data transfer, ATC1 generates an interrupt (ATC1IRQ). This means that for standard transfers, the program must set the counter to the number of times ATC1 needs to be activated.

2. Burst transfers [transfer modes E to F]

In burst transfers, one activation of ATC1 continuously transfers multiple bytes of data. In this case, the program must set the counter to the number of data bytes contained in the burst transfer. When the burst transfer starts, the transfer counter decrements everytime when one byte of data is transferred. When the counter reaches 0x00, ATC1 generates an interrupt (ATC1IRQ). It is also possible to force ATC1 to shut down during a burst transfer using external interrupt 0. (See section 18.3.4 "Data Transfer Modes Setting").

■ The transfer data counter (AT1TRC)

The transfer data counter can be set to a maximum 255 transfers (for standard transfers) or 255 bytes (for burst transfers). Note that setting the counter to 0x00 disables transfers.

18.3.4 Data Transfer Modes Setting

■ Data transfer modes

There are two types of ATC1 transfers, standard and burst, and sixteen transfer modes. Set the transfer mode in ATC1 control register 0 (AT1CNT0). [Table:18.1.2 Transfer Modes]

■ Standard and burst transfers

The ATC1 transfer modes are divided into standard transfer modes and burst transfer modes. There are fourteen standard modes, 0 to D, and two burst modes, E and F.

In standard modes, the operation specified for that mode executes everytime when ATC1 is activated. When the transfer ends, the value set in the transfer counter (AT1TRC) decrements and bus control returns to the MCU core. This operation repeats until the transfer counter reaches 0x00. When this happens, ATC1 completes the final data transfer, then generates an interrupt (ATC1IRQ).

For instance, if the initial transfer counter value is 0x05, and the ATC1 activation factor is set to a timer 0 interrupt, ATC1 is activated everytime when timer 0 overflows and the automatic transfer begins. After fifth data transfers (activated by fifth timer 0 overflow) is completed, the transfer counter value becomes 0x00, an ATC1 interrupt occurs, and the operation ends. Timer 0 overflows occurring after this point do not activate ATC1. For standard transfers, the program must set the transfer counter to the number of ATC1 activations required.

In burst modes, once ATC1 is activated, it transfers in one operation the number of bytes set in the transfer counter (AT1TRC). After the burst transfer begins, the transfer counter decrements everytime when ATC1 transfers one byte of data. When the counter reaches 0x00, ATC1 generates an interrupt (ATC1IRQ) and the burst transfer ends. For burst transfers, the program must set the transfer counter to the number of data bytes in the burst transfer.

The external interrupt 0 can also be used to shut down ATC1 during a burst transfer. To enable this function, set the burst transfer stop enable bit (BTSTP) in ATC1 control register 1 (AT1CNT1) to 1. When BTSTP = 1, ATC1 data transfers stop when the external interrupt 0 interrupt request flag (IRQ0IR flag in the IRQ0ICR register) is set. In an emergency shutdown, the transfer counter and memory pointer save the values prior to the shutdown. When the interrupt service routine ends, a new activation factor restarts ATC1, and the burst transfer begins transferring data from the point at which it stopped.

When burst transfer stop is enabled, do not select external interrupt 0 for ATC1trigger factor.

18.3.5 Transfer Mode 0

In transfer mode 0, ATC1 automatically transfers one byte of data from any memory space to the I/O space (special registers : 0x03F00 - 0x03FFF) everytime an ATC1 activation request occurs.

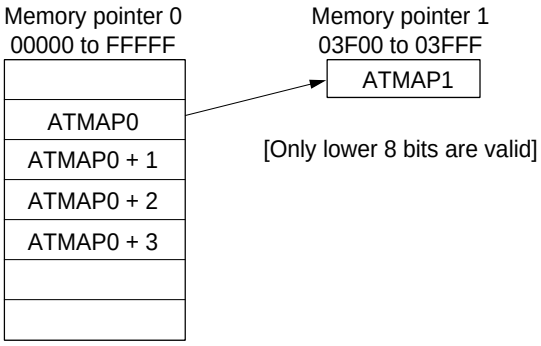


Figure:18.3.2 Transfer Mode 0

Set the source address in 20-bit memory pointer 0 (AT1MAP0H, M, L), and set the destination I/O address in lower 8 bits of memory pointer 1(AT1MAP1L). You do not have to set the upper 12 bits of the I/O space address (0x03F) in AT1MAP1H and AT1MAP1M.

Transfer mode 0 does not have an increment function for the memory pointers and executes data transfer for a fixed address.

Set the data transfer count for ATC1 in the transfer data counter (AT1TRC). Up to 255 transfers can be set. The counter decrements everytime an ATC1 is activated. When it reaches 0x00, an interrupt (ATC1IRQ) occurs and the automatic transfer ends.

18.3.6 Transfer Mode 1

In transfer mode 1, ATC1 automatically transfers one byte of data from the I/O space (special registers : 0x03F00-0x03FFF) to any memory space everytime an ATC1 activation request occurs.

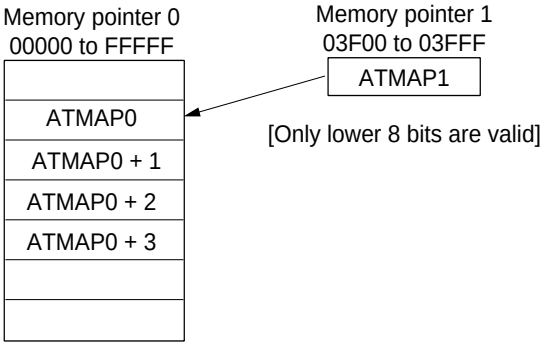


Figure:18.3.3 Transfer Mode 1

Set the source I/O address in lower 8 bits of memory pointer 1 (AT1MAP1L), and set the destination address in 20-bit memory pointer 0 (AT1MAP0H, M, L). You do not have to set the upper 12 bits of the I/O space address (0x03F) in AT1MAP1H and AT1MAP1M.

Transfer mode 1 does not have an increment function for the memory pointers and executes data transfer for a fixed address.

Set the data transfer count for ATC1 in the transfer data counter (AT1TRC). Up to 255 transfers can be set. The counter decrements everytime an ATC1 is activated. When it reaches 0x00, an interrupt (ATC1IRQ) occurs and the automatic transfer ends.

18.3.7 Transfer Mode 2

In transfer mode 2, ATC1 automatically transfers one byte of data from any memory space to the I/O space (special registers : 0x03F00 - 0x03FFF) everytime an ATC1 activation request occurs.

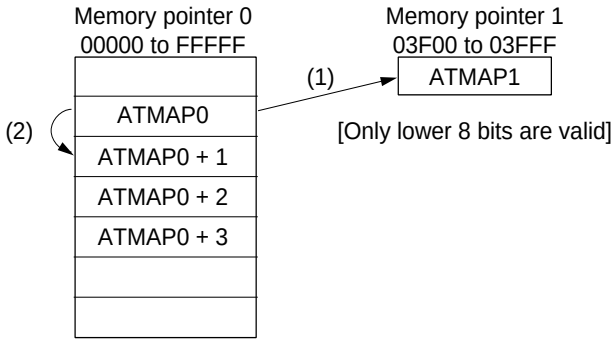


Figure:18.3.4 Transfer Mode 2

Set the source address in 20-bit memory pointer 0 (AT1MAP0H, M, L), and set the destination I/O address in lower 8 bits of memory pointer 1(AT1MAP1L). You do not have to set the upper 12 bits of the I/O space address (0x03F) in AT1MAP1H and AT1MAP1M.

In transfer mode 2, the value in memory pointer 0 increments everytime a byte-length data transfer ends. As a result, the source address for the next transfer is one address higher than that for the previous transfer.

Set the data transfer count for ATC1 in the transfer data counter (AT1TRC). Up to 255 transfers can be set. The counter decrements everytime an ATC1 is activated. When it reaches 0x00, an interrupt (ATC1IRQ) occurs and the automatic transfer ends.

18.3.8 Transfer Mode 3

In transfer mode 3, ATC1 automatically transfers one byte of data from the I/O space (special registers : 0x03F00 - 0x03FFF) to any memory space everytime an ATC1 activation request occurs.

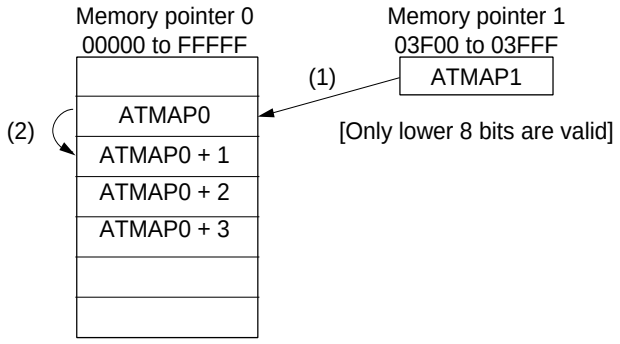


Figure:18.3.5 Transfer Mode 3

Set the source I/O address in lower 8 bits of memory pointer 1 (AT1MAP1L), and set the destination address in 20-bit memory pointer 0 (AT1MAP0H, M, L). You do not have to set the upper 12 bits of the I/O space address (0x3F) in AT1MAP1H and AT1MAP1M.

In transfer mode 3, the value in memory pointer 0 increments everytime a byte-length data transfer ends. As a result, the destination address for the next transfer is one address higher than that for the previous transfer.

Set the data transfer count for ATC1 in the transfer data counter (AT1TRC). Up to 255 transfers can be set. The counter decrements everytime an ATC1 is activated. When it reaches 0x00, an interrupt (ATC1IRQ) occurs and the automatic transfer ends.

18.3.9 Transfer Mode 4

In transfer mode 4, ATC1 automatically transfers two bytes (one word) of data from any memory space to the I/O space (special registers : 0x03F00 - 0x03FFF) everytime an ATC1 activation request occurs.

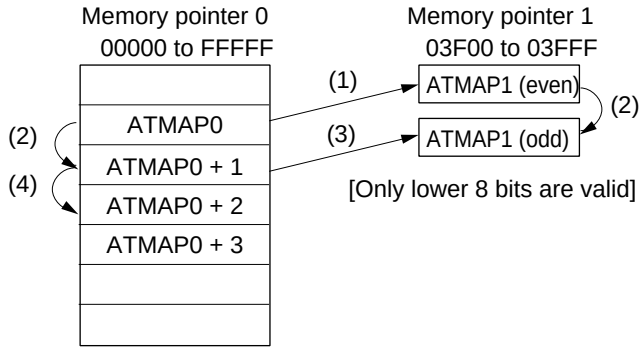


Figure:18.3.6 Transfer Mode 4

Set the source address in 20-bit memory pointer 0 (AT1MAP0H, M, L), and set the destination I/O address in the lower 8 bits of memory pointer 1(AT1MAP1L). You do not have to set the upper 12 bits of the I/O space address (0x03F) in AT1MAP1H and AT1MAP1M.

Always set an even address as the destination I/O address in memory pointer 1. When ATC1 transfers one word to the I/O space, ATC1 can transfer the even address set in memory pointer 1 and the consecutive odd address.

In transfer mode 4, ATC1 executes a data byte transfer twice to send one data word everytime when activated. The value in memory pointer 0 increments everytime a byte-length data transfer ends. As a result, the source address for the next ATC1 operation is two addresses higher than that for the previous operation.

In this word-length transfer, ATC1 transfers the first data byte to an even address in the I/O space and the second data byte to an odd address in the I/O space.

Set the data transfer data count for ATC1 in the transfer data counter (AT1TRC). Up to 255 transfers can be set. The counter decrements everytime ATC1 is activated (after each word transfer). When it reaches x'00', an interrupt (ATC1IRQ) occurs and the automatic transfer ends.

18.3.10 Transfer Mode 5

In transfer mode 5, ATC1 automatically transfers two bytes (one word) of data from the I/O space (special registers : 0x03F00' - 0x03FFF') to any memory space everytime an ATC1 activation request occurs.

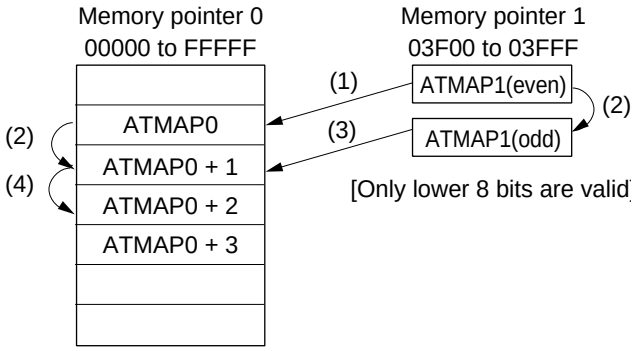


Figure:18.3.7 Transfer Mode 5

Set the source I/O address in lower 8 bits of memory pointer 1 (AT1MAP1L), and set the destination address in 20-bit memory pointer 0 (AT1MAP0H, M, L). You do not have to set the upper 12 bits of the I/O space address (0x3F) in AT1MAP1H and AT1MAP1M.

Always set an even address as the source I/O address in memory pointer 1. When ATC1 transfers one word from the I/O space, ATC1 can transfer the even address set in memory pointer 1 and the consecutive odd address.

In transfer mode 5, ATC1 executes a data byte transfer twice to send one data word everytime when activated. The value in memory pointer 0 increments by one each time a byte-length data transfer ends. As a result, the destination address for the next ATC1 operation is two addresses higher than that for the previous operation.

In this word-length transfer, ATC1 transfers the first data byte from an even address in the I/O space and the second data byte from an odd address in the I/O space.

Set the data transfer count for ATC1 in the transfer data counter (AT1TRC).Up to 255 transfers can be set. The counter decrements everytime an ATC1 is activated (after each word transfer). When it reaches 0x00, an interrupt (ATC1IRQ) occurs and the automatic transfer ends.

18.3.11 Transfer Mode 6

In transfer mode 6, ATC1 automatically transfers one byte of data two times everytime an ATC1 activation request occurs.

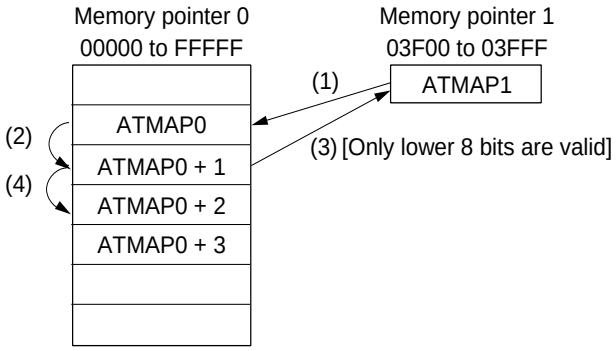


Figure:18.3.8 Transfer Mode 6

In this mode the transfer direction indicated by memory pointers 0 and 1 reverses for the second data byte transfer.

In the first data byte transfer, the I/O space address (0x03F00 - 0x03FFF) in memory pointer 1 is the source address, and the address in memory pointer 0, for any memory space, is the destination address. When the first data byte transfer ends, the address in memory pointer 0 increments by one.

In the second data byte transfer, the incremented address in memory pointer 0 becomes the source address, and the I/O space address (0x03F00 - 0x03FFF) in memory pointer 1 becomes the destination address. The adsdress in memory pointer 0 remains unchanged after the second data byte transfer ends.

Set the I/O address in lower 8 bits of memory pointer 1 (AT1MAP1L). You do not have to set the upper 12 bits of the I/O space address (0x03F) in AT1MAP1H, AT1MAP1M.

In transfer mode 6, ATC1 executes a data byte transfer twice everytime when activated. The value in memory pointer 0 increments by one everytime a byte-length data transfer ends. As a result, the source address for the next ATC1 operation is two addresses higher than that for the previous operation.

Set the data transfer count for ATC1 in the transfer data counter (AT1TRC). Up to 255 transfers can be set. The counter decrements everytime an ATC1 is activated (after one byte of data is transferred twice). When it reaches 0x00, an interrupt (ATC1IRQ) occurs and the automatic transfer ends.

18.3.12 Transfer Mode 7

In transfer mode 7, ATC1 automatically transfers one byte of data two times everytime an ATC1 activation request occurs.

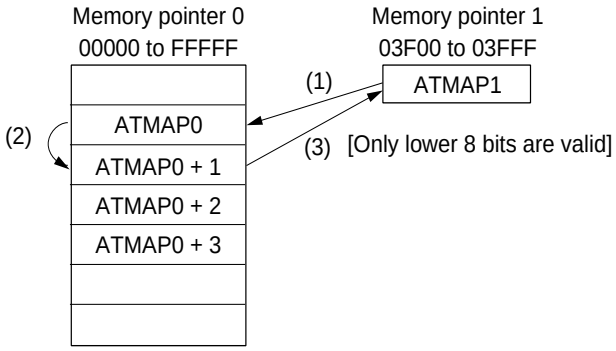


Figure:18.3.9 Transfer Mode 7

In this mode the transfer direction indicated by memory pointers 0 and 1 reverses for the second data byte transfer.

In the first data byte transfer, the I/O space address (0x03F00 - 0x03FF') in memory pointer 1 is the source address, and the address in memory pointer 0, for any memory space, is the destination address. When the first data byte transfer ends, the address in memory pointer 0 increments by one.

In the second data byte transfer, the incremented address in memory pointer 0 becomes the source address, and the I/O space address (0x03F00 - 0x03FFF) in memory pointer 1 becomes the destination address. The address in memory pointer 0 remains unchanged after the second data byte transfer ends.

Set the I/O address in lower 8 bits of memory pointer 1 (AT1MAP1L). You do not have to set the upper 12 bits of the I/O space address (0x03F) in AT1MAP1H, AT1MAP1M.

In transfer mode 7, ATC1 executes a data byte transfer twice everytime when activated. However, the value in memory pointer 0 increments by one only after the first transfer ends. As a result, the source address for the next ATC1 operation is one address higher than that for the previous operation.

Set the data transfer count for ATC1 in the transfer data counter (AT1TRC). Up to 255 transfers can be set. The counter decrements everytime an ATC1 is activated (after one byte of data has been transferred twice). When it reaches 0x00, an interrupt (ATC1IRQ) occurs and the automatic transfer ends.

18.3.13 Transfer Mode 8

In transfer mode 8, ATC1 automatically transfers one byte of data two times everytime an ATC1 activation request occurs.

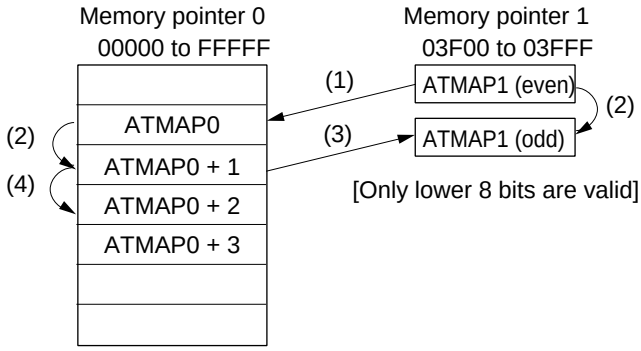


Figure:18.3.10 Transfer Mode 8

In this mode the transfer direction indicated by memory pointers 0 and 1 reverses for the second data byte transfer.

In the first data byte transfer, the I/O space address (0x03F00 - 0x03FFF) in memory pointer 1 is the source address, and the address in memory pointer 0, for any memory space, is the destination address. When the first data byte transfer ends, the address in memory pointer 0 increments by one.

In the second data byte transfer, the incremented address in memory pointer 0 becomes the source address, and the I/O space address (0x03F00 - 0x03FFF) in memory pointer 1 becomes the destination address. When the second data byte transfer ends, the address in memory pointer 0 increments again.

Set an even I/O address in the lower 8 bits of memory pointer 1 (AT1MAP1L). You do not have to set the upper 12 bits of the I/O space address (0x03F) in AT1MAP1H, AT1MAP1M.

Always set an even I/O address in memory pointer 1. In this double transfer of a data byte from and to the I/O space, ATC1 targets the even I/O address set in memory pointer 1 and the consecutive odd address. In this mode, the first data byte transfer accesses an even I/O address and the second data byte transfer accesses an odd I/O address.

Transfer mode 8 can be used to support continuous transmission/ reception for serial interface 0,1 and 2. Set the memory pointer 1 to point to the serial reception buffer (RXBUF0, RXBUF1) and select serial interrupts as the ATC1 trigger factor. In this way, everytime the serial communication ends, the MCU continuously reads the reception data (first data byte transfer), then writes the transmission data to the transmission buffer (TXBUF0, TXBUF1) (second data byte transfer) up to 255 times, entirely through the hardware.

Before execute a continuous serial transaction, store the serial transmission data in the memory space that memory pointer 0 points, the transmission data must fill every other address in the space. Once the serial transaction ends, the received data is stored in empty (skipped) addresses and the transmission and reception data at stored in an alternative pattern.

In transfer mode 8, ATC1 executes a data byte transfer twice each time it is activated. The value in memory pointer 0 increments by one everytime a byte-length data transfer ends. As a result, the source address for the next ATC1 operation is two addresses higher than that for the previous operation.

Set the data transfer count for ATC1 in the transfer data counter (AT1TRC). Up to 255 transfers can be set. The counter decrements everytime an ATC1 is activated (after one byte of data is transferred twice). When it reaches 0x00, an interrupt (ATC1IRQ) occurs and the automatic transfer ends.

18.3.14 Transfer Mode 9

In transfer mode 9, ATC1 automatically transfers one byte of data two times everytime an ATC1 activation request occurs.

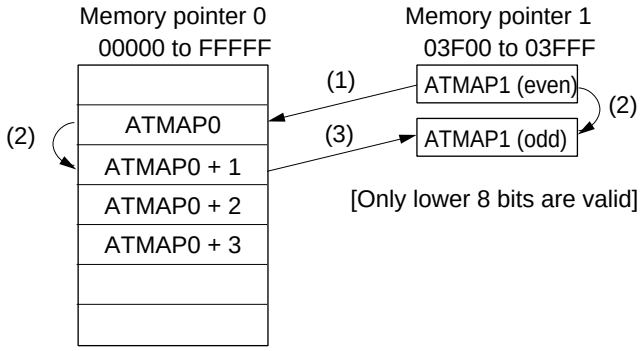


Figure:18.3.11 Transfer Mode 9

In this mode the transfer direction indicated by memory pointers 0 and 1 reverses for the second data byte transfer.

In the first data byte transfer, the I/O space address (0x03F00 - 0x03FFF) in memory pointer 1 is the source address, and the address in memory pointer 0 for any memory space is the destination address. When the first data byte transfer ends, the address in memory pointer 0 increments by one.

In the second data byte transfer, the incremented address in memory pointer 0 becomes the source address, and the I/O space address (0x03F00 - 0x03FFF) in memory pointer 1 becomes the destination address. The address in memory pointer 0 remains unchanged after the second data byte transfer ends.

Set an even I/O address in lower 8 bits of memory pointer 1 (AT1MAP1L). You do not have to set the upper 12 bits of the I/O space address (0x03F) in AT1MAP1H, AT1MAP1M.

Always set an even I/O address in memory pointer 1. In this double transfer of a data byte from and to the I/O space, ATC1 targets the even I/O address set in memory pointer 1 and the consecutive odd address. In this mode, the first data byte transfer accesses an even I/O address and the second data byte transfer accesses an odd I/O address.

Transfer mode 9 can be used to support continuous transmission/ reception for serial interface 0,1 and 2. Set the memory pointer 1 to point to the serial reception buffer (RXBUF0, RXBUF1) and select serial interrupts as the ATC1 trigger factor. In this way, everytime a serial communication ends, the MCU continuously reads the reception data (first data byte transfer), then writes the transmission data to the transmission buffer (TXBUF0, TXBUF1) (second data byte transfer) up to 255 times, entirely through the hardware.

Before execute a continuous serial transaction, store the serial transmission data in the memory space that memory pointer 0 points, once the serial communication ends, the MCU has written to the reception data over the transmission data, so that only reception data remains in the memory.

In transfer mode 9, ATC1 executes a data byte transfer twice everytime when activated. However, the value in memory pointer 0 increments by one only after the first transfer ends. As a result, the source address for the next ATC1 operation is one address higher than that for the previous operation.

Set the data transfer count for ATC1 in the transfer data counter (AT1TRC). Up to 255 transfers can be set. The counter decrements everytime an ATC1 is activated (after one byte of data is transferred twice). When it reaches 0x00, an interrupt (ATC1IRQ) occurs and the automatic transfer ends.

18.3.15 Transfer mode A

In transfer mode A, ATC1 automatically transfers one byte of data from any memory space to any other memory space everytime an ATC1 activation request occurs.

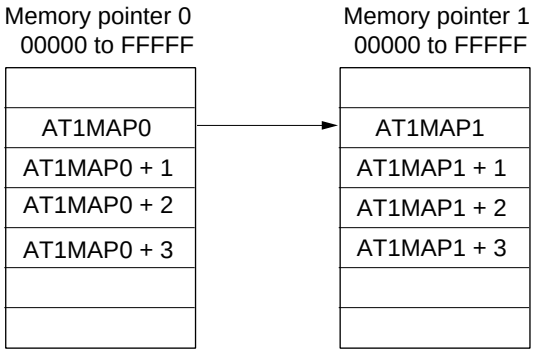


Figure:18.3.12 Transfer Mode A

Set the source address in 20-bit memory pointer 0 (AT1MAP0H, M, L), and set the destination address in 20-bit memory pointer 1 (AT1MAP0H, M, L).

Transfer mode A does not have an increment function for the memory pointers and executes data transfer for a fixed address.

Set the data transfer count for ATC1 in the transfer data counter (AT1TRC). Up to 255 transfers can be set. The counter decrements everytime an ATC1 is activated. When it reaches 0x00, an interrupt (ATC1IRQ) occurs and the automatic transfer ends.

18.3.16 Transfer Mode B

In transfer mode B, ATC1 automatically transfers one byte of data from any memory space to any other memory space everytime an ATC1 activation request occurs.

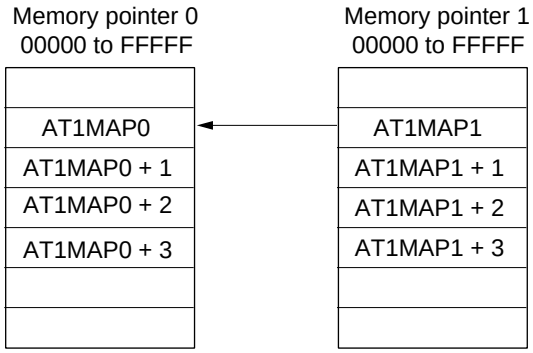


Figure:18.3.13 Transfer Mode B

Set the source address in 20-bit memory pointer 1 (AT1MAP1H, M, L), and set the destination address in 20-bit memory pointer 0 (AT1MAP0H, M, L).

Transfer mode B does not have an increment function for the memory pointers and executes data transfer for a fixed address.

Set the data transfer count for ATC1 in the transfer data counter (AT1TRC). Up to 255 transfers can be set. The counter decrements everytime an ATC1 is activated. When it reaches 0x00, an interrupt (ATC1IRQ) occurs and the automatic transfer ends.

18.3.17 Transfer Mode C

In transfer mode C, ATC1 automatically transfers one byte of data from any memory space to any other memory space everytime an ATC1 activation request occurs.

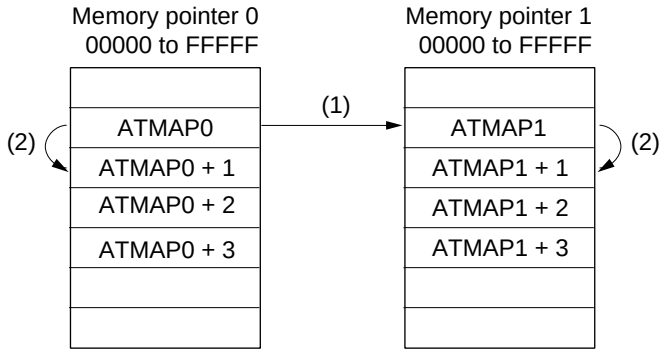


Figure:18.3.14 Transfer Mode C

Set the source address in 20-bit memory pointer 0 (AT1MAP0H, M, L), and set the destination address in 20-bit memory pointer 1 (AT1MAP1H, M, L).

In transfer mode C, the values in memory pointers 0 and 1 increment everytime a byte-length data transfer ends. As a result, the source and destination addresses for the next transfer are one address higher than those for the original transfer.

Set the data transfer count for ATC1 in the transfer data counter (AT1TRC). Up to 255 transfers can be set. The counter decrements everytime an ATC1 is activated. When it reaches 0x00, an interrupt (ATC1IRQ) occurs and the automatic transfer ends.

18.3.18 Transfer Mode D

In transfer mode D, ATC1 automatically transfers one byte of data from any memory space to any other memory space everytime an ATC1 activation request occurs.

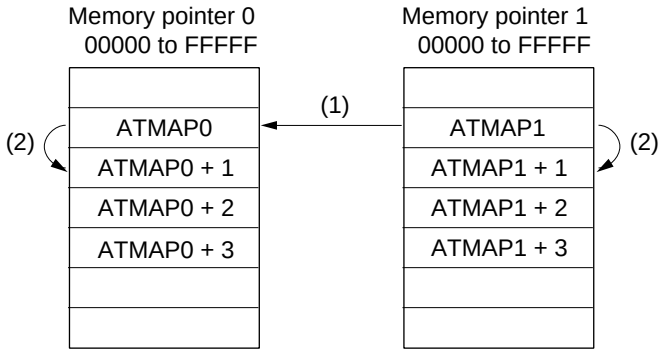


Figure:18.3.15 Transfer Mode D

Set the source address in 20-bit memory pointer 1 (AT1MAP1H, M, L), and set the destination address in 20-bit memory pointer 0 (AT1MAP0H, M, L).

In transfer mode D, the values in memory pointers 0 and 1 increment everytime a byte-length data transfer ends. As a result, the source and destination addresses for the next transfer are one address higher than those for the original transfer.

Set the data transfer count for ATC1 in the transfer data counter (AT1TRC). Up to 255 transfers can be set. The counter decrements everytime an ATC1 is activated. When it reaches 0x00, an interrupt (ATC1IRQ) occurs and the automatic transfer ends.

18.3.19 Transfer Mode E

Transfer mode E is a burst mode. In this mode, when ATC1 is activated, it automatically transfers the number of data bytes set in the transfer data counter (AT1TRC) in one continuous operation.

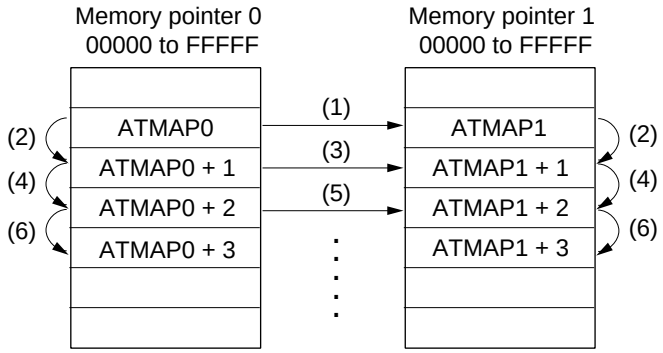


Figure:18.3.16 Transfer Mode E

Set the source address in 20-bit memory pointer 0 (AT1MAP0H, M, L), and set the destination address in 20-bit memory pointer 1 (AT1MAP1H, M, L). Once ATC1 is activated, memory pointers 0 and 1 increment everytime a byte-length data transfer ends.

For burst transfers, set the number of data bytes to be transferred in the transfer data counter (AT1TRC). Up to 255 transfers can be set. Once the burst transfer starts, the counter decrements everytime an ATC1 transfers one byte of data. When it reaches 0x00, an interrupt (ATC1IRQ) occurs and the burst transfer ends.

You can shut down ATC1 during burst transfers using external interrupt 0. You can enable or disable ATC1 shut-down with the burst transfer stop enable flag (BSTP) of ATC1 control register 1 (AT1CNT1).

When BTSTP=1 and the interrupt request flag for external interrupt 0 (the IRQ0IR flag in the IRQ0ICR register) is set, the ATC1 data transfer shuts down immediately. During this shutdown, the transfer counter and the memory pointers save the values they contained prior to the shutdown. When the interrupt service routine ends and a new ATC1 trigger factor occurs, the burst transfer restarts from the point at which it stopped.

When burst transfer stop is enabled, do not select external interrupt 0 for ATC1trigger factor.

18.3.20 Transfer Mode F

Transfer mode F is a burst mode. In this mode, when ATC1 is activated, it automatically transfers the number of data bytes set in the transfer data counter (AT1TRC) in one continuous operation.

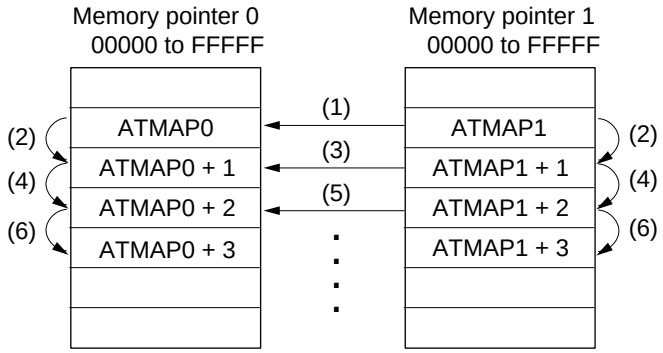


Figure:18.3.17 Transfer Mode F

Set the source address in 20-bit memory pointer 1 (AT1MAP1H, M, L), and set the destination address in 20-bit memory pointer 0 (AT1MAP0H, M, L). Once ATC1 is activated, memory pointers 0 and 1 increment everytime a byte-length data transfer ends.

For burst transfers, set the number of data bytes to be transferred in the transfer data counter (AT1TRC). Up to 255 transfers can be set. Once the burst transfer starts, the counter decrements everytime ATC1 transfers one byte of data. When it reaches 0x00, an interrupt (ATC1IRQ) occurs and the burst transfer ends.

You can shut down ATC1 during burst transfers using external interrupt 0. You can enable or disable ATC1 shut-down with the burst transfer stop enable flag (BSTP) of ATC1 control register 1 (AT1CNT1).

When BTSTP=1 and the interrupt request flag for external interrupt 0 (the IRQ0IR flag in the IRQ0ICR register) is set, the ATC1 data transfer shuts down immediately. During this shutdown, the transfer counter and the memory pointers save the values they contained prior to the shutdown. When the interrupt service routine ends and a new ATC1 trigger factor occurs, the burst transfer restarts from the point at which it stopped.

When burst transfer stop is enabled, do not select external interrupt 0 for ATC1trigger factor.

18.4 Setup Example

An example setup procedure, with a description of each step is as follows ;

Setup Procedure	Description
(1) Set the data transfer mode. AT1CNT0 (0x3FD0) bp7 :FMODE bp6 :AT1ACT = 0 bp5-2 :AT1MD3-0 bp0 :AT1EN = 0	(1) Select the data transfer mode with the AT1MD flag in the AT1CNT0 register. No matter which mode you select, setting the FMODE flag disables the increment function in memory pointer 0.Normally set this flag to 0.Note that you must set the ATC1 enable flag, AT1EN, to 0 at this step.Only enable ATC1 after setting all the other registers.
(2) Set memory pointer 0. AT1MAP0L (0x03FD3) AT1MAP0M (0x03FD4) AT1MAP0H (0x03FD5)	(2) Set the source or destination address in the AT1MAP0 registers depending on the transfer mode you select.
(3) Set memory pointer 1. AT1MAP1L (0x03FD6) AT1MAP1M (0x03FD7) AT1MAP1H (0x03FD8)	(3) Set the source or destination address in the AT1MAP1 registers depending on the transfer mode you select.
(4) Set the transfer data counter. AT1TRC (0x03FD2)	(4) Set the ATC1 data transfer count in the AT1TRC register.
(5) Select the ATC1 activation factor. AT1CNT1 (0x03FD1) bp4 :BTSTP bp3-0 :AT1IR3-0	(5) Select the ATC1 activation factor with the AT1IR flag in the AT1CNT1 register. If you select a burst-type transfer mode, then you must also enable or disable ATC1 shutdown at this step, by setting the BTSTP.
(6) Enable ATC operation. AT1CNT0 (0x03FD0) bp0 :AT1EN = 1	(6) Enable ATC1 data transfers with the AT1EN flag in the AT1CNT0 register.

To activate ATC1 in the software, first complete steps (1) to (6), then set the AT1ACT flag in the AT1CNT0 register. After the AT1ACT flag is set, ATC1 is started and data transfer is started. The hardware automatically clears AT1ACT flag when ATC1 is activated. In standard transfer mode, set a program that sets flags as many as necessary for the the data transfer.

Chapter 19 Appendix

19

19.1 Instruction Set

MN101E SERIES INSTRUCTION SET

Group	Mnemonic	Operation	Flag				Code Size	Cycle	Re-peat	Machine Code												Notes
			VF	NF	CF	ZF				Ext.	1	2	3	4	5	6	7	8	9	10	11	
Data Move Instructions																						
MOV	MOV Dn,Dm	Dn→Dm	--	--	--	--	2	1			1010 DnDm											
	MOV imm8,Dm	imm8→Dm	--	--	--	--	4	2			1010 DmDm	<#8.	...>									
	MOV Dn,PSW	Dn→PSW	●	●	●	●	3	3		0010	1001 01Dn											
	MOV PSW,Dm	PSW→Dm	--	--	--	--	3	2		0010	0001 01Dm											
	MOV (An),Dm	mem8(An)→Dm	--	--	--	--	2	2			0100 1ADm											
	MOV (d8,An),Dm	mem8(d8+An)→Dm	--	--	--	--	4	2			0110 1ADm	<d8.	...>									*1
	MOV (d16,An),Dm	mem8(d16+An)→Dm	--	--	--	--	7	4		0010	0110 1ADm	<d16	....	....	...>							
	MOV (d4,SP),Dm	mem8(d4+SP)→Dm	--	--	--	--	3	2			0110 01Dm	<d4>										*2
	MOV (d8,SP),Dm	mem8(d8+SP)→Dm	--	--	--	--	5	3		0010	0110 01Dm	<d8.	...>									*3
	MOV (d16,SP),Dm	mem8(d16+SP)→Dm	--	--	--	--	7	4		0010	0110 00Dm	<d16	....	....	...>							
	MOV (io8),Dm	mem8(IOTOP+io8)→Dm	--	--	--	--	4	2			0110 00Dm	<io8	...>									
	MOV (abs8),Dm	mem8(abs8)→Dm	--	--	--	--	4	2			0100 01Dm	<abs	8..>									
	MOV (abs12),Dm	mem8(abs12)→Dm	--	--	--	--	5	2			0100 00Dm	<abs	12..	...>								
	MOV (abs16),Dm	mem8(abs16)→Dm	--	--	--	--	7	4		0010	1100 00Dm	<abs	16..	....	...>							
	MOV Dn,(Am)	Dn→mem8(Am)	--	--	--	--	2	2			0101 1aDn											
	MOV Dn,(d8,Am)	Dn→mem8(d8+Am)	--	--	--	--	4	2			0111 1aDn	<d8.	...>									*1
	MOV Dn,(d16,Am)	Dn→mem8(d16+Am)	--	--	--	--	7	4		0010	0111 1aDn	<d16	....	....	...>							
	MOV Dn,(d4,SP)	Dn→mem8(d4+SP)	--	--	--	--	3	2			0111 01Dn	<d4>										*2
	MOV Dn,(d8,SP)	Dn→mem8(d8+SP)	--	--	--	--	5	3		0010	0111 01Dn	<d8.	...>									*3
	MOV Dn,(d16,SP)	Dn→mem8(d16+SP)	--	--	--	--	7	4		0010	0111 00Dn	<d16	....	....	...>							
	MOV Dn,(io8)	Dn→mem8(IOTOP+io8)	--	--	--	--	4	2			0111 00Dn	<io8	...>									
	MOV Dn,(abs8)	Dn→mem8(abs8)	--	--	--	--	4	2			0101 01Dn	<abs	8..>									
	MOV Dn,(abs12)	Dn→mem8(abs12)	--	--	--	--	5	2			0101 00Dn	<abs	12..	...>								
	MOV Dn,(abs16)	Dn→mem8(abs16)	--	--	--	--	7	4		0010	1101 00Dn	<abs	16..	....	...>							
	MOV imm8,(io8)	imm8→mem8(IOTOP+io8)	--	--	--	--	6	3			0000 0010	<io8	...>	<#8.	...>							
	MOV imm8,(abs8)	imm8→mem8(abs8)	--	--	--	--	6	3			0001 0100	<abs	8..>	<#8.	...>							
	MOV imm8,(abs12)	imm8→mem8(abs12)	--	--	--	--	7	3			0001 0101	<abs	12..	...>	<#8.	...>						
	MOV imm8,(abs16)	imm8→mem8(abs16)	--	--	--	--	9	5		0011	1101 1001	<abs	16..	....	...>	<#8.	...>					
	MOV Dn,(HA)	Dn→mem8(HA)	--	--	--	--	2	2			1101 00Dn											
MOVW	MOVW (An),DWm	mem16(An)→DWm	--	--	--	--	2	3			1110 00Ad											
	MOVW (An),Am	mem16(An)→Am	--	--	--	--	3	4		0010	1110 10Aa											*4
	MOVW (d4,SP),DWm	mem16(d4+SP)→DWm	--	--	--	--	3	3			1110 011d	<d4>										*2
	MOVW (d4,SP),Am	mem16(d4+SP)→Am	--	--	--	--	3	3			1110 010a	<d4>										*2
	MOVW (d8,SP),DWm	mem16(d8+SP)→DWm	--	--	--	--	5	4		0010	1110 011d	<d8.	...>									*3
	MOVW (d8,SP),Am	mem16(d8+SP)→Am	--	--	--	--	5	4		0010	1110 010a	<d8.	...>									*3
	MOVW (d16,SP),DWm	mem16(d16+SP)→DWm	--	--	--	--	7	5		0010	1110 001d	<d16	....	....	...>							
	MOVW (d16,SP),Am	mem16(d16+SP)→Am	--	--	--	--	7	5		0010	1110 000a	<d16	....	....	...>							
	MOVW (abs8),DWm	mem16(abs8)→DWm	--	--	--	--	4	3			1100 011d	<abs	8..>									
	MOVW (abs8),Am	mem16(abs8)→Am	--	--	--	--	4	3			1100 010a	<abs	8..>									
	MOVW (abs16),DWm	mem16(abs16)→DWm	--	--	--	--	7	5		0010	1100 011d	<abs	16..	....	...>							
	MOVW (abs16),Am	mem16(abs16)→Am	--	--	--	--	7	5		0010	1100 010a	<abs	16..	....	...>							
	MOVW DWn,(Am)	DWn→mem16(Am)	--	--	--	--	2	3			1111 00aD											
	MOVW An,(Am)	An→mem16(Am)	--	--	--	--	3	4		0010	1111 10aA											*4
	MOVW DWn,(d4,SP)	DWn→mem16(d4+SP)	--	--	--	--	3	3			1111 011D	<d4>										*2
	MOVW An,(d4,SP)	An→mem16(d4+SP)	--	--	--	--	3	3			1111 010A	<d4>										*2
	MOVW DWn,(d8,SP)	DWn→mem16(d8+SP)	--	--	--	--	5	4		0010	1111 011D	<d8.	...>									*3
	MOVW An,(d8,SP)	An→mem16(d8+SP)	--	--	--	--	5	4		0010	1111 010A	<d8.	...>									*3
	MOVW DWn,(d16,SP)	DWn→mem16(d16+SP)	--	--	--	--	7	5		0010	1111 001D	<d16	....	....	...>							
	MOVW An,(d16,SP)	An→mem16(d16+SP)	--	--	--	--	7	5		0010	1111 000A	<d16	....	....	...>							
	MOVW DWn,(abs8)	DWn→mem16(abs8)	--	--	--	--	4	3			1101 011D	<abs	8..>									
	MOVW An,(abs8)	An→mem16(abs8)	--	--	--	--	4	3			1101 010A	<abs	8..>									
	MOVW DWn,(abs16)	DWn→mem16(abs16)	--	--	--	--	7	5		0010	1101 011D	<abs	16..	....	...>							
	MOVW An,(abs16)	An→mem16(abs16)	--	--	--	--	7	5		0010	1101 010A	<abs	16..	....	...>							
	MOVW DWn,(HA)	DWn→mem16(HA)	--	--	--	--	2	3			1001 010D											
	MOVW An,(HA)	An→mem16(HA)	--	--	--	--	2	3			1001 011A											
	MOVW imm8,DWm	sign(imm8)→DWm	--	--	--	--	4	2			0000 110d	<#8.	...>									*5
	MOVW imm8,Am	zero(imm8)→Am	--	--	--	--	4	2			0000 111a	<#8.	...>									*6
	MOVW imm16,DWm	imm16→DWm	--	--	--	--	6	3			1100 111d	<#16	....	....	...>							

*1 d8 sign-extension *4 A=An, a=Am
*2 d4 zero-extension *5 #8 sign-extension
*3 d8 zero-extension *6 #8 zero-extension

MN101E SERIES INSTRUCTION SET

Group	Mnemonic	Operation	Flag VF	Flag NF	Flag CF	Flag ZF	Code Size	Cycle	Re-peat	extension	1	2	3	4	5	6	7	8	9	10	11	Notes
	MOVW imm16,Am	imm16→Am	--	--	--	--	6	3			1101	111a	<#16	....	....	...>						
	MOVW SP,Am	SP→Am	--	--	--	--	3	3			0010	0000	100a									
	MOVW An,SP	An→SP	--	--	--	--	3	3			0010	0000	101A									
	MOVW DWn,DWm	DWn→DWm	--	--	--	--	3	3			0010	1000	00Dd									*1
	MOVW DWn,Am	DWn→Am	--	--	--	--	3	3			0010	0100	11Da									
	MOVW An,DWm	An→DWm	--	--	--	--	3	3			0010	1100	11Ad									
	MOVW An,Am	An→Am	--	--	--	--	3	3			0010	0000	00Aa									*2
PUSH	PUSH Dn	SP-1→SP,Dn→mem8(SP)	--	--	--	--	2	3			1111	10Dn										
	PUSH An	SP-2→SP,An→mem16(SP)	--	--	--	--	2	5			0001	011A										
POP	POP Dn	mem8(SP)→Dn,SP+1→SP	--	--	--	--	2	3			1110	10Dn										
	POP An	mem16(SP)→An,SP+2→SP	--	--	--	--	2	4			0000	011A										
EXT	EXT Dn,DWm	sign(Dn)→DWm	--	--	--	--	3	3			0010	1001	000d									*3
Arithmetic manupulation instructions																						
ADD	ADD Dn,Dm	Dm+Dn→Dm	●	●	●	●	3	2			0011	0011	DnDm									
	ADD imm4,Dm	Dm+sign(imm4)→Dm	●	●	●	●	3	2			1000	00Dm	<#4>									*6
	ADD imm8,Dm	Dm+imm8→Dm	●	●	●	●	4	2			0000	10Dm	<#8.	...>								
ADDC	ADDC Dn,Dm	Dm+Dn+CF→Dm	●	●	●	●	3	2	○		0011	1011	DnDm									
ADDW	ADDW DWn,DWm	DWm+DWn→DWm	●	●	●	●	3	3	○		0010	0101	00Dd									*1
	ADDW DWn,Am	Am+DWn→Am	●	●	●	●	3	3	○		0010	0101	10Da									
	ADDW imm4,Am	Am+sign(imm4)→Am	●	●	●	●	3	2			1110	110a	<#4>									*6
	ADDW imm8,Am	Am+sign(imm8)→Am	●	●	●	●	5	3			0010	1110	110a	<#8.	...>							*7
	ADDW imm16,Am	Am+imm16→Am	●	●	●	●	7	4			0010	0101	011a	<#16	....	....	...>					
	ADDW imm4,SP	SP+sign(imm4)→SP	--	--	--	--	3	2			1111	1101	<#4>									*6
	ADDW imm8,SP	SP+sign(imm8)→SP	--	--	--	--	4	2			1111	1100	<#8.	...>								*7
	ADDW imm16,SP	SP+imm16→SP	--	--	--	--	7	4			0010	1111	1100	<#16	....	....	...>					
	ADDW imm16,DWm	DWm+imm16→DWm	●	●	●	●	7	4			0010	0101	010d	<#16	....	....	...>					
ADDUW	ADDUW Dn,Am	Am+zero(Dn)→Am	●	●	●	●	3	3	○		0010	1000	1aDn									*8
ADDSW	ADDSW Dn,Am	Am+sign(Dn)→Am	●	●	●	●	3	3	○		0010	1001	1aDn									
SUB	SUB Dn,Dm(when Dn≠Dm)	Dm-Dn→Dm	●	●	●	●	3	2	○		0010	1010	DnDm									
	SUB Dn,Dn	Dn-Dn→Dn	0	0	0	1	2	1			1000	01Dn										
	SUB imm8,Dm	Dm-imm8→Dm	●	●	●	●	5	3			0010	1010	DmDm	<#8.	...>							
SUBC	SUBC Dn,Dm	Dm-Dn-CF→Dm	●	●	●	●	3	2	○		0010	1011	DnDm									
SUBW	SUBW DWn,DWm	DWm-DWn→DWm	●	●	●	●	3	3			0010	0100	00Dd									*1
	SUBW DWn,Am	Am-DWn→Am	●	●	●	●	3	3			0010	0100	10Da									
	SUBW imm16,DWm	DWm-imm16→DWm	●	●	●	●	7	4			0010	0100	010d	<#16	....	....	...>					
	SUBW imm16,Am	Am-imm16→Am	●	●	●	●	7	4			0010	0100	011a	<#16	....	....	...>					
MULU	MULU Dn,Dm	Dm*Dn→DWk	0	●	●	●	3	8			0010	1111	111D									*4
DIVU	DIVU Dn,DWm	DWm/Dn→DWm-l...DWm-h	●	●	●	●	3	9			0010	1110	111d									*5
CMP	CMP Dn,Dm	Dm-Dn...PSW	●	●	●	●	3	2			0011	0010	DnDm									
	CMP imm8,Dm	Dm-imm8...PSW	●	●	●	●	4	2			1100	00Dm	<#8.	...>								
	CMP imm8,(abs8)	mem8(abs8)-imm8...PSW	●	●	●	●	6	3			0000	0100	<abs	8..>	<#8.	...>						
	CMP imm8,(abs12)	mem8(abs12)-imm8...PSW	●	●	●	●	7	3			0000	0101	<abs	12..	...>	<#8.	...>					
	CMP imm8,(abs16)	mem8(abs16)-imm8...PSW	●	●	●	●	9	5			0011	1101	1000	<abs	16..	....	...>	<#8.	...>			
CMPW	CMPW DWn,DWm	DWm-DWn...PSW	●	●	●	●	3	3			0010	1000	01Dd									*1
	CMPW DWn,Am	Am-DWn...PSW	●	●	●	●	3	3			0010	0101	11Da									
	CMPW An,Am	Am-An...PSW	●	●	●	●	3	3			0010	0000	01Aa									*2
	CMPW imm16,DWm	DWm-imm16...PSW	●	●	●	●	6	3			1100	110d	<#16	....	....	...>						
	CMPW imm16,Am	Am-imm16...PSW	●	●	●	●	6	3			1101	110a	<#16	....	....	...>						
Logical manipulation instructions																						
AND	AND Dn,Dm	Dm&Dn→Dm	0	●	0	●	3	2			0011	0111	DnDm									
	AND imm8,Dm	Dm&imm8→Dm	0	●	0	●	4	2			0001	11Dm	<#8.	...>								
	AND imm8,PSW	PSW&imm8→PSW	●	●	●	●	5	3			0010	1001	0010	<#8.	...>							
OR	OR Dn,Dm	DmIDn→Dm	0	●	0	●	3	2			0011	0110	DnDm									
	OR imm8,Dm	DmIimm8→Dm	0	●	0	●	4	2			0001	10Dm	<#8.	...>								
	OR imm8,PSW	PSWIimm8→PSW	●	●	●	●	5	3			0010	1001	0011	<#8.	...>							
XOR	XOR Dn,Dm	Dm^Dn→Dm	0	●	0	●	3	2			0011	1010	DnDm									*9
	XOR imm8,Dm	Dm^imm8→Dm	0	●	0	●	5	3			0011	1010	DmDm	<#8.	...>							

*1 D=DWn, d=DWm
*2 A=An, a=Am
*3 d=DWm
*4 D=DWk
*5 D=DWm
*6 #4 sign-extension
*7 #8 sign-extension
*8 Dn zero extension
*9 m≠n

MN101E SERIES INSTRUCTION SET

Group	Mnemonic	Operation	Flag VF	Flag NF	Flag CF	Flag ZF	Code Size	Cycle	Re-peat	Extension	Machine Code 1	2	3	4	5	6	7	8	9	10	11	Notes
NOT	NOT Dn	¯Dn→Dn=	0	●	0	●	3	2			0010	0010	10Dn									
ASR	ASR Dn	Dn.msb→temp,Dn.lsb→CF Dn>>1→Dn,temp→Dn.msb	0	--	●	●	3	2	○		0010	0011	10Dn									
LSR	LSR Dn	Dn.lsb→CF,Dn>>1→Dn 0→Dn.msb	0	0	●	●	3	2	○		0010	0011	11Dn									
ROR	ROR Dn	Dn.lsb→temp,Dn>>1→Dn CF→Dn.msb,temp→CF	0	●	●	●	3	2	○		0010	0010	11Dn									
Bit manipulation instructions																						
BSET	BSET (io8)bp	mem8(IOTOP+io8)&bpdata...PSW 1→mem8(IOTOP+io8)bp	0	●	0	●	5	5			0011	1000	0bp.	<io8	...>							
	BSET (abs8)bp	mem8(abs8)&bpdata...PSW 1→mem8(abs8)bp	0	●	0	●	4	4				1011	0bp.	<abs	8..>							
	BSET (abs16)bp	mem8(abs16)&bpdata...PSW 1→mem8(abs16)bp	0	●	0	●	7	6			0011	1100	0bp.	<abs	16..	....	...>					
BCLR	BCLR (io8)bp	mem8(IOTOP+io8)&bpdata...PSW 0→mem8(IOTOP+io8)bp	0	●	0	●	5	5			0011	1000	1bp.	<io8	...>							
	BCLR (abs8)bp	mem8(abs8)&bpdata...PSW 0→mem8(abs8)bp	0	●	0	●	4	4				1011	1bp.	<abs	8..>							
	BCLR (abs16)bp	mem8(abs16)&bpdata...PSW 0→mem8(abs16)bp	0	●	0	●	7	6			0011	1100	1bp.	<abs	16..	....	...>					
BTST	BTST imm8,Dm	Dm&imm8...PSW	0	●	0	●	5	3			0010	0000	11Dm	<#8.	...>							
	BTST (abs16)bp	mem8(abs16)&bpdata...PSW	0	●	0	●	7	5			0011	1101	0bp.	<abs	16..	....	...>					
Branch instructions																						
Bcc	BEQ label	if(ZF=1), PC+3+d4(label)+H→PC if(ZF=0), PC+3→PC	--	--	--	--	3	2/3				1001	000H	<d4>								*1
	BEQ label	if(ZF=1), PC+4+d7(label)+H→PC if(ZF=0), PC+4→PC	--	--	--	--	4	2/3				1000	1010	<d7.	...H							*2
	BEQ label	if(ZF=1), PC+5+d11(label)+H→PC if(ZF=0), PC+5→PC	--	--	--	--	5	2/3				1001	1010	<d11	....	...H						*3
	BNE label	if(ZF=0), PC+3+d4(label)+H→PC if(ZF=1), PC+3→PC	--	--	--	--	3	2/3				1001	001H	<d4>								1
	BNE label	if(ZF=0), PC+4+d7(label)+H→PC if(ZF=1), PC+4→PC	--	--	--	--	4	2/3				1000	1011	<d7.	...H							*2
	BNE label	if(ZF=0), PC+5+d11(label)+H→PC if(ZF=1), PC+5→PC	--	--	--	--	5	2/3				1001	1011	<d11	....	...H						*3
	BGE label	if((VF^NF)=0),PC+4+d7(label)+H→PC if((VF^NF)=1),PC+4→PC	--	--	--	--	4	2/3				1000	1000	<d7.	...H							*2
	BGE label	if((VF^NF)=0),PC+5+d11(label)+H→PC if((VF^NF)=1),PC+5→PC	--	--	--	--	5	2/3				1001	1000	<d11	....	...H						*3
	BCC label	if(CF=0),PC+4+d7(label)+H→PC if(CF=1), PC+4→PC	--	--	--	--	4	2/3				1000	1100	<d7.	...H							*2
	BCC label	if(CF=0), PC+5+d11(label)+H→PC if(CF=1), PC+5→PC	--	--	--	--	5	2/3				1001	1100	<d11	....	...H						*3
	BCS label	if(CF=1),PC+4+d7(label)+H→PC if(CF=0), PC+4→PC	--	--	--	--	4	2/3				1000	1101	<d7.	...H							*2
	BCS label	if(CF=1), PC+5+d11(label)+H→PC if(CF=0), PC+5→PC	--	--	--	--	5	2/3				1001	1101	<d11	....	...H						*3
	BLT label	if((VF^NF)=1),PC+4+d7(label)+H→PC if((VF^NF)=0),PC+4→PC	--	--	--	--	4	2/3				1000	1110	<d7.	...H							*2
	BLT label	if((VF^NF)=1),PC+5+d11(label)+H→PC if((VF^NF)=0),PC+5→PC	--	--	--	--	5	2/3				1001	1110	<d11	....	...H						*3
	BLE label	if((VF^NF)|ZF=1),PC+4+d7(label)+H→PC if((VF^NF)|ZF=0),PC+4→PC	--	--	--	--	4	2/3				1000	1111	<d7.	...H							*2
	BLE label	if((VF^NF)|ZF=1),PC+5+d11(label)+H→PC if((VF^NF)|ZF=0),PC+5→PC	--	--	--	--	5	2/3				1001	1111	<d11	....	...H						*3
	BGT label	if((VF^NF)|ZF=0),PC+5+d7(label)+H→PC if((VF^NF)|ZF=1),PC+5→PC	--	--	--	--	5	3/4			0010	0010	0001	<d7.	...H							*2

*1 d4 sign-extension
*2 d7 sign-extension
*3 d11 sign-extension

MN101E SERIES INSTRUCTION SET

Group	Mnemonic	Operation	Flag				Code Size	Cycle	Re-peat	Exten-sion	Machine Code											Notes
			VF	NF	CF	ZF					1	2	3	4	5	6	7	8	9	10	11	
Bcc	BGT label	if((VF^NF)|ZF=0),PC+6+d11(label)+H→PC if((VF^NF)|ZF=1),PC+6→PC	--	--	--	--	6	3/4			0010	0011	0001	<d11	....	...H						*3
	BHI label	if(CFIZF=0),PC+5+d7(label)+H→PC if(CFIZF=1), PC+5→PC	--	--	--	--	5	3/4			0010	0010	0010	<d7.	...H							*2
	BHI label	if(CFIZF=0),PC+6+d11(label)+H→PC if(CFIZF=1), PC+6→PC	--	--	--	--	6	3/4			0010	0011	0010	<d11	....	...H						*3
	BLS label	if(CFIZF=1),PC+5+d7(label)+H→PC if(CFIZF=0), PC+5→PC	--	--	--	--	5	3/4			0010	0010	0011	<d7.	...H							*2
	BLS label	if(CFIZF=1),PC+6+d11(label)+H→PC if(CFIZF=0), PC+6→PC	--	--	--	--	6	3/4			0010	0011	0011	<d11	....	...H						*3
	BNC label	if(NF=0),PC+5+d7(label)+H→PC if(NF=1),PC+5→PC	--	--	--	--	5	3/4			0010	0010	0100	<d7.	...H							*2
	BNC label	if(NF=0),PC+6+d11(label)+H→PC if(NF=1),PC+6→PC	--	--	--	--	6	3/4			0010	0011	0100	<d11	....	...H						*3
	BNS label	if(NF=1),PC+5+d7(label)+H→PC if(NF=0),PC+5→PC	--	--	--	--	5	3/4			0010	0010	0101	<d7.	...H							*2
	BNS label	if(NF=1),PC+6+d11(label)+H→PC if(NF=0),PC+6→PC	--	--	--	--	6	3/4			0010	0011	0101	<d11	....	...H						*3
	BVC label	if(VF=0),PC+5+d7(label)+H→PC if(VF=1),PC+5→PC	--	--	--	--	5	3/4			0010	0010	0110	<d7.	...H							*2
	BVC label	if(VF=0),PC+6+d11(label)+H→PC if(VF=1),PC+6→PC	--	--	--	--	6	3/4			0010	0011	0110	<d11	....	...H						*3
	BVS label	if(VF=1),PC+5+d7(label)+H→PC if(VF=0),PC+5→PC	--	--	--	--	5	3/4			0010	0010	0111	<d7.	...H							*2
	BVS label	if(VF=1),PC+6+d11(label)+H→PC if(VF=0),PC+6→PC	--	--	--	--	6	3/4			0010	0011	0111	<d11	....	...H						*3
	BRA label	PC+3+d4(label)+H→PC	--	--	--	--	3	3				1110	111H	<d4>								*1
	BRA label	PC+4+d7(label)+H→PC	--	--	--	--	4	3				1000	1001	<d7.	...H							*2
	BRA label	PC+5+d11(label)+H→PC	--	--	--	--	5	3				1001	1001	<d11	....	...H						*3
CBEQ	CBEQ imm8,Dm,label	if(Dm=imm8),PC+6+d7(label)+H→PC if(Dm≠imm8),PC+6→PC	●	●	●	●	6	3/4				1100	10Dm	<#8.	...>	<d7.	...H					*2
	CBEQ imm8,Dm,label	if(Dm=imm8),PC+8+d11(label)+H→PC if(Dm≠imm8),PC+8→PC	●	●	●	●	8	4/5			0010	1100	10Dm	<#8.	...>	<d11	....	...H				*3
	CBEQ imm8,(abs8),label	if(mem8(abs8)=imm8),PC+9+d7(label)+H→PC if(mem8(abs8)≠imm8),PC+9→PC	●	●	●	●	9	6/7			0010	1101	1100	<abs	8..>	<#8.	...>	<d7.	...H			*2
	CBEQ imm8,(abs8),label	if(mem8(abs8)=imm8),PC+10+d11(label)+H→PC if(mem8(abs8)≠imm8),PC+10→PC	●	●	●	●	10	6/7			0010	1101	1101	<abs	8..>	<#8.	...>	<d11	....	...H		*3
	CBEQ imm8,(abs16),label	if(mem8(abs16)=imm8),PC+11+d7(label)+H→PC if(mem8(abs16)≠imm8),PC+11→PC	●	●	●	●	11	7/8			0011	1101	1100	<abs	16..	....	...>	<#8.	...>	<d7.	...H	*2
	CBEQ imm8,(abs16),label	if(mem8(abs16)=imm8),PC+12+d11(label)+H→PC if(mem8(abs16)≠imm8),PC+12→PC	●	●	●	●	12	7/8			0011	1101	1101	<abs	16..	....	...>	<#8.	...>	<d11	....	...H	*3
CBNE	CBNE imm8,Dm,label	if(Dm≠imm8),PC+6+d7(label)+H→PC if(Dm=imm8),PC+6→PC	●	●	●	●	6	3/4				1101	10Dm	<#8.	...>	<d7.	..H>					*2
	CBNE imm8,Dm,label	if(Dm≠imm8),PC+8+d11(label)+H→PC if(Dm=imm8),PC+8→PC	●	●	●	●	8	4/5			0010	1101	10Dm	<#8.	...>	<d11	....	...H				*3
	CBNE imm8,(abs8),label	if(mem8(abs8)≠imm8),PC+9+d7(label)+H→PC if(mem8(abs8)=imm8),PC+9→PC	●	●	●	●	9	6/7			0010	1101	1110	<abs	8..>	<#8.	...>	<d7.	...H			*2
	CBNE imm8,(abs8),label	if(mem8(abs8)≠imm8),PC+10+d11(label)+H→PC if(mem8(abs8)=imm8),PC+10→PC	●	●	●	●	10	6/7			0010	1101	1111	<abs	8..>	<#8.	...>	<d11	....	...H		*3
	CBNE imm8,(abs16),label	if(mem8(abs16)≠imm8),PC+11+d7(label)+H→PC if(mem8(abs16)=imm8),PC+11→PC	●	●	●	●	11	7/8			0011	1101	1110	<abs	16..	....	...>	<#8.	...>	<d7.	...H	*2
	CBNE imm8,(abs16),label	if(mem8(abs16)≠imm8),PC+12+d11(label)+H→PC if(mem8(abs16)=imm8),PC+12→PC	●	●	●	●	12	7/8			0011	1101	1111	<abs	16..	....	...>	<#8.	...>	<d11	....	...H	*3
TBZ	TBZ (abs8)bp,label	if(mem8(abs8)bp=0),PC+7+d7(label)+H→PC if(mem8(abs8)bp=1),PC+7→PC	0	●	0	●	7	6/7			0011	0000	0bp.	<abs	8..>	<d7.	...H					*2
	TBZ (abs8)bp,label	if(mem8(abs8)bp=0),PC+8+d11(label)+H→PC if(mem8(abs8)bp=1),PC+8→PC	0	●	0	●	8	6/7			0011	0000	1bp.	<abs	8..>	<d11	....	...H				*3

*1 d4 sign-extension
*2 d7 sign-extension
*3 d11 sign-extension

MN101E SERIES INSTRUCTION SET

Group	Mnemonic	Operation	Flag VF	Flag NF	Flag CF	Flag ZF	Code Size	Cycle	Re-peat	Extension	Machine Code 1	2	3	4	5	6	7	8	9	10	11	Notes
TBZ	TBZ (io8)bp,label	if(mem8(IOTOP+io8)bp=0),PC+7+d7(label)+H→PC if(mem8(IOTOP+io8)bp=1),PC+7→PC	0	●	0	●	7	6/7		0011	0100	0bp.	<io8	...>	<d7.	...H						*1
	TBZ (io8)bp,label	if(mem8(IOTOP+io8)bp=0),PC+8+d11(label)+H→PC if(mem8(IOTOP+io8)bp=1),PC+8→PC	0	●	0	●	8	6/7		0011	0100	1bp.	<io8	...>	<d11	....	...H					*2
	TBZ (abs16)bp,label	if(mem8(abs16)bp=0),PC+9+d7(label)+H→PC if(mem8(abs16)bp=1),PC+9→PC	0	●	0	●	9	7/8		0011	1110	0bp.	<abs	16..	....	...>	<d7.	...H				*1
	TBZ (abs16)bp,label	if(mem8(abs16)bp=0),PC+10+d11(label)+H→PC if(mem8(abs16)bp=1),PC+10→PC	0	●	0	●	10	7/8		0011	1110	1bp.	<abs	16..	....	...>	<d11	....	...H			*2
TBNZ	TBNZ (abs8)bp,label	if(mem8(abs8)bp=1),PC+7+d7(label)+H→PC if(mem8(abs8)bp=0),PC+7→PC	0	●	0	●	7	6/7		0011	0001	0bp.	<abs	8..>	<d7.	...H						*1
	TBNZ (abs8)bp,label	if(mem8(abs8)bp=1),PC+8+d11(label)+H→PC if(mem8(abs8)bp=0),PC+8→PC	0	●	0	●	8	6/7		0011	0001	1bp.	<abs	8..>	<d11	....	...H					*2
	TBNZ (io8)bp,label	if(mem8(io)bp=1),PC+7+d7(label)+H→PC if(mem8(io)bp=0),PC+7→PC	0	●	0	●	7	6/7		0011	0101	0bp.	<io8	...>	<d7.	...H						*1
	TBNZ (io8)bp,label	if(mem8(io)bp=1),PC+8+d11(label)+H→PC if(mem8(io)bp=0),PC+8→PC	0	●	0	●	8	6/7		0011	0101	1bp.	<io8	...>	<d11	....	...H					*2
	TBNZ (abs16)bp,label	if(mem8(abs16)bp=1),PC+9+d7(label)+H→PC if(mem8(abs16)bp=0),PC+9→PC	0	●	0	●	9	7/8		0011	1111	0bp.	<abs	16..	....	...>	<d7.	...H				*1
	TBNZ (abs16)bp,label	if(mem8(abs16)bp=1),PC+10+d11(label)+H→PC if(mem8(abs16)bp=0),PC+10→PC	0	●	0	●	10	7/8		0011	1111	1bp.	<abs	16..	....	...>	<d11	....	...H			*2
JMP	JMP (An)	0→PC.17-16,An→PC.15-0,0→PC.H	---	---	---	---	3	4		0010	0001	00A0										
	JMP label	abs18(label)+H→PC	---	---	---	---	7	5		0011	1001	0aaH	<abs	18.b	p15~	0..>						*5
	JMP label	abs20(label)+H→PC	---	---	---	---	9	6		0011	1101	1010	000B	bbbH	<abs	20.b	p15~	0..>				*6*7
JSR	JSR (An)	SP-3→SP,(PC+3).bp7-0→mem8(SP) (PC+3).bp15-8→mem8(SP+1) (PC+3).H→mem8(SP+2).bp7, 0→mem8(SP+2).bp6-4, (PC+3).bp19-16→mem8(SP+2).bp3-0 0→PC.bp19-16 An→PC.bp15-0,0→PC.H	---	---	---	---	3	7		0010	0001	00A1										
	JSR label	SP-3→SP,(PC+5).bp7-0→mem8(SP) (PC+5).bp15-8→mem8(SP+1) (PC+5).H→mem8(SP+2).bp7, 0→mem8(SP+2).bp6-4, (PC+5).bp19-16→mem8(SP+2).bp3-0 PC+5+d12(label)+H→PC	---	---	---	---	5	6			0001	000H	<d12	....	...>							*3
	JSR label	SP-3→SP,(PC+6).bp7-0→mem8(SP) (PC+6).bp15-8→mem8(SP+1) (PC+6).H→mem8(SP+2).bp7, 0→mem8(SP+2).bp6-4, (PC+6).bp19-16→mem8(SP+2).bp3-0 PC+6+d16(label)+H→PC	---	---	---	---	6	7			0001	001H	<d16	....	....	...>						*4
	JSR label	SP-3→SP,(PC+7).bp7-0→mem8(SP) (PC+7).bp15-8→mem8(SP+1) (PC+7).H→mem8(SP+2).bp7, 0→mem8(SP+2).bp6-4, (PC+7).bp19-16→mem8(SP+2).bp3-0 abs18(label)+H→PC	---	---	---	---	7	8		0011	1001	1aaH	<abs	18.b	p15~	0..>						*5
	JSR label	SP-3→SP,(PC+7).bp7-0→mem8(SP) (PC+7).bp15-8→mem8(SP+1) (PC+7).H→mem8(SP+2).bp7, 0→mem8(SP+2).bp6-4, (PC+7).bp19-16→mem8(SP+2).bp3-0 abs20(label)+H→PC	---	---	---	---	9	9		0011	1101	1011	000B	bbbH	<abs	20.b	p15~	0..>				*6 *7
	JSRV (tbl4)	SP-3→SP,(PC+3).bp7-0→mem8(SP) (PC+3).bp15-8→mem8(SP+1) (PC+3).H→mem8(SP+2).bp7 0→mem8(SP+2).bp6-4, (PC+3).bp19-16→mem8(SP+2).bp3-0 mem8(x'004080+tbl4<<2)→PC.bp7-0 mem8(x'004080+tbl4<<2+1)→PC.bp15-8 mem8(x'004080+tbl4<<2+2).bp7→PC.H mem8(x'004080+tbl4<<2+2).bp3-0→ PC.bp19-16	---	---	---	---	3	9			1111	1110	<t4>									
NOP	NOP	PC+2→PC	---	---	---	---	2	1	○		0000	0000										

*1 d7 sign-extension
*2 d11 sign-extension
*3 d12 sign-extension
*4 d16 sign-extension
*5 aa=abs18.17 - 16
*6 B=abs20.19
*7 bbb=abs20.18 - 16

MN101E SERIES INSTRUCTION SET

Group	Mnemonic	Operation	Flag VF	Flag NF	Flag CF	Flag ZF	Code Size	Cycle	Re-peat	Exten-sion	Machine Code 1	2	3	4	5	6	7	8	9	10	11	Notes
RTS	RTS	mem8(SP)→(PC).bp7-0 mem8(SP+1)→(PC).bp15-8 mem8(SP+2).bp7→(PC).H mem8(SP+2).bp3-0→(PC).bp19-16 SP+3→SP	---	---	---	---	2	7			0000 0001											
RTI	RTI	mem8(SP)→PSW mem8(SP+1)→(PC).bp7-0 mem8(SP+2)→(PC).bp15-8 mem8(SP+3).bp7→(PC).H mem8(SP+3).bp3-0→(PC).bp19-16 mem8(SP+4)→HA-l mem8(SP+5)→HA-h SP+6→SP	●	●	●	●	2	11			0000 0011											
Contorl instructions																						
REP	REP imm3	imm3-1→RPC	---	---	---	---	3	2			0010 0001 1rep											*1
BE	BE	PSW & x'3F'→PSW	---	---	---	---	3	3			0010 0010 0000											
BD	BD	PSW | x'c0'→PSW	---	---	---	---	3	3			0010 0011 0000											

*1 no repeat whn imm3=0, (rep: imm3-1)

Other than the instruction of MN101E Series,the assembler of this Series has the following instructions as macro instructions.
The assembler will interpret the macro instructions below as the assembler instructions.

macro instructions		replaced instructions		remarks
INC	Dn	ADD	1,Dn	
DEC	Dn	ADD	-1,Dn	
INC	An	ADDW	1,An	
DEC	An	ADDW	-1,An	
INC2	An	ADDW	2,An	
DEC2	An	ADDW	-2,An	
CLR	Dn	SUB	Dn,Dm	n=m
ASL	Dn	ADD	Dn,Dm	n=m
LSL	Dn	ADD	Dn,Dm	n=m
ROL	Dn	ADDC	Dn,Dm	n=m
NEG	Dn	NOT ADD	Dn 1,Dn	
NOPL		MOVW	DWn,DWm	n=m
MOV	(SP),Dn	MOV	(0,SP),Dn	
MOV	Dn,(SP)	MOV	Dn,(0,SP)	
MOVW	(SP),DWn	MOVW	(0,SP),DWn	
MOVW	DWn,(SP)	MOVW	DWn,(0,SP)	
MOVW	(SP),An	MOVW	(0,SP),An	
MOVW	An,(SP)	MOVW	An,(0,SP)	

Ver3.3(2002.01.31)

19.2 Instruction Map

MN101E SERIES INSTRUCTION MAP

1st nibble\2nd nibble

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	NOP	RTS	MOV #8,(io8)	RTI	CMP #8,(abs8)/(abs12)		POP An		ADD #8,Dm				MOVW #8,DWm		MOVW #8,Am	
1	JSR d12(label)		JSR d16(label)		MOV #8,(abs8)/(abs12)		PUSH An		OR #8,Dm				AND #8,Dm			
2	When the exension code is b'oo10'															
3	When the extension code is b'0011'															
4	MOV (abs12),Dm				MOV (abs8),Dm				MOV (An),Dm							
5	MOV Dn,(abs12)				MOV Dn,(abs8)				MOV Dn,(Am)							
6	MOV (io8),Dm				MOV (d4,SP),Dm				MOV (d8,An),Dm							
7	MOV Dn,(io8)				MOV Dn,(d4,SP)				MOV Dn,(d8,Am)							
8	ADD #4,Dm				SUB Dn,Dn				BGE d7	BRA d7	BEQ d7	BNE d7	BCC d7	BCS d7	BLT d7	BLE d7
9	BEQ d4		BNE d4		MOVW DWn,(HA)		MOVW An,(HA)		BGE d11	BRA d11	BEQ d11	BNE d11	BCC d11	BCS d11	BLT d11	BLE d11
A	MOV Dn,Dm / MOV #8,Dm															
B	BSET (abs8)bp								BCLR (abs8)bp							
C	CMP #8,Dm				MOVW (abs8),Am		MOVW (abs8),DWm		CBEQ #8,Dm,d7				CMPW #16,DWm		MOVW #16,DWm	
D	MOV Dn,(HA)				MOVW An,(abs8)		MOVW DWn,(abs8)		CBNE #8,Dm,d7				CMPW #16,Am		MOVW #16,Am	
E	MOVW (An),DWm				MOVW (d4,SP),Am		MOVW (d4,SP),DWm		POP Dn				ADDW #4,Am		BRA d4	
F	MOVW DWn,(Am)				MOVW An,(d4,SP)		MOVW DWn,(d4,SP)		PUSH Dn				ADDW #8,SP	ADDW #4,SP	JSRV (tbl4)	

Extension code: b'0010'

2nd nible\3rd nibble

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	MOVW An,Am				CMPW An,Am				MOVW SP,Am		MOVW An,SP		BTST #8,Dm			
1	JMP (A0)	JSR (A0)	JMP (A1)	JSR (A1)	MOV PSW,Dm				REP #3							
2	BE	BGT d7	BHI d7	BLS d7	BNC d7	BNS d7	BVC d7	BVS d7	NOT Dn				ROR Dn			
3	BD	BGT d11	BHI d11	BLS d11	BNC d11	BNS d11	BVC d11	BVS d11	ASR Dn				LSR Dn			
4	SUBW DWn,DWm				SUBW #16,DWm		SUBW #16,Am		SUBW DWn,Am				MOVW DWn,Am			
5	ADDW DWn,DWm				ADDW #16,DWm		ADDW #16,Am		ADDW DWn,Am				CMPW DWn,Am			
6	MOV (d16,SP),Dm				MOV (d8,SP),Dm				MOV (d16,An),Dm							
7	MOV Dn,(d16,SP)				MOV Dn,(d8,SP)				MOV Dn,(d16,Am)							
8	MOVW DWn,DWm (NOPL @n=m)				CMPW DWn,DWm				ADDUW Dn,Am							
9	EXT Dn,DWm		AND #8,PSW	OR #8,PSW	MOV Dn,PSW				ADDSW Dn,Am							
A	SUB Dn,Dm / SUB #8,Dm															
B	SUBC Dn,Dm															
C	MOV (abs16),Dm				MOVW (abs16),Am		MOVW (abs16),DWm		CBEQ #8,Dm,d12				MOVW An,DWm			
D	MOV Dn,(abs16)				MOVW An,(abs16)		MOVW DWn,(abs16)		CBNE #8,Dm,d12				CBEQ #8,(abs8),d7/d11		CBNE #8,(abs8),d7/d11	
E	MOVW (d16,SP),Am		MOVW (d16,SP),DWm		MOVW (d8,SP),Am		MOVW (d8,SP),DWm		MOVW (An),Am				ADDW #8,Am		DIVU	
F	MOVW An,(d16,SP)		MOVW DWn,(d16,SP)		MOVW An,(d8,SP)		MOVW DWn,(d8,SP)		MOVW An,(Am)				ADDW #16,SP		MULU	

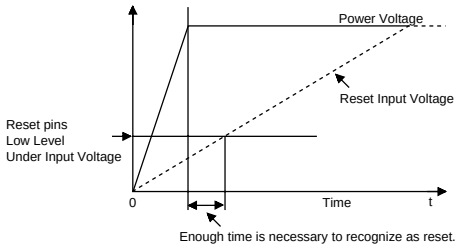
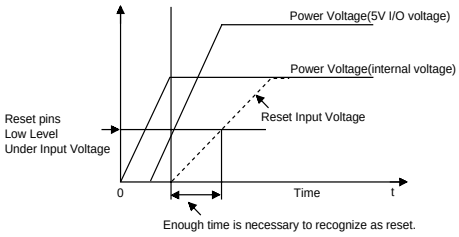
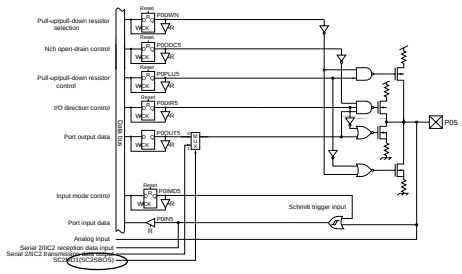
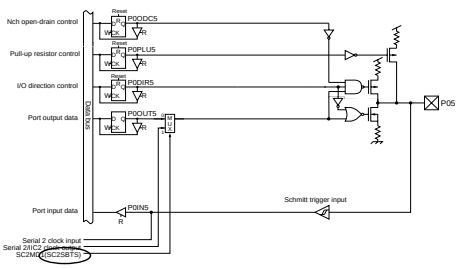
Extension code: b'0011'

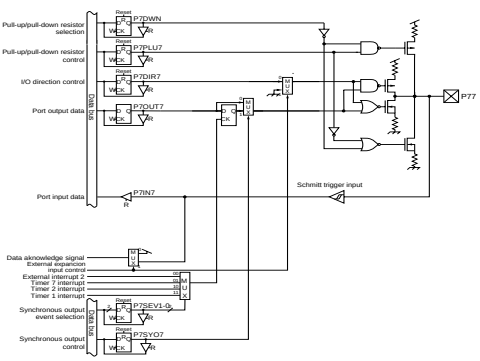
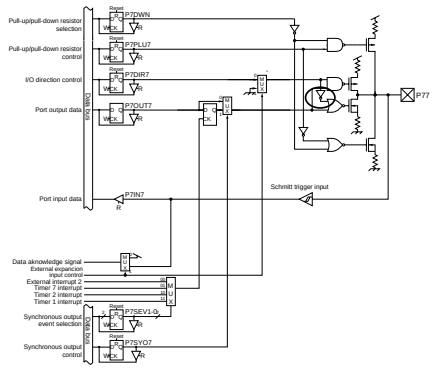
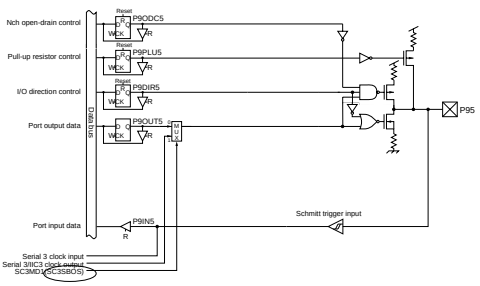
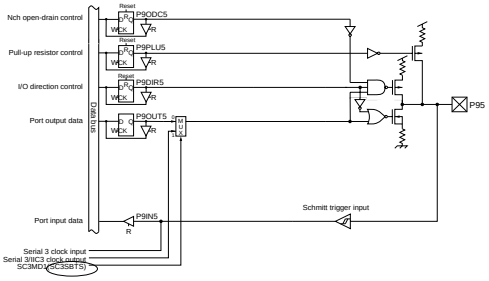
2nd nibble\ 3rd nibble	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	TBZ (abs8)bp,d7								TBZ (abs8)bp,d11							
1	TBNZ (abs8)bp,d7								TBNZ (abs8)bp,d11							
2	CMP Dn,Dm															
3	ADD Dn,Dm															
4	TBZ (io8)bp,d7								TBZ (io8)bp,d11							
5	TBNZ (io8)bp,d7								TBNZ (io8)bp,d11							
6	OR Dn,Dm															
7	AND Dn,Dm															
8	BSET (io8)bp								BCLR (io8)bp							
9	JMP abs18(label)								JSR abs18(label)							
A	XOR Dn,Dm / XOR #8,Dm															
B	ADDC Dn,Dm															
C	BSET (abs16)bp								BCLR (abs16)bp							
D	BTST (abs16)bp								cmp #8,(abs16)	mov #8,(abs16)	JMP abs20(label)	JSR abs20(label)	CBEQ #8,(abs16),d7/11		CBNE #8,(abs16),d7/11	
E	TBZ (abs16)bp,d7								TBZ (abs16)bp,d11							
F	TBNZ (abs16)bp,d7								TBNZ (abs16)bp,d11							

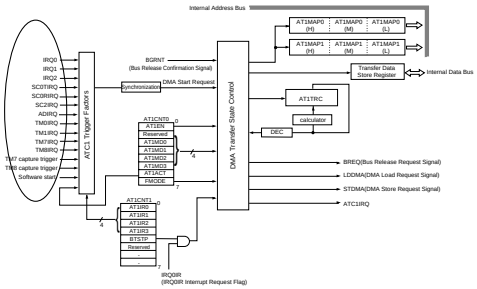
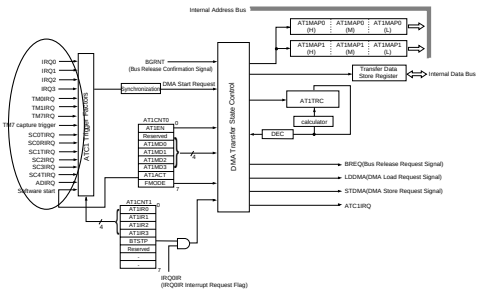
Ver2.1(2001.03.26)

Record of Changes

MN101E01L LSI Users Manual Record of Changes (Ver.0.65 to Ver.0.7)

Page	Section	Definition	Previous Edition (Ver.0.65)	New Edition (Ver.0.7)
I-35	Figure 1.7.5	Change		
II-5	Table 2.1.3	Change	Page No. CPUM II-44, II-49 MEMCTR II-37 RCCTR II-29 SBNKR II-18 DBNKR II-19 RCnAP II-30, II-32	Page No. CPUM II-51 MEMCTR II-38 RCCTR II-30 SBNKR II-19 DBNKR II-20 RCnAP II-31 to 32
III-53	Table 3.3.2	Change	Page No. NFCTR III-45 PSCMD III-44 EDGDT III-46 IRQSEL III-46 LVLMD III-46 IRQ1ICR III-20 IRQ3ICR III-46 IRQ4ICR III-22 IRQ5ICR III-46	Page No. NFCTR III-55 PSCMD III-54 EDGDT III-56 IRQSEL III-58 LVLMD III-59 IRQ1ICR III-21 IRQ3ICR III-23 IRQ4ICR III-24 IRQ5ICR III-31
IV-6	53	Change	The Port 0 output mode register (P0OMD) is	The Port 0 NcH open-drain control register (P0ODC) is .....
IV-12	Figure 4.2.6	Change		
IV-66	8 (bottom)	Change	.....at the memory extension model.	.....at the memory extension mode.

Page	Section	Defini-tion	Previous Edition (Ver.0.65)	New Edition (Ver.0.7)
IV-79	Figiure 4.9.8	Change		
IV-95	Figiure 4.11.6	Change		
IV-119	Table 4.16.1	Change	Page No. P7OUT P7DIR P7PLU P7SYO P7SEV	Page No. I0CTR IV-110
V-30	Table	Change	Description (6) ...so that the setting value is set to 249 (0x49)	Description (6) ...so that the setting value is set to 249 (0xF9)
V-33	Note (4)	Change	Timer can be recovered from STOP mode..	CPU can be recovered from STOP mode..
V-54	Table	Addition	Setup Procedure -	Setup Procedure TM1ICR (0x03FE9) bp1:TM1IE=0
VI-4	Table 6.2.1	Change	Timer 7 binary counter(lower 8 bit)	Timer 7 compare register 2-match interrupt control register
VI-20	Table	Deletion	Setup Procedure(3) TMSEL7	Setup Procedure(3) TMSEL
VIII-5	1	Change	(RMCTR:0x03F6E)	(RMCTR:0x03F7F)

Page	Section	Definition	Previous Edition (Ver.0.65)	New Edition (Ver.0.7)
VIII-8	Table	Change	Setup Procedure (6) - Description (6) Set the TM0PWM flag of the TM0MD register.....	Setup Procedure (6) bp6:TM0POP=0 Description (6) Set the TM0PWM flag and TM0MOD flag of the TM0MD register.....
XIV-44,45	Figure 14.3.21 14.3.22	Change	Write data to TXBUF2	Write data to TXBUF3
XV-45	Table 15.3.19	Change	TM50C	TM5OC
XVI-6	Table (bottom)	Change	bp6 1:...PD1(P23 L level), ...	bp6 1:...(P23, PD1 Falling edge), ...
XVI-10	Table 16.3.2	Change	fxx2	fx x 2
XVI-15	3	Change	....., and the sampling hold time is set to T_{AD} x 2.	....., and the sampling hold time is set to T_{AD} x 6.
XVIII-5	Figure 18.1.1	Change		

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